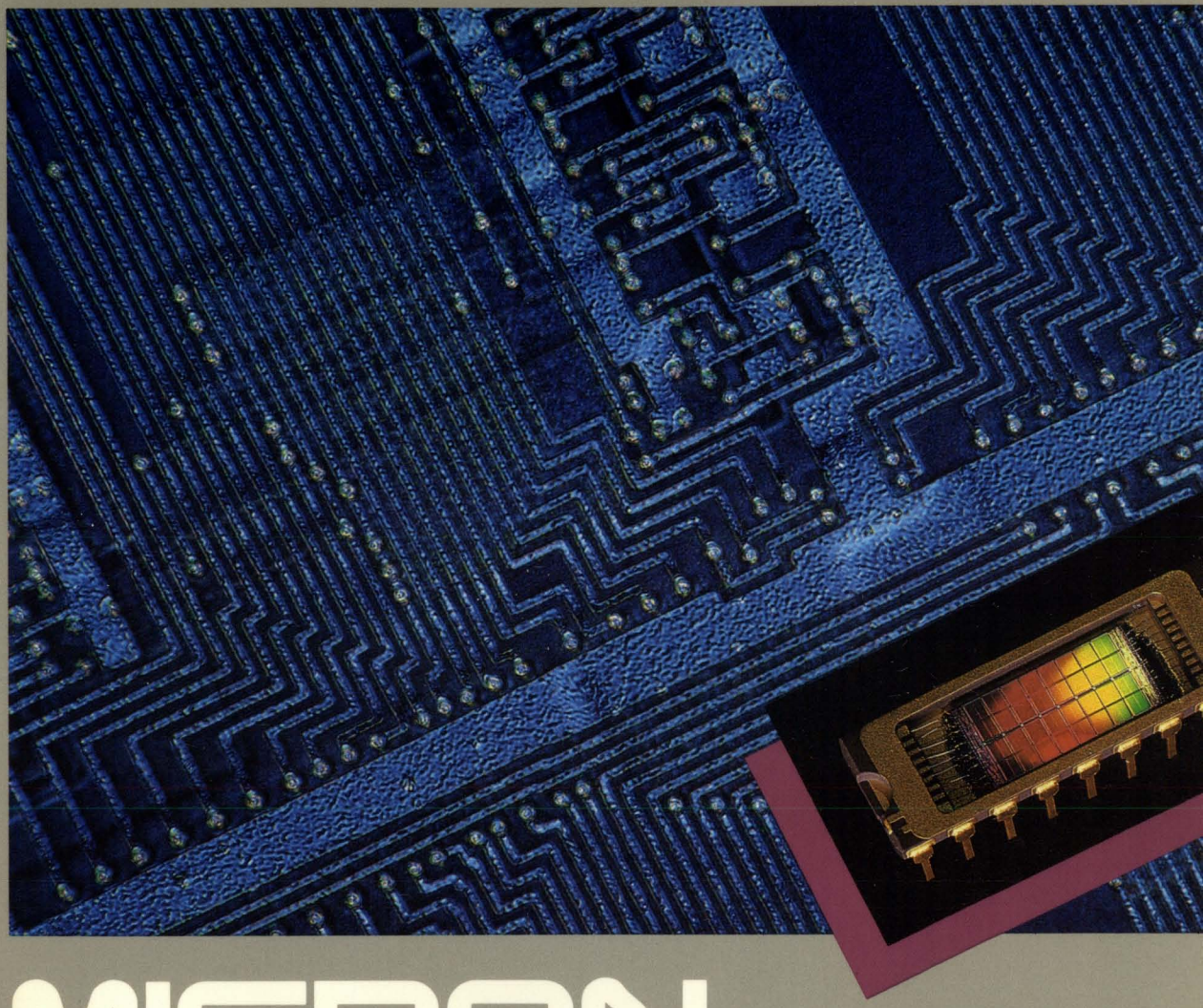
MOS DATA BOOK



MICRON

TECHNOLOGY, INC.

MICRON

MOS DATA BOOK

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1/90A

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The MOS Data Book has been organized into eleven sections and includes complete detailed specifications on our growing, high performance CMOS and NMOS product line.

Sections 1 through 7 cover individual product families. Each section contains a product selection guide followed by data sheets. Three different types of data sheets are used: Advance Information, which contains initial descriptions of products still under development; Preliminary Information, which contains initial device characterization limits which are subject to change upon full characterization of production devices; and Final Information, which contains minimum and maximum limits specified over the complete power supply and temperature range for production devices.

Section 8 contains application information.

Section 9 contains selected information about Micron's growing Defense Electronics product offering.

Section 10 contains packaging information.

Section 11 contains ordering information and a list of sales representatives and distributors by geographical location for the North American Continent, Europe and Asia.

Additional or updated information on any Micron product is available from:

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OE ..... With Output Enable
SI/O ..... Separate Data Inputs and Outputs
OT ..... Outputs Track Inputs During Write
HZ ..... High Impedance Outputs During Write

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E ..... With Expansion Logic
MB ..... With Mailbox Register Logic
VF ..... With Variable Flag Logic

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DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package and Number of Pins							Process	Page
				Standby	Active	PDIP	PLCC	ZIP	SOJ	CDIP	CLCC	Flat Pack		
64K x 1	Page Mode	MT4264	100,120,150,200	15mw	75mw	16	-	-	-	16	18	16	NMOS	1-3
64K x 4	Page Mode	MT4067	80,100,120,150	15mw	150mw	18	18	20	-	18	18	16	NMOS	1-13
256K x 1	Page Mode	MT1259	80,100,120,150	15mw	150mw	16	18	16	-	16	18	16	NMOS	1-23
256K x 4	Fast Page Mode	MT4C4256	80,100,120,150	5mw	175mw	20	-	20	20	20	-	20	CMOS	1-33
256K x 4	Stactic Column	MT4C4258	80,100,120,150	5mw	175mw	20	-	20	20	20	-	20	CMOS	1-43
1MEG x 1	Fast Page Mode	MT4C1024	80,100,120,150	5mw	175mw	18	-	20	20	18	-	18	CMOS	1-53
1MEG x 1	Nibble Mode	MT4C1025	80,100,120,150	5mw	175mw	18	-	20	20	18	-	18	CMOS	1-63
1MEG x 1	Static Column	MT4C1026	80,100,120,150	5mw	175mw	18	-	20	20	18	-	18	CMOS	1-73
1MEG x 4	Fast Page Mode	MT4C4001	80,100,120	5mw	175mw	20	-	-	20	20	-	-	CMOS	1-83
1MEG x 4	Static Column	MT4C4003	80,100,120	5mw	175mw	20	-	-	20	20	-	-	CMOS	1-93
4MEG x 1	Fast Page Mode	MT4C1004	80,100,120	5mw	175mw	18	-	-	20	18	-	-	CMOS	1-103
4MEG x 1	Nibble Mode	MT4C1005	80,100,120	5mw	175mw	18	-	-	20	18	-	-	CMOS	1-113
4MEG x 1	Static Column	MT4C1006	80,100,120	5mw	175mw	18	-	-	20	18	-	-	CMOS	1-123

DRAM

64K x 1 DRAM

PAGE MODE

FEATURES

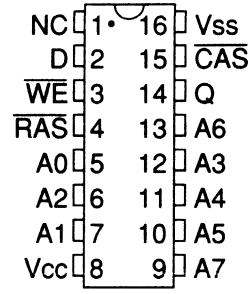
- Industry standard pin-out, functions and timing
- Single +5V ±10% power supply
- Low power, 15mW standby; 75mW active, typical
- Common I/O using EARLY-WRITE
- Q held indefinitely by $\overline{CAS}$
- 256 cycle refresh in 4ms
- Fully compatible with MT1259 (256K)
- Optional Page Mode access cycle

OPTIONS

	MARKING
• Timing	
100ns access	-10
120ns access	-12
150ns access	-15
200ns access	-20
• Packages:	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

16 Pin DIP
(PA, CA)



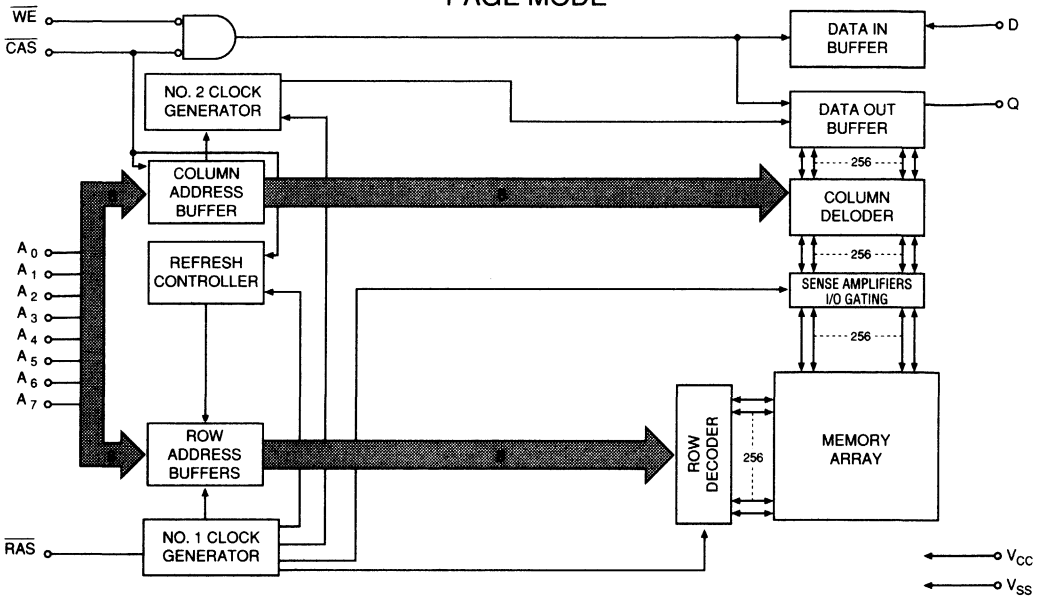
GENERAL DESCRIPTION

The MT4264 is a randomly accessed solid-state memory containing 65,536 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 16 address bits which are entered 8 bits (A0-A7) at a time. $\overline{RAS}$ is used to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY or HIDDEN refresh) so that all 256 combinations of $\overline{RAS}$ addresses (A0-A7) are executed at least every 4ms, regardless of sequence.

PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM
PAGE MODE



TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses		
				tR	tC	
Standby	H	H	H	X	X	High Impedance
READ	L	L	H	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In
PAGE-MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts	I_I	-10	10	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

(Notes: 1, 2, 3, 4, 6) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
STANDBY CURRENT ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}		4	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ Cycling)	I_{CC2}		30	mA	2
$\overline{RAS}$ ONLY REFRESH CURRENT ($\overline{CAS}$ = V_{IH})	I_{CC3}		20	mA	2
PAGE MODE CURRENT ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling)	I_{CC4}		30	mA	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_7, D	C_{I1}		5	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		8	pF	18
Output Capacitance: Q	C_O		8	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

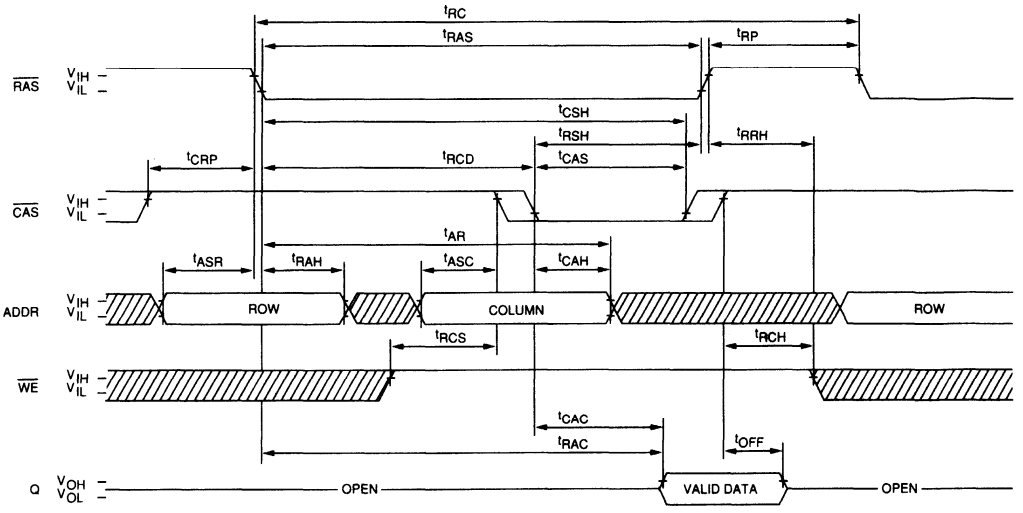
(Notes: 3, 4, 5, 10, 11, 17, 18) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-10		-12		-15		-20			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	t_{RC}	195		230		260		330		ns	6, 7
READ-MODIFY-WRITE cycle time	t_{RWC}	220		255		295		370		ns	
PAGE-MODE cycle time	t_{PC}	90		100		120		170		ns	6, 7
Access time from $\overline{RAS}$	t_{RAC}		100		120		150		200	ns	7, 8
Access time from $\overline{CAS}$	t_{CAC}		50		60		75		120	ns	7, 9
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	200	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50		60		75		100		ns	
$\overline{RAS}$ precharge time	t_{RP}	80	20,000	90	20,000	100	20,000	120	20,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10,000	60	10,000	75	10,000	120	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		200		ns	
$\overline{CAS}$ precharge time	t_{CPN}	25		25		30		35		ns	19
$\overline{CAS}$ precharge time (PAGE-MODE)	t_{CP}	30		30		35		40		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	50	25	60	25	75	30	80	ns	13
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	15		15		20		25		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	20		20		25		50		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	70		80		100		130		ns	
READ command set-up time	t_{RCS}	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	30	0	30	0	35	0	40	ns	12
$\overline{WE}$ command set-up time	t_{WCS}	0		0		0		0		ns	16
WRITE command hold time	t_{WCH}	35		40		45		60		ns	
WRITE command hold time referenced to $\overline{RAS}$	t_{WCR}	85		100		120		140		ns	
WRITE command pulse width	t_{WP}	35		40		45		50		ns	
WRITE command to $\overline{RAS}$ lead time	t_{RWL}	35		40		45		55		ns	
WRITE command to $\overline{CAS}$ lead time	t_{CWL}	35		40		45		55		ns	
Data-in set-up time	t_{DS}	0		0		0		0		ns	15
Data-in hold time	t_{DH}	35		40		45		55		ns	15
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	85		100		120		135		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		50		60		100		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	90		110		135		180		ns	16
Transition time (rise or fall)	t_T	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	t_{REF}		4		4		4		4	ms	
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRP}	10		15		20		20		ns	

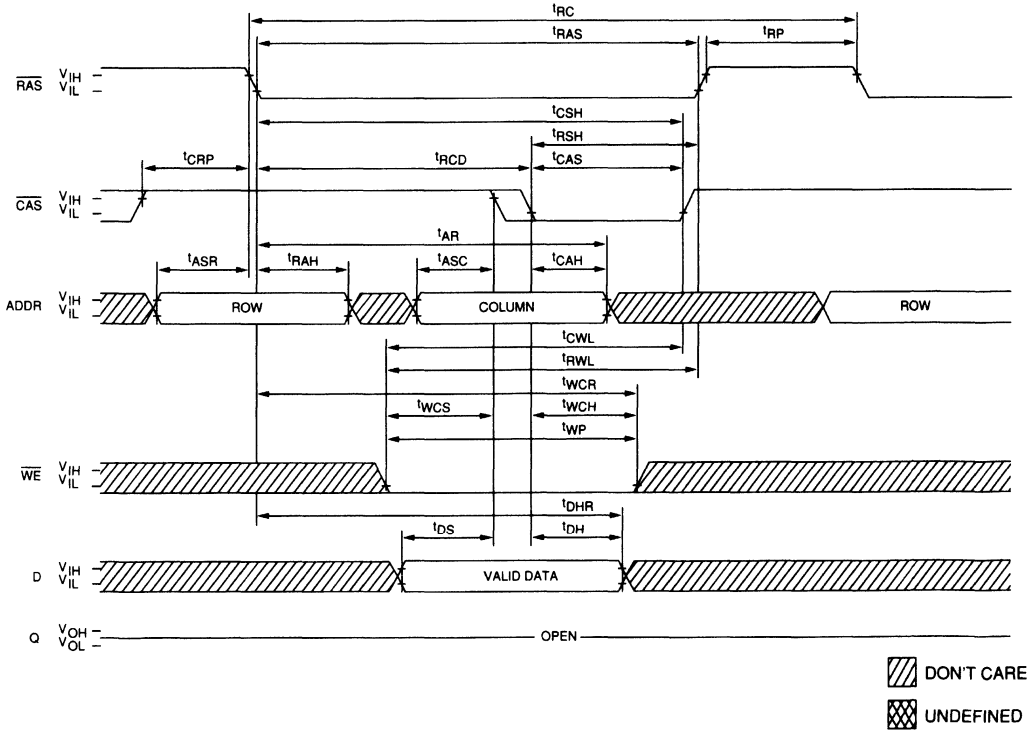
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
16. ^tWCS, ^tRWD and ^tCWD are restrictive operating parameters in late READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \ge ^tCWD$ (min) and $^tRWD \ge ^tRWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.

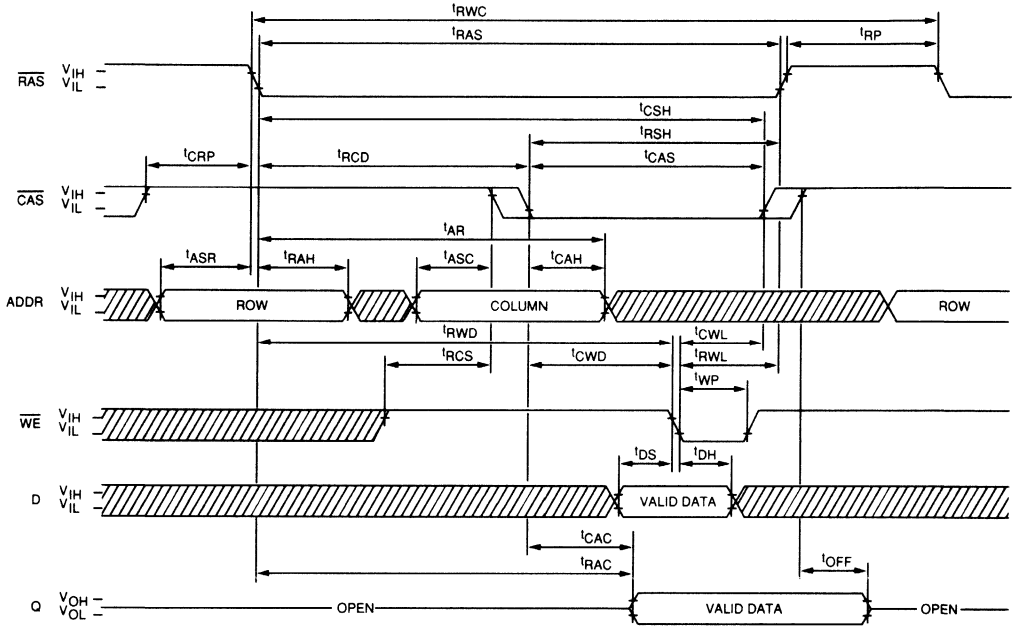
READ CYCLE



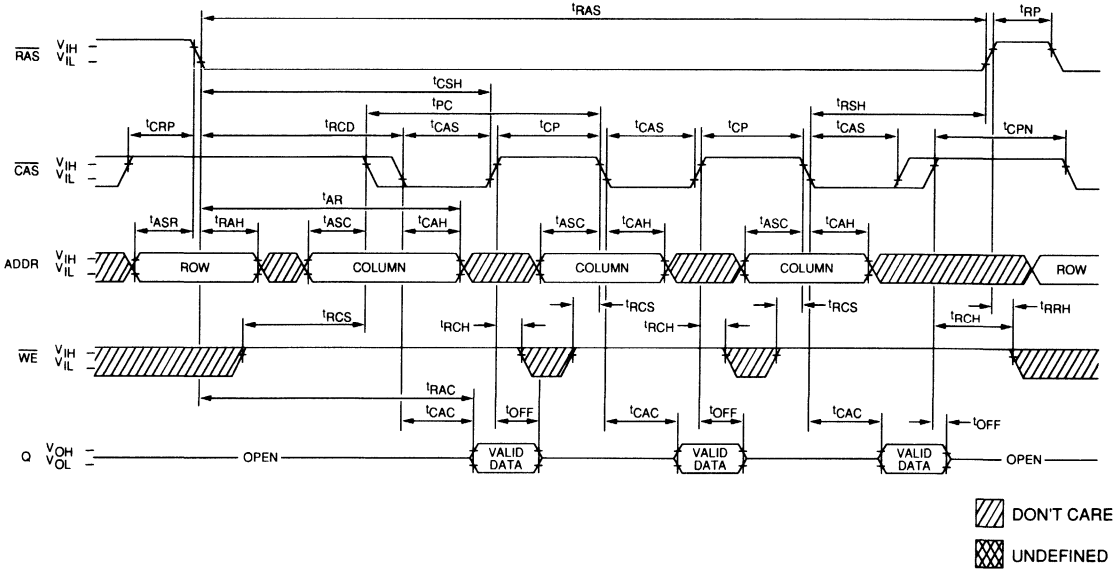
EARLY-WRITE CYCLE



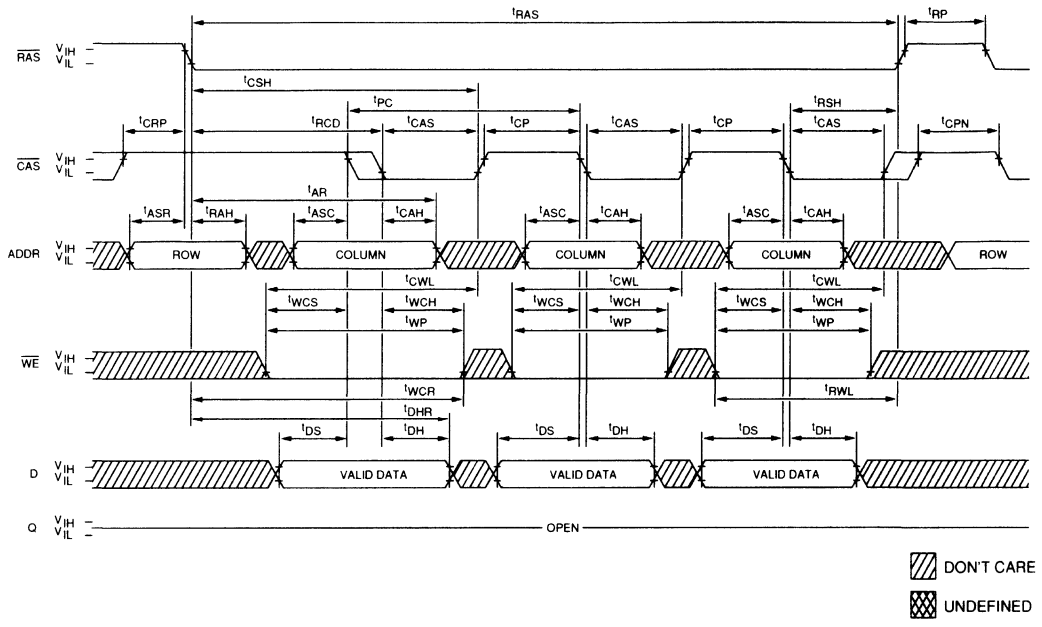
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE

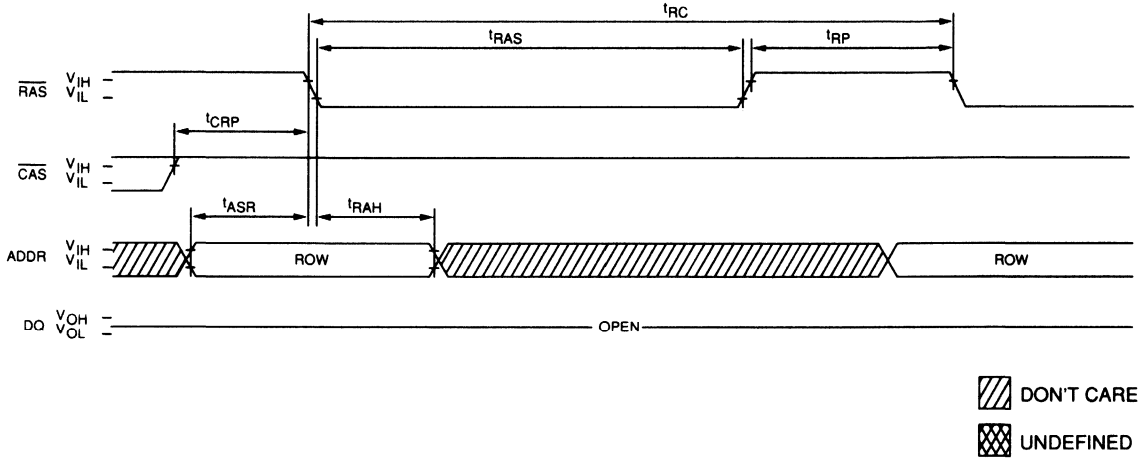


PAGE-MODE EARLY-WRITE CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7)



DRAM 64K x 4 DRAM

FEATURES

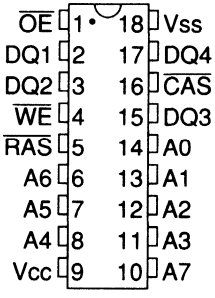
- Industry standard pin-out, timing and functions
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby; 150mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256 cycle refresh in 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

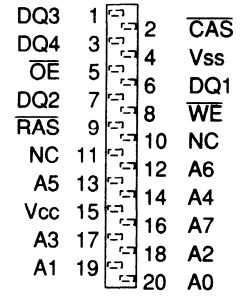
• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
150ns access	-15
• Packages:	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
PLCC	EJ

PIN ASSIGNMENT (Top View)

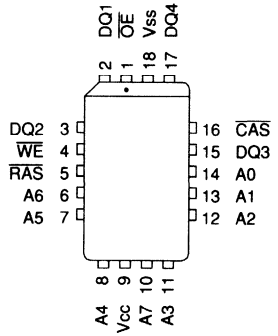
18 Pin DIP (PB, CB)



20 Pin ZIP (ZB)



18 Pin PLCC (EJA)

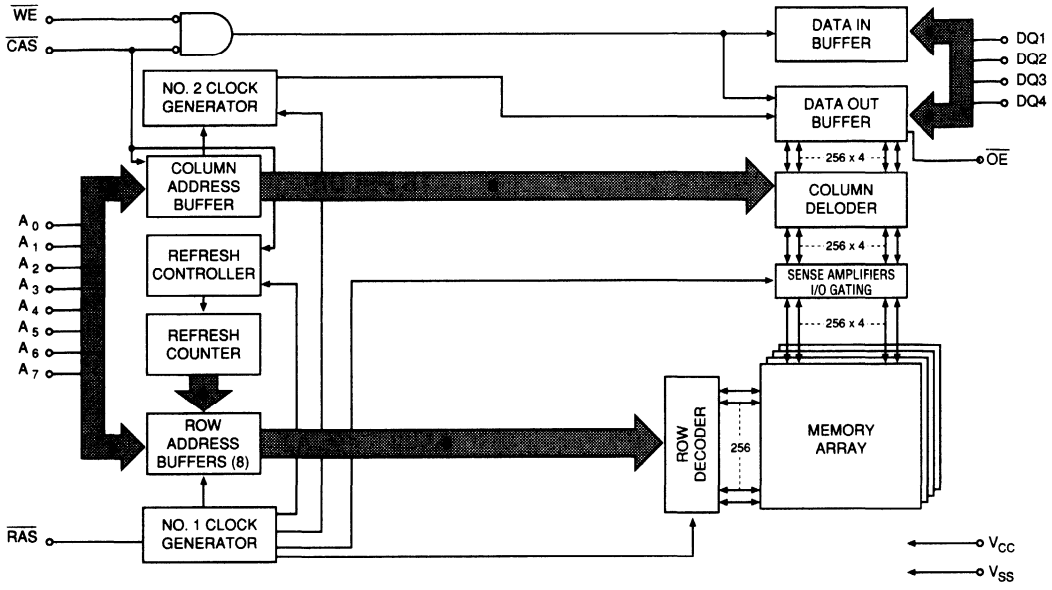


GENERAL DESCRIPTION

The MT4067 is a randomly accessed solid-state memory containing 262,144 bits organized in a x4 configuration. The 16 address bits are entered 8 bits at a time using $\overline{RAS}$ to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits. If the $\overline{WE}$ pin goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, the output pin is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-MODIFY-WRITE cycle. Data-in is latched when $\overline{WE}$ strobes LOW.

By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled to execute several faster READ, WRITE, READ-WRITE or READ-MODIFY-WRITE cycles within the $\overline{RAS}$ address defined page boundary. Returning $\overline{RAS}$ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM
PAGE MODE



TRUTH TABLE

Function	RAS	CAS	WE	OE	Addresses tR	Addresses tC	
Standby	H	H	H	H	X	X	High Impedance
READ	L	L	H	L	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	H	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	L→H	ROW	COL	Valid Data Out, Valid Data In
PAGE-MODE READ	L	H→L→H	H	L	ROW	COL	Valid Data Out, Valid Data Out
PAGE-MODE WRITE	L	H→L→H	L	H	ROW	COL	Valid Data In, Valid Data In
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	L→H	ROW	COL	Valid Data Out, Valid Data In
RAS ONLY REFRESH	L	H	H	H	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	H	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	H	H	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts	I_I	-10	10	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

(Notes: 1,2,3,4,6) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	5	5	5	5	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	65	55	55	45	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	65	55	55	45	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	55	40	40	35	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	65	55	55	45	mA	2,22

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		5	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		8	pF	18
Input/Output Capacitance: DQ	C_{IO}		7	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

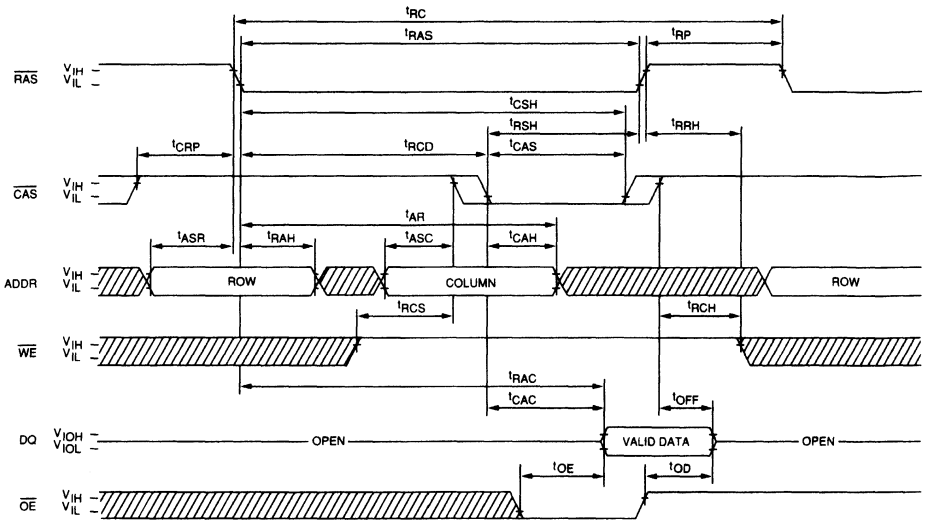
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	200		250		295		345		ns	
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
Output Enable	^tOE		25		25		30		40	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
Output Disable	^tOD		25		30		30		35	ns	
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time reference to $\overline{RAS}$	^tDHR	35		60		65		70		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	50		70		90		110		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	90		120		150		185		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	22
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	21
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$) refresh	^tCSR	10		15		20		20		ns	21
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		0		ns	21

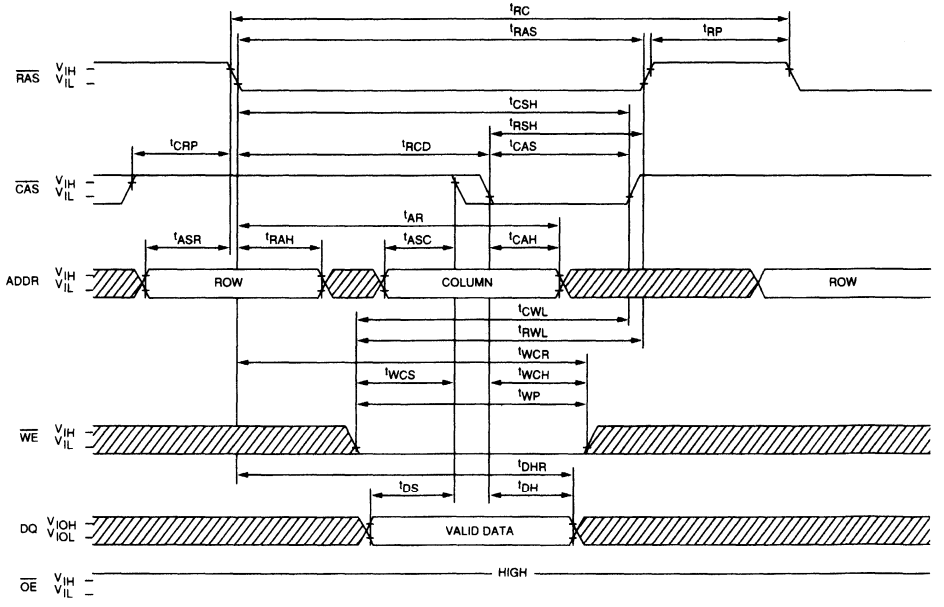
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \ge ^tCWD$ (min) and $^tRWD \ge ^tRWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. During a READ cycle if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, (V_{IH}) Q goes open. If $\overline{OE}$ is tied permanently LOW, a READ-MODIFY-WRITE operation is not possible.
21. On-chip refresh and address counters are enabled.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.

READ CYCLE



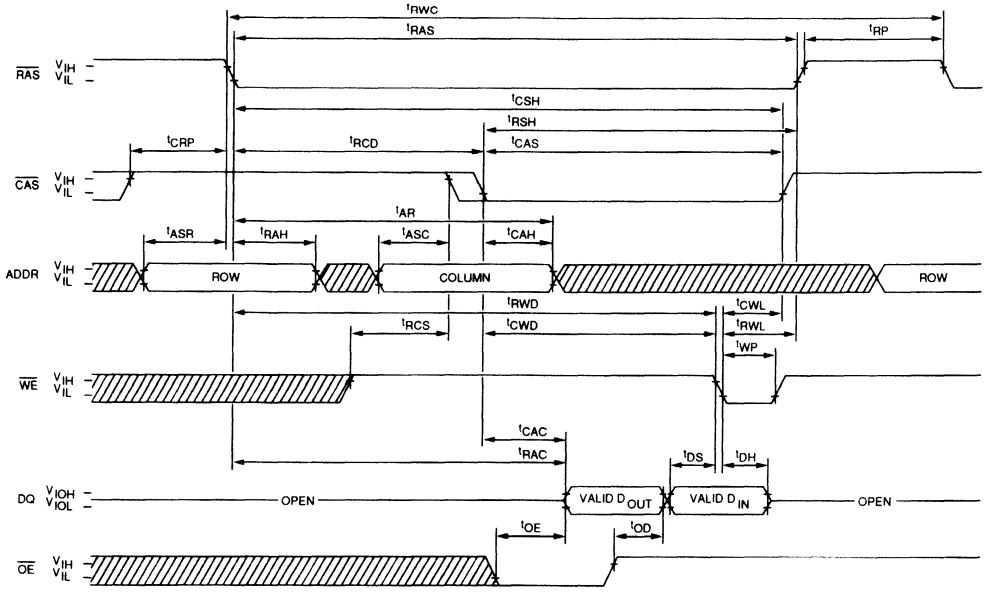
EARLY-WRITE CYCLE



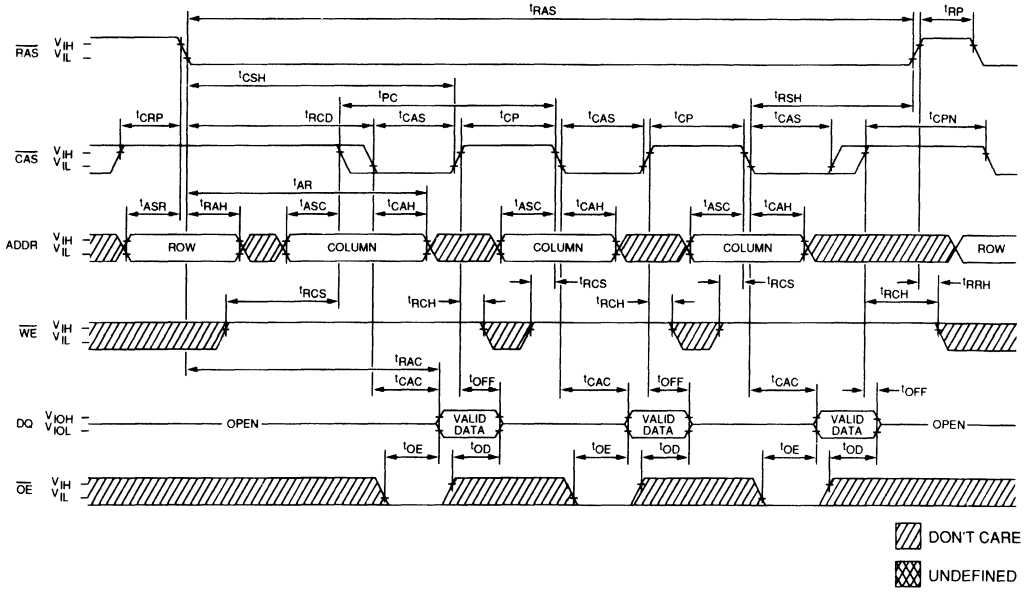
DON'T CARE

UNDEFINED

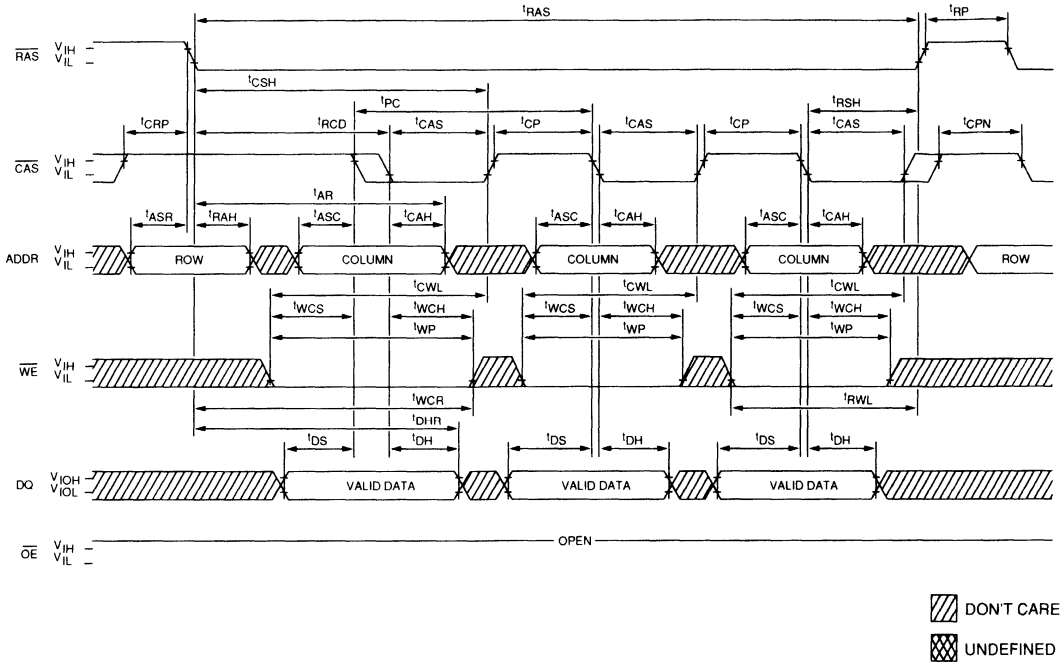
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE

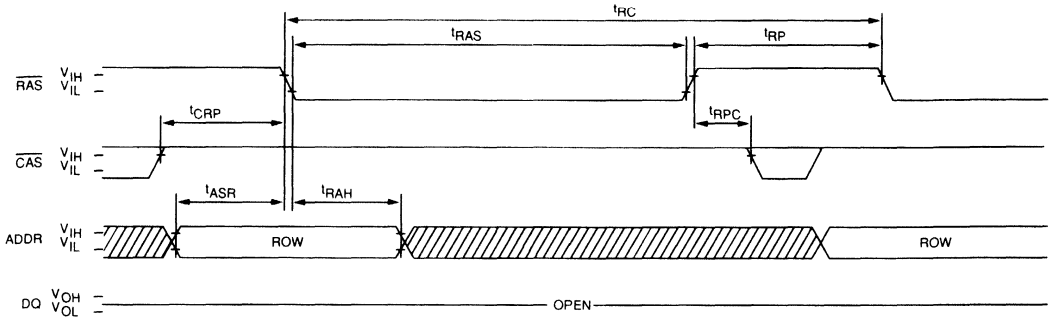


PAGE-MODE EARLY-WRITE CYCLE



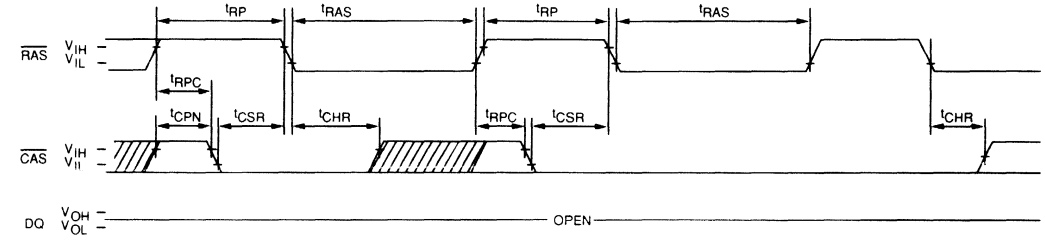
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; $\overline{WE}$ = DON'T CARE.)



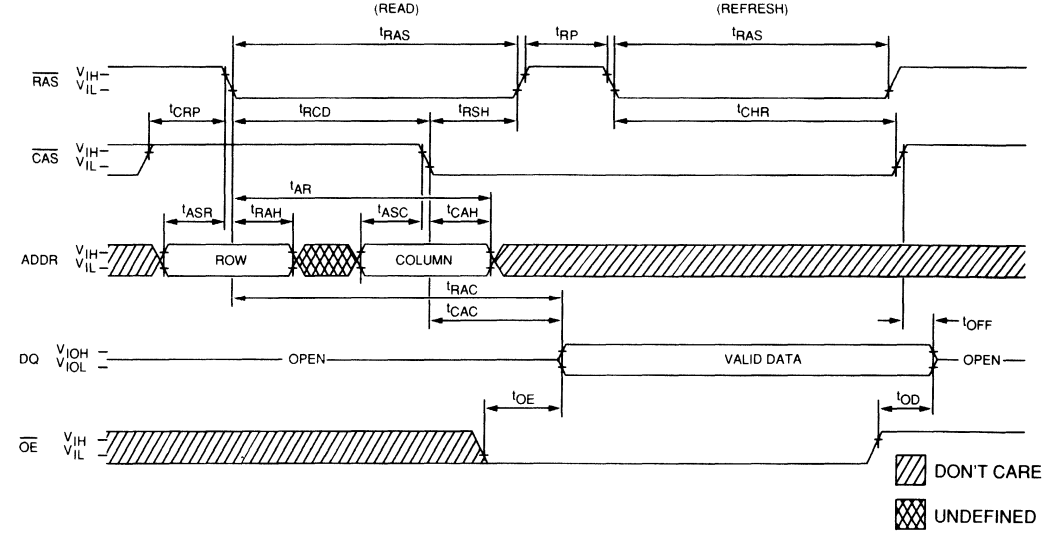
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_7, $\overline{WE}$, $\overline{OE}$ = DON'T CARE.)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[22]



DRAM 256K x 1 DRAM

FEATURES

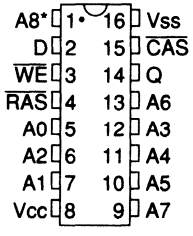
- Industry standard pin-out, timing and functions
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby; 150mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256 cycle refresh in 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

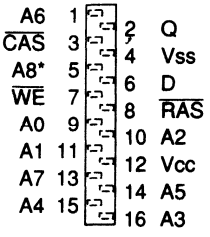
• Timing	
80ns access	-8
100ns access	-10
120ns access	-12
150ns access	-15
• Packages:	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
PLCC	EJ

PIN ASSIGNMENT (Top View)

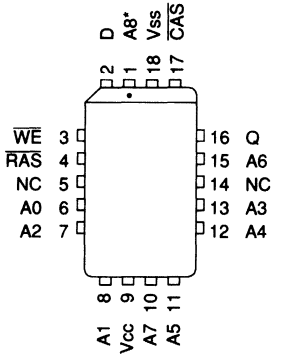
16 Pin DIP
(PA, CA)



16 Pin ZIP
(ZA)



18 Pin PLCC
(EJA)



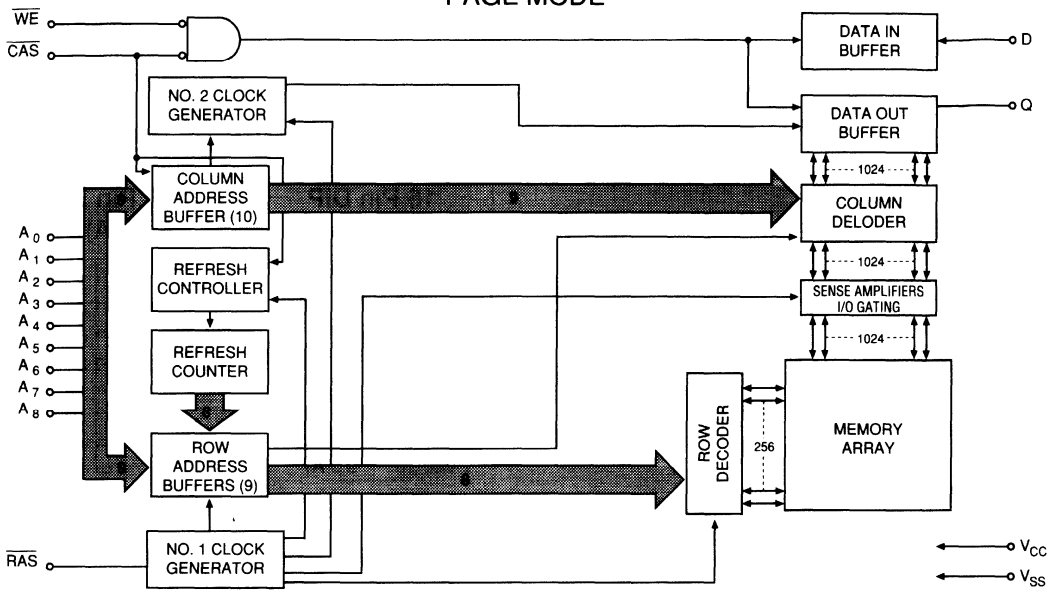
* ADDRESS NOT USED FOR $\overline{RAS}$ ONLY REFRESH

GENERAL DESCRIPTION

The MT1259 is a randomly accessed solid-state memory containing 262,144 bits organized in a x1 configuration. The 18 address bits are entered 9 bits at a time using $\overline{RAS}$ to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. If the $\overline{WE}$ pin goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, the output pin is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-MODIFY-WRITE cycle. Data-in is latched when $\overline{WE}$ strobes LOW.

By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled to execute several faster READ, WRITE, READ-WRITE or READ-MODIFY-WRITE cycles within the $\overline{RAS}$ address defined page boundary. Returning $\overline{RAS}$ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM
PAGE MODE



TRUTH TABLE

Function	RAS	CAS	WE	Addresses		
				tR	tC	
Standby	H	H	H	X	X	High Impedance
READ	L	L	H	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In
PAGE-MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts	I_I	-10	10	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

(Notes: 1,2,3,4,6) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	5	5	5	5	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	65	55	55	45	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	65	55	55	45	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	55	40	40	35	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	65	55	55	45	mA	2,20

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8, D	C_{I1}		5	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		8	pF	18
Output Capacitance: Q	C_O		7	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

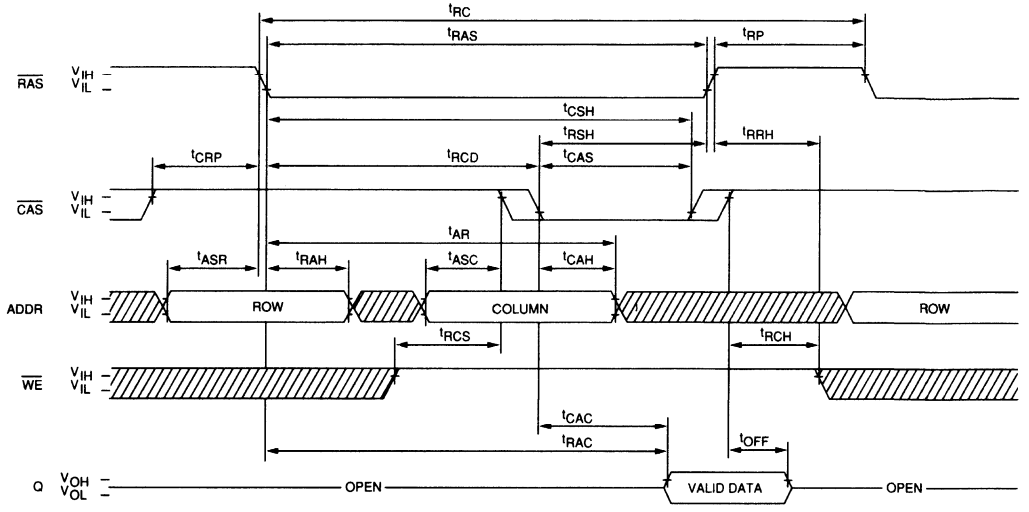
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	180		220		255		295		ns	
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	30		40		50		60		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	70		90		110		135		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	21
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	20
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$) refresh	^tCSR	10		15		20		20		ns	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		0		ns	20

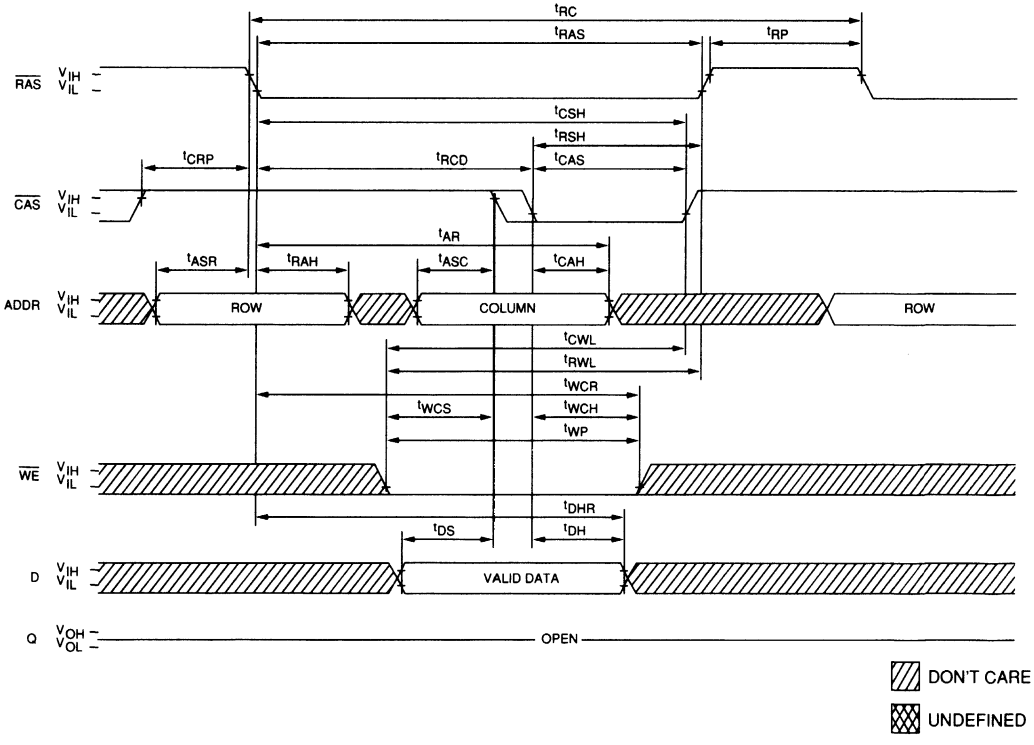
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge {}^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \ge {}^tCWD$ (min) and $^tRWD \ge {}^tRWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. On-chip refresh and address counters are enabled.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

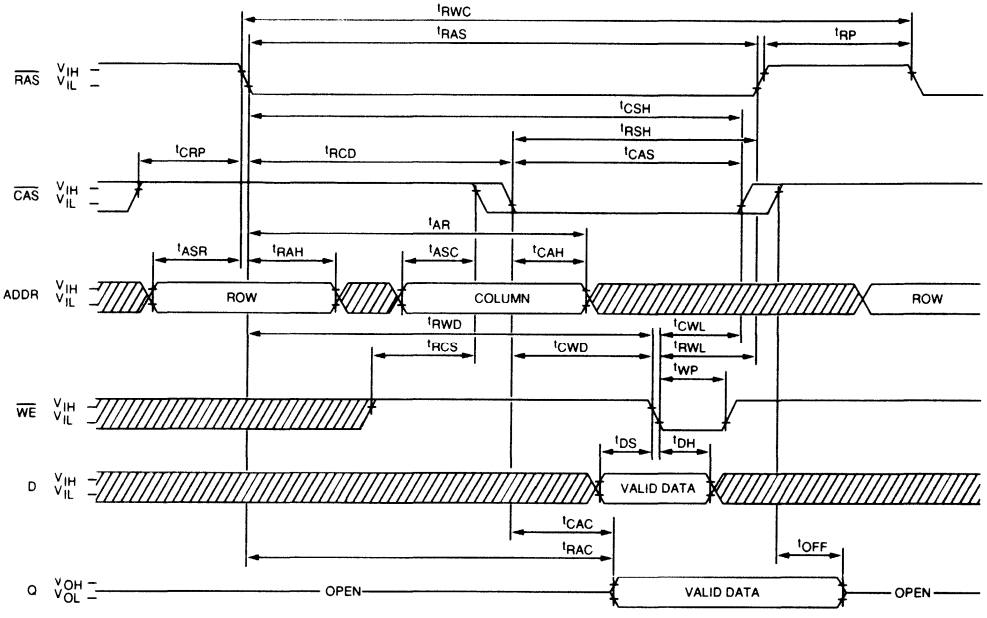
READ CYCLE



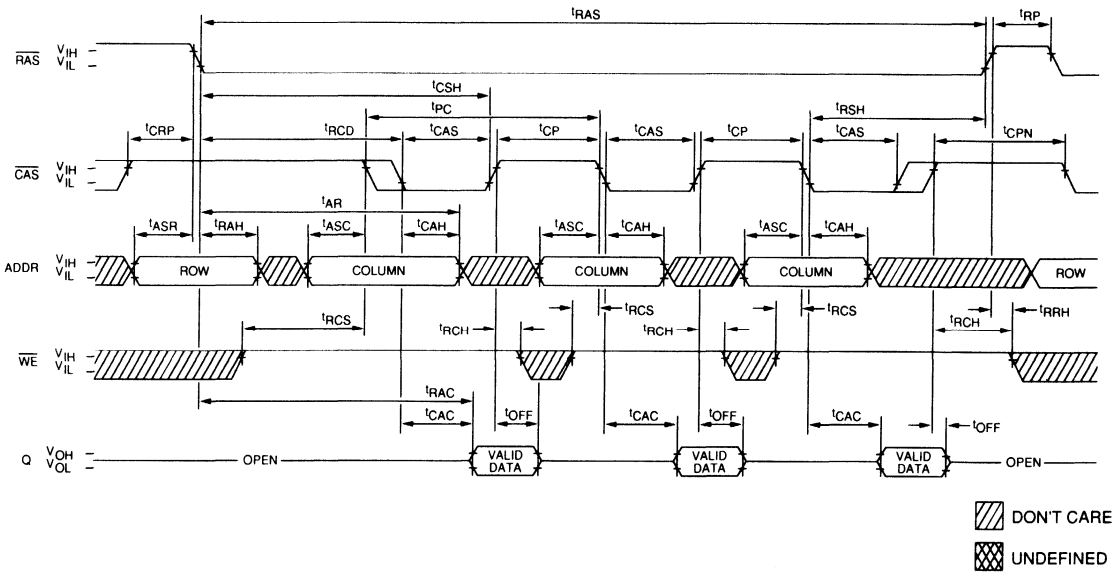
EARLY-WRITE CYCLE



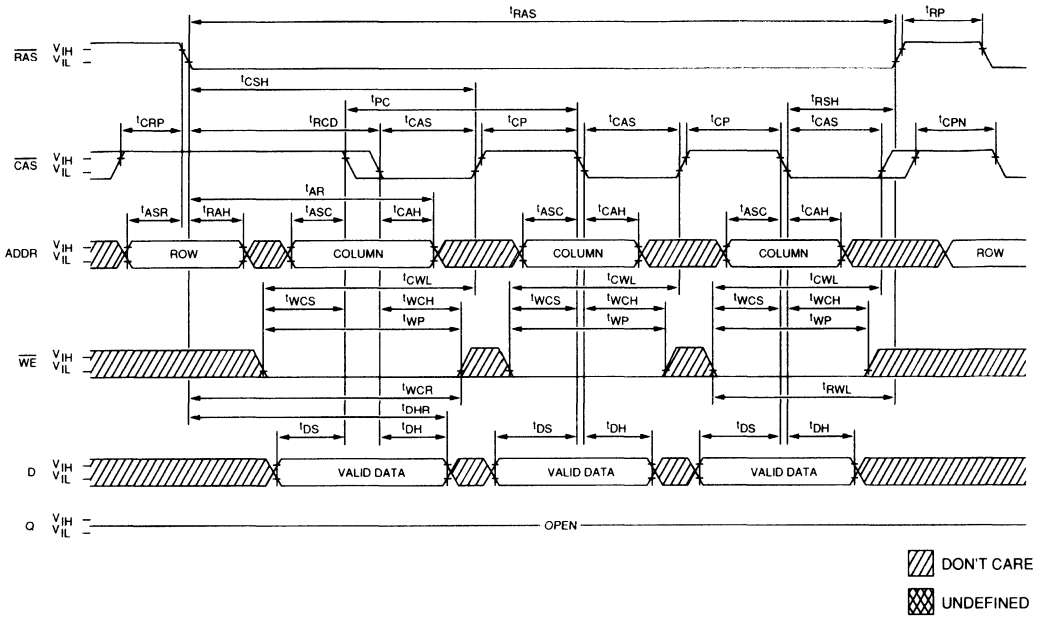
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE

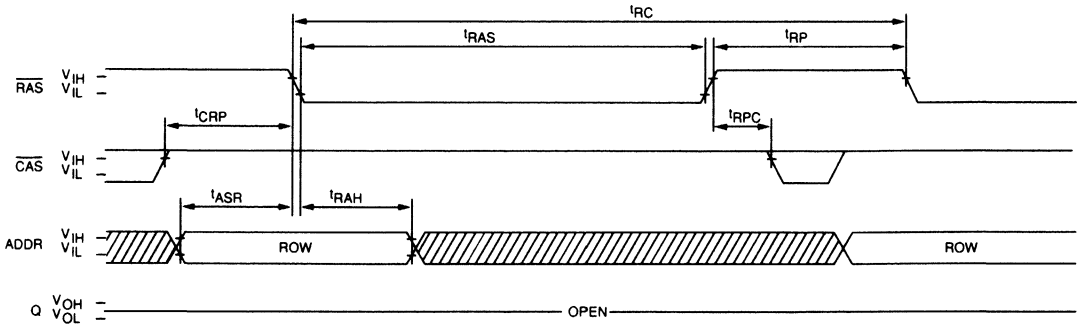


PAGE-MODE EARLY-WRITE CYCLE



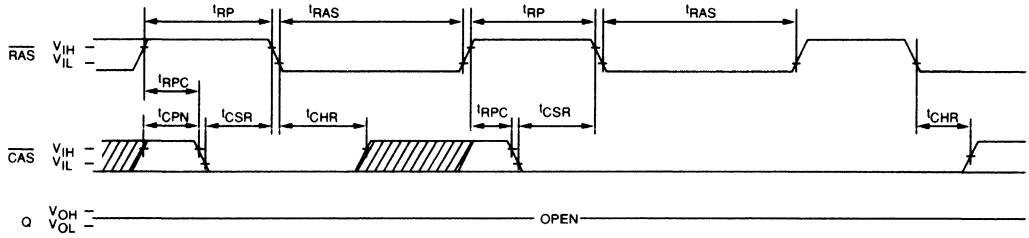
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



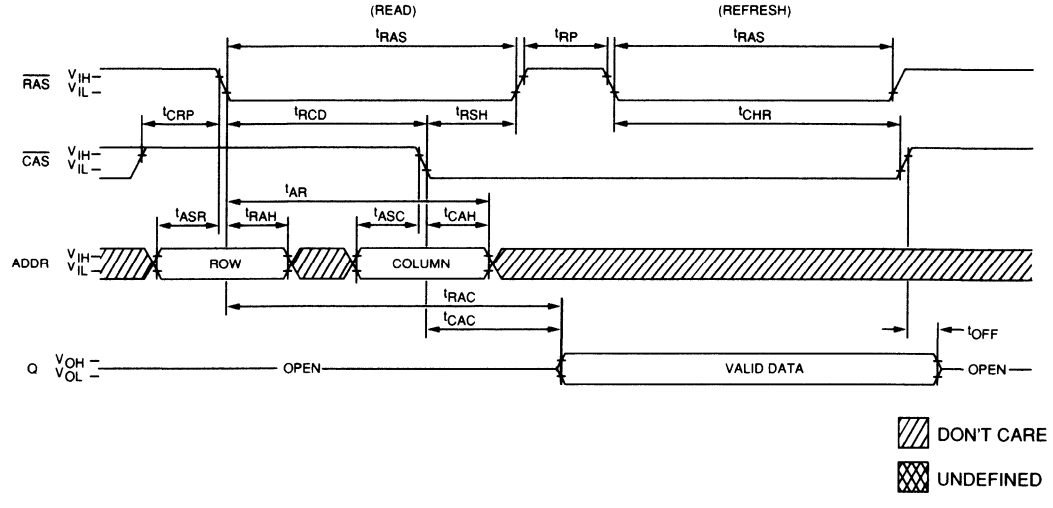
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8 and $\overline{WE}$ = DON'T CARE.)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[21]



DRAM

256K x 4 DRAM

FAST PAGE MODE

FEATURES

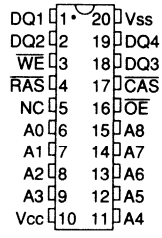
- Industry standard x4 pin-out, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh in 8ms
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional Fast Page Mode access cycle

OPTIONS

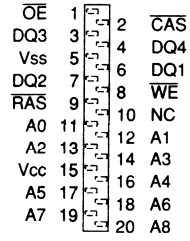
OPTIONS	MARKING
• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

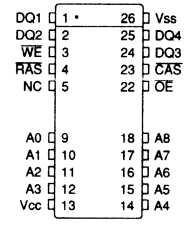
20 Pin DIP (PD, CD)



20 Pin ZIP (ZB)



20 Pin SOJ (DJA)



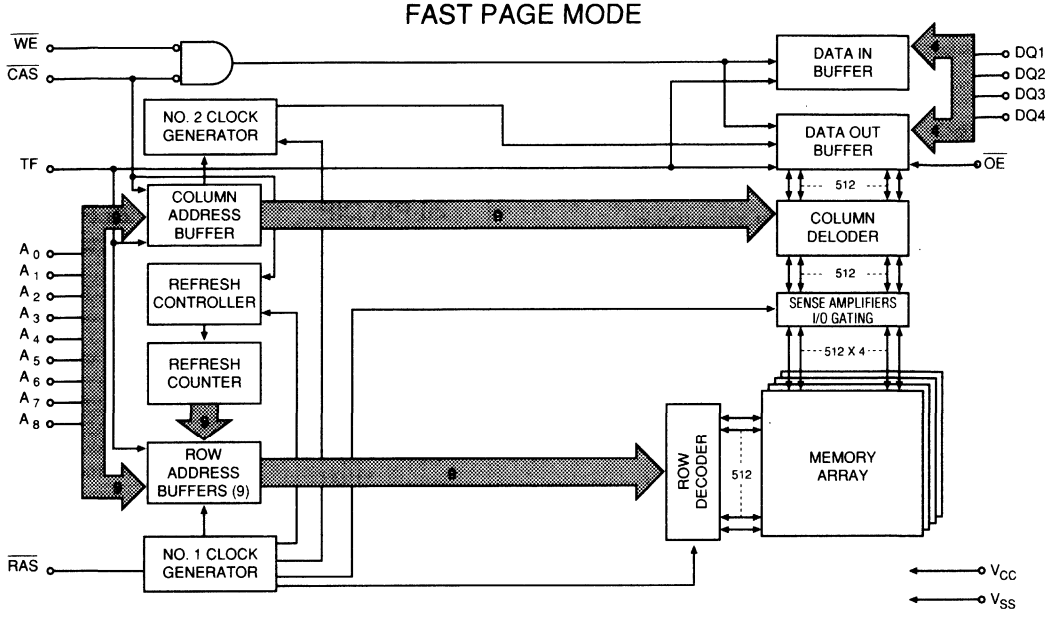
GENERAL DESCRIPTION

The MT4C4265 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The 4 data inputs and 4 data outputs are routed through 4 pins using common I/O and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh will increment refresh counter for automatic $\overline{RAS}$ addressing.

PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



TRUTH TABLE

Function	RAS	CAS	WE	OE	TF	Addresses tR	Addresses tC	
Standby	H	H	H	H	X	X	X	High Impedance
READ	L	L	H	L	X	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	H	X	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	L→H	X	ROW	COL	Valid Data Out, Valid Data In
PAGE-MODE READ	L	H→L→H	H	L	X	ROW	COL	Valid Data Out, Valid Data Out
PAGE-MODE WRITE	L	H→L→H	L	H	X	ROW	COL	Valid Data In, Valid Data In
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	L→H	X	ROW	COL	Valid Data Out, Valid Data In
RAS ONLY REFRESH	L	H	H	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	H	X	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	H	H	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input ($0V \le V_{IN} \le 6.5V$, all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, $0V \le V_{OUT} \le 5.5V$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

		MAX				
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}	70	60	50	mA	3, 4
STANDBY CURRENT (TTL) Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	3	2	2	mA	
$\overline{RAS}$ ONLY REFRESH CURRENT Average power supply current, $\overline{RAS}$ ONLY mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC3}	70	60	50	mA	3
FAST PAGE MODE CURRENT Average power supply current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC4}	50	40	30	mA	3,4
STANDBY CURRENT (CMOS) Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC5}	1	1	1	mA	25
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT Average power supply current, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC6}	70	60	50	mA	3

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	160		190		220		ns	
READ-WRITE cycle time	^tRWC	215		220		295		ns	
FAST PAGE MODE READ or WRITE cycle time	^tPC	45		55		70		ns	
FAST PAGE MODE READ-WRITE cycle time	^tPRWC	100		115		140		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		30	ns	15
Output Enable	^tOE		20		25		30	ns	
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		55		65	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		25		35		ns	
$\overline{RAS}$ precharge time	^tRP	70		80		90		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	35	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	15		15		20		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	25	75	25	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	12		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	17	40	20	50	20	60	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		85		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

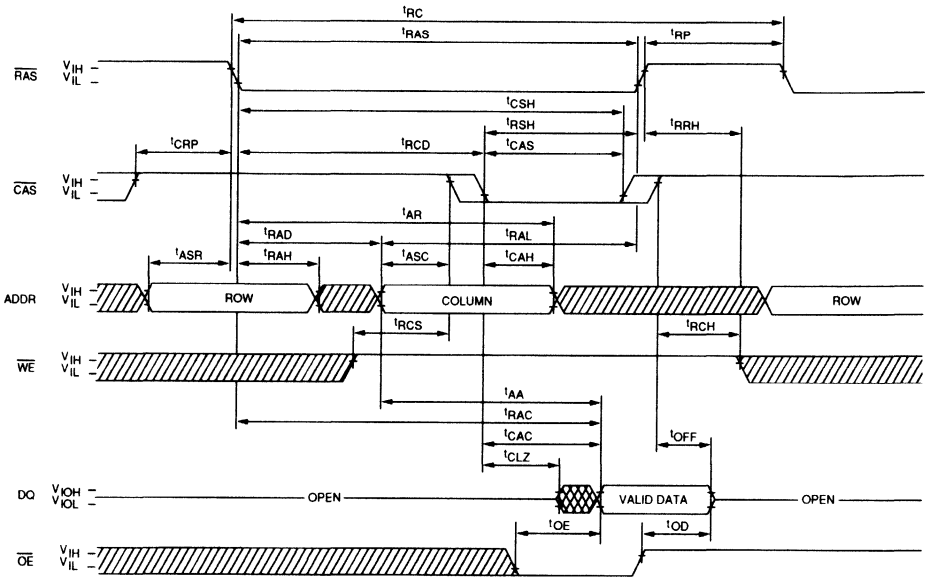
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	35	ns	20
Output Disable	^tOD		20		20		35	ns	
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		85		ns	
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		25		30		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	20		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	110		130		160		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	70		80		100		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	55		65		75		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5

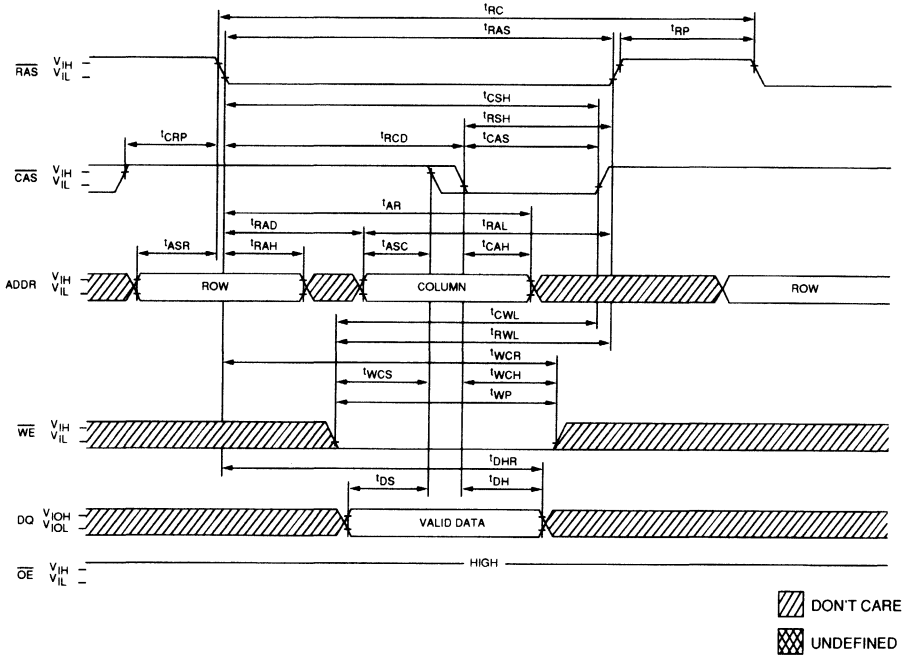
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \ge {}^tRWD$ (min), $^tAWD \ge {}^tAWD$ (min) and $^tCWD \ge {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW a READ-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
25. All other inputs at Vcc -0.2V.

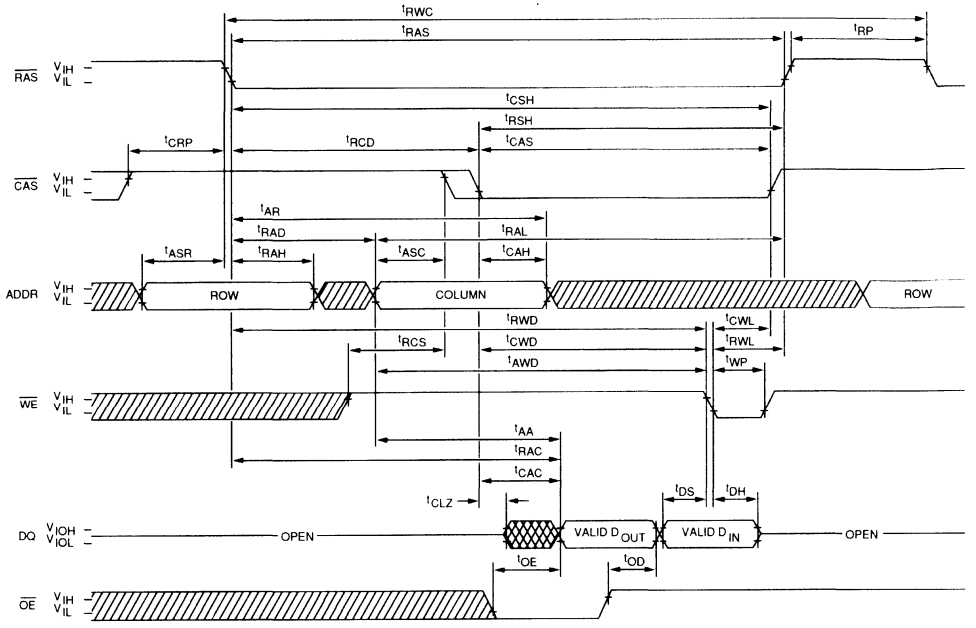
READ CYCLE



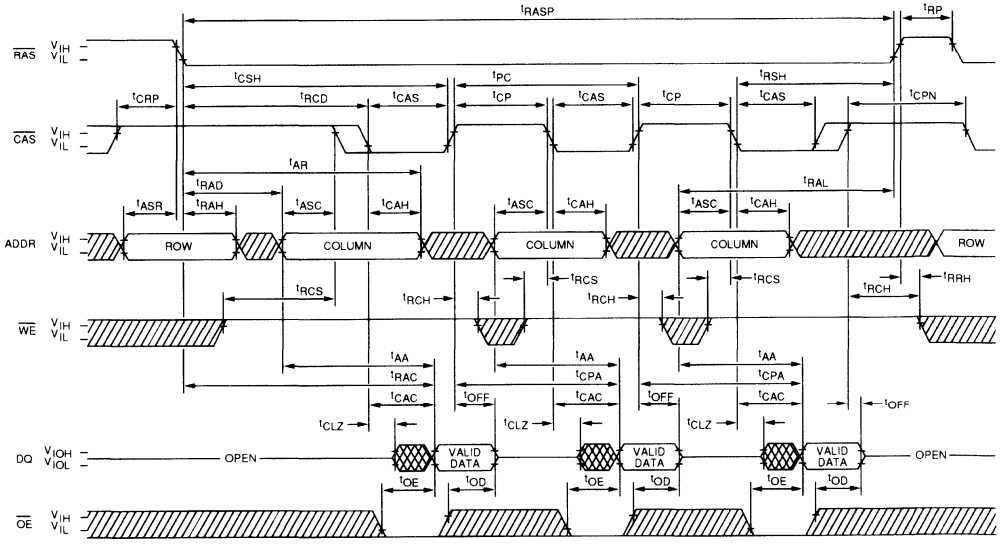
EARLY-WRITE CYCLE



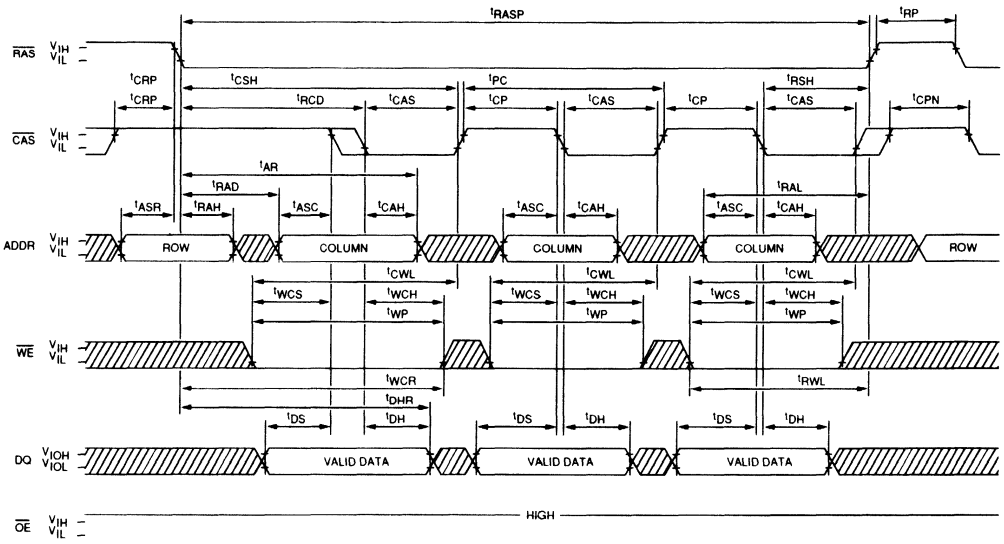
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



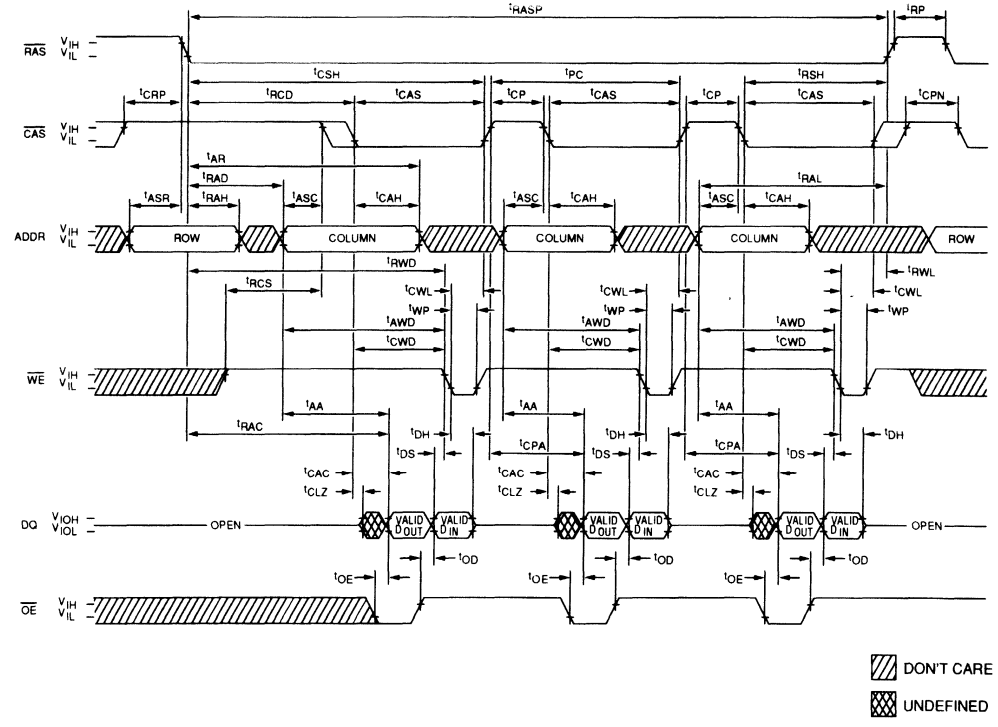
PAGE-MODE READ CYCLE



PAGE-MODE EARLY-WRITE CYCLE

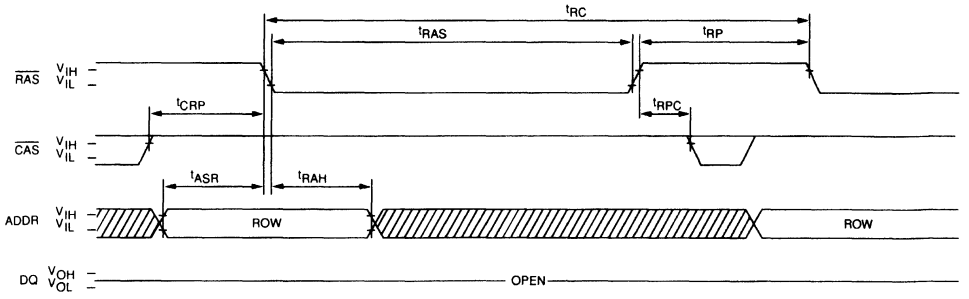


PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



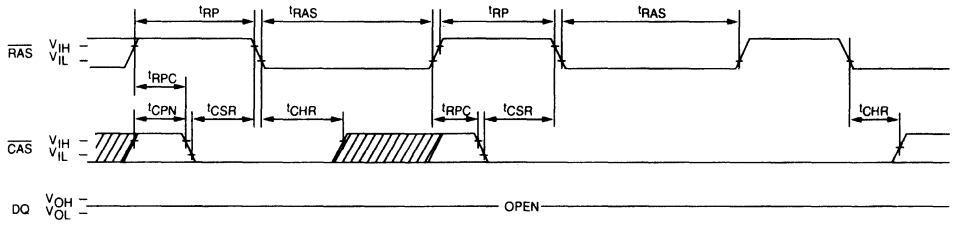
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; $\overline{WE}$ = DON'T CARE.)



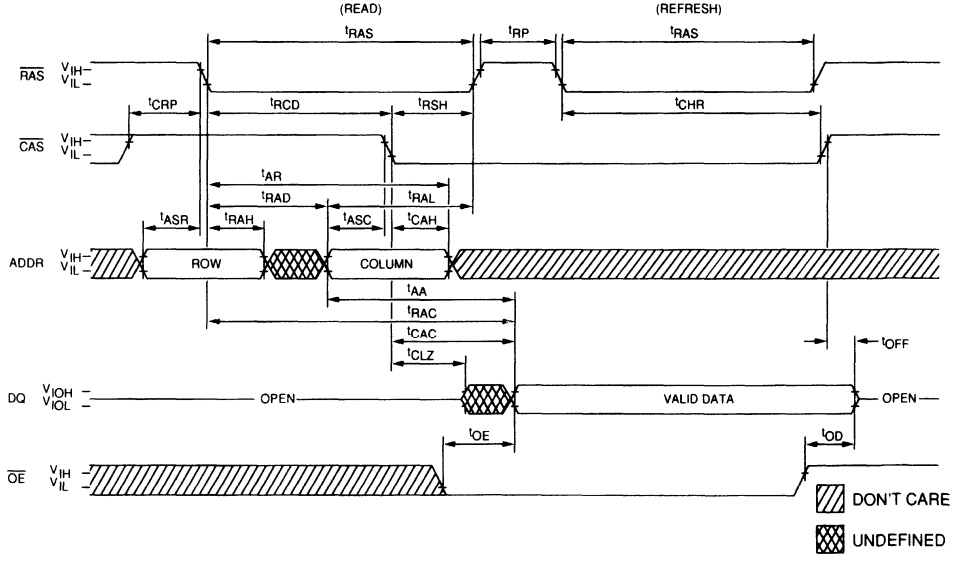
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH, $\overline{OE}$=LOW)[24]



DRAM

256K x 4 DRAM

STATIC COLUMN

FEATURES

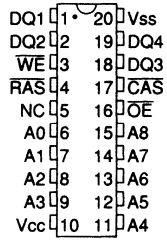
- Industry standard x4 pin-out, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional Static Column access cycle

OPTIONS

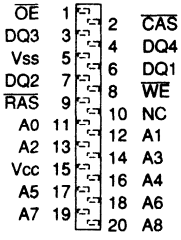
	MARKING
• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

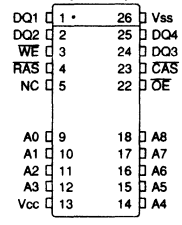
20 Pin DIP (PD, CD)



20 Pin ZIP (ZB)



20 Pin SOJ (DJA)



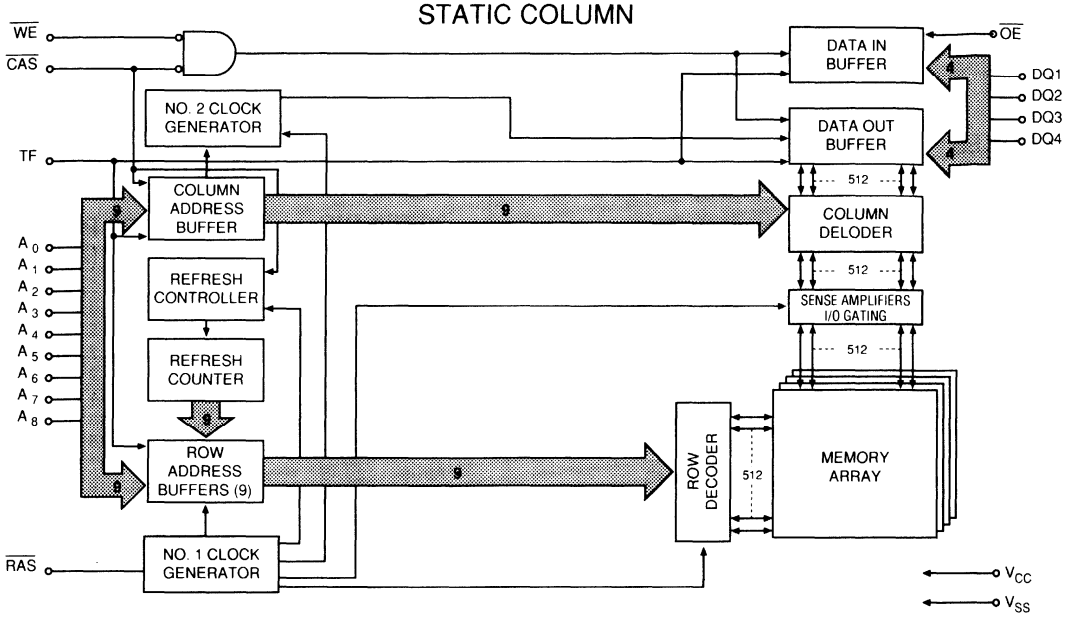
GENERAL DESCRIPTION

The MT4C4258 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data, in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The 4 data inputs and 4 data outputs are routed through 4 pins using common I/O and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh will increment refresh counter for automatic $\overline{RAS}$ addressing.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



TRUTH TABLE

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Standby	H	H	H	H	X	X	X	High Impedance
READ	L	L	H	L	X	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	H	X	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	L→H	X	ROW	COL	Valid Data Out, Valid Data In
STATIC COLUMN READ	L	L	H	L	X	ROW	COL→COL	Valid Data Out, Valid Data Out
STATIC COLUMN WRITE	L	L	L	H	X	ROW	COL→COL	Valid Data In, Valid Data In
STATIC COLUMN READ-WRITE	L	L	H→L→H	L→H	X	ROW	COL→COL	Valid Data Out, Valid Data In
RAS ONLY REFRESH	L	H	H	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	H	X	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	H	H	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MAX -8	MAX -10	MAX -12	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}	70	60	50	mA	3, 4
OPERATING CURRENT: STATIC COLUMN ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}	70	60	50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}	3	2	2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}	1	1	1	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}	70	60	50	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	70	60	50	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	150		180		220		ns	
READ-MODIFY-WRITE cycle time	^tRWC	205		245		255		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		25		30		30	ns	15
Output Enable	^tOE		25		25		25	ns	
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		55		65	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		25		30		ns	
$\overline{RAS}$ precharge time	^tRP	60		70		90		ns	
$\overline{CAS}$ pulse width	^tCAS	25	10,000	30	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	10		15		20		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	55	25	70	15	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		15		10		ns	
Row address set-up time	^tASR	0		0		ns			
Row address hold time	^tRAH	10		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	40	20	50	15	60	ns	18
Column address set-up time	^tASC	0		0		ns			
Column address hold time	^tCAH	15		20		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	95		115		130		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	30	0	25	ns	20
Output Disable	^tOD		20		30		25	ns	
$\overline{WE}$ command set-up time	^tWCS	0		0		ns	21		
Write command hold time	^tWCH	15		20		25		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

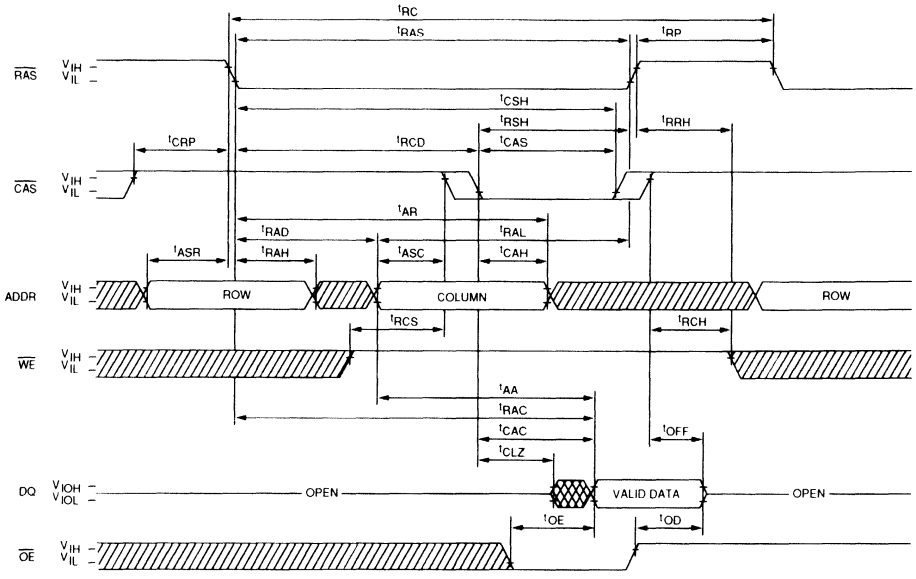
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		80		ns	
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
Write inactive time	^tWI	10		10		10		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	110		135		150		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	70		85		100		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	55		65		80		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5
STATIC COLUMN MODE cycle time	^tSC	45		55		65		ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	80	100,000	100	100,000	120	100,000	ns	
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		10		15		ns	
STATIC COLUMN READ-MODIFY-WRITE cycle time	^tSRMW	110		135		160		ns	
Last write to column address delay time	^tLWAD	20	40	25	45	30	55	ns	
Last write to column address hold time	^tAHLW	75		95		115		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	^tROH	10		20		20		ns	
Output data hold time from column address	^tAOH	5	—	5	—	5	—	ns	
Output data enable from write	^tOW		20		30		35	ns	
$\overline{OE}$ to data delay	^tOED	20		25		30		ns	
$\overline{OE}$ command hold time	^tOEH	20		25		25		ns	
Access time from last write	^tALW		75		95		115	ns	

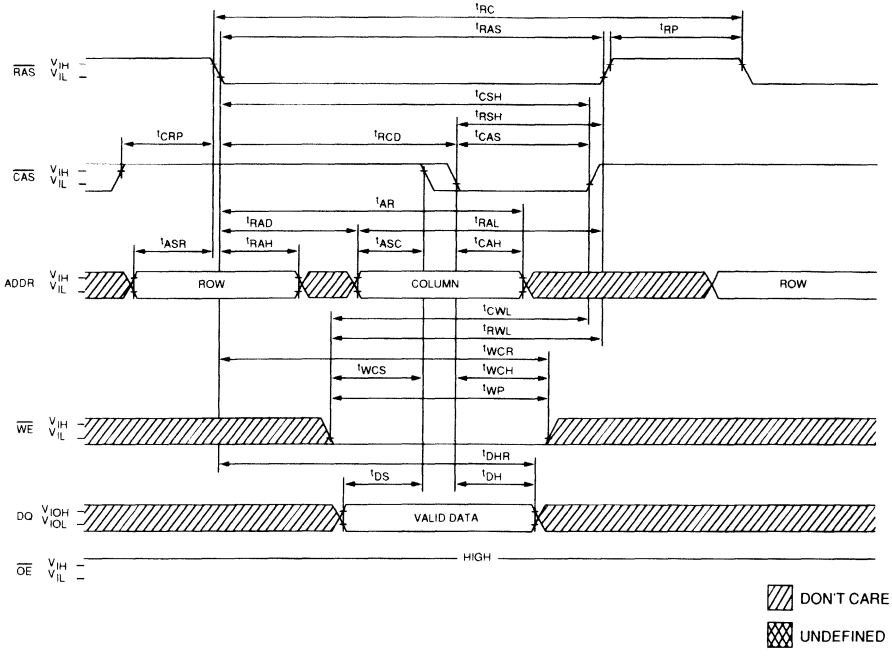
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (min), $^tAWD \ge {}^tAWD$ (min) and $^tCWD \ge {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW a READ-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.

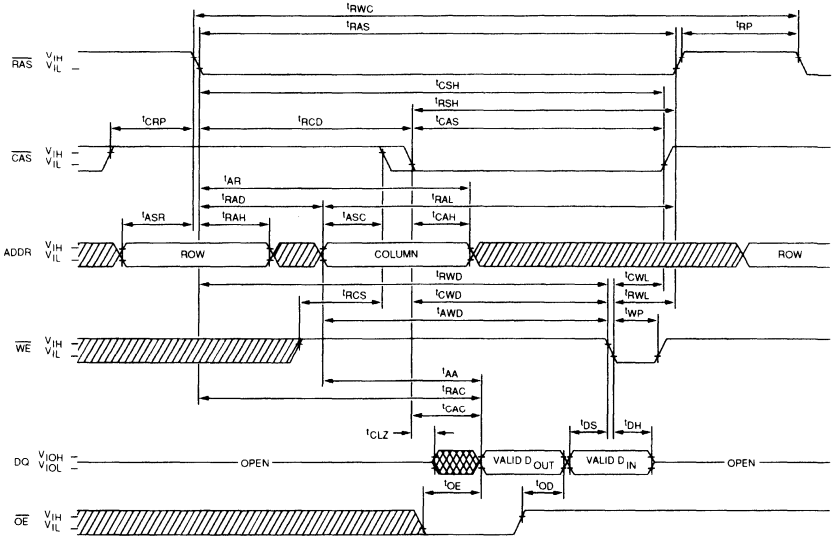
READ CYCLE



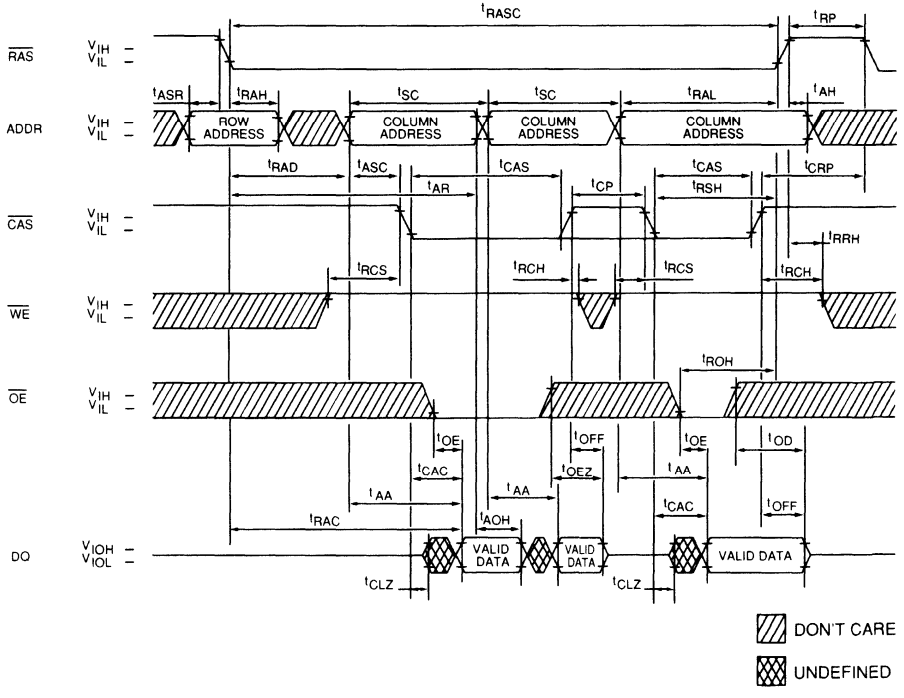
EARLY-WRITE CYCLE



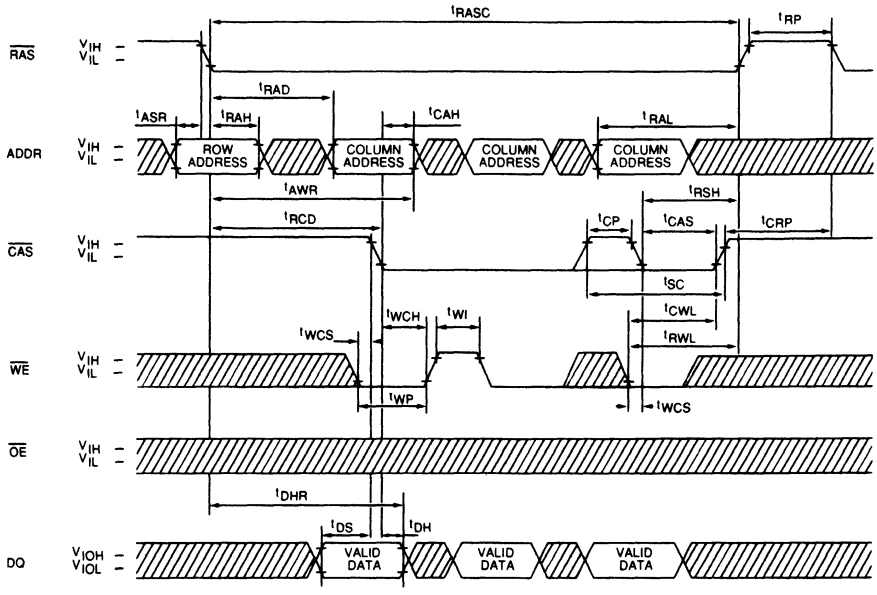
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



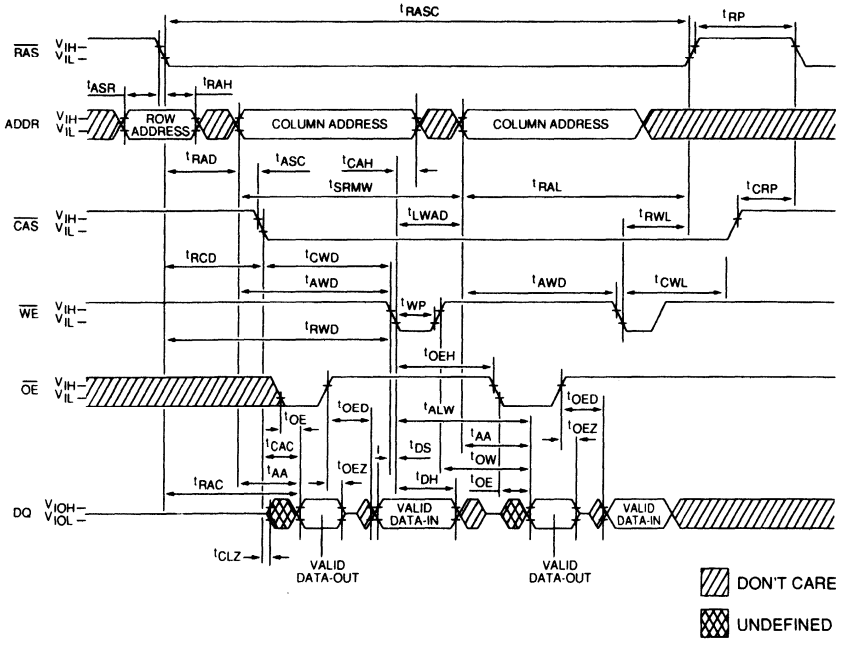
STATIC COLUMN READ CYCLE



STATIC COLUMN EARLY-WRITE CYCLE

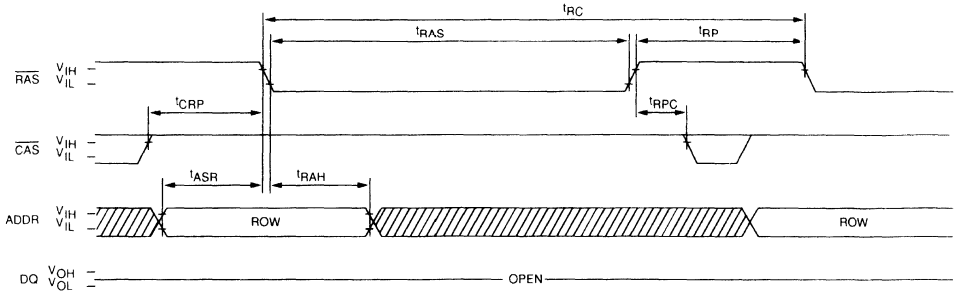


STATIC COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



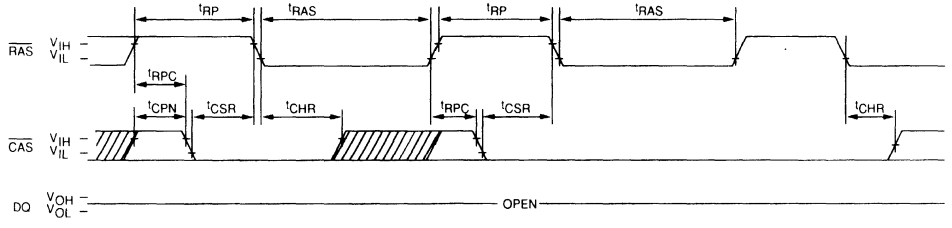
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; $\overline{WE}$ = DON'T CARE.)



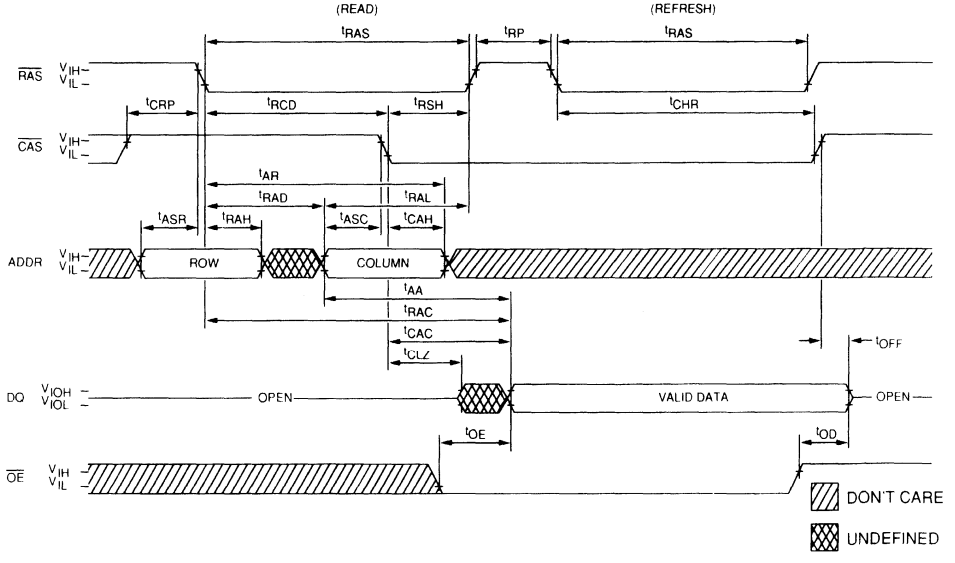
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH, $\overline{OE}$=LOW)[24]



DRAM

1MEG x 1 DRAM

FAST PAGE MODE

FEATURES

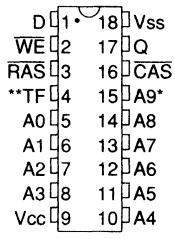
- Industry standard x1 pin-out, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh in 8ms
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional Fast Page Mode access cycle

OPTIONS

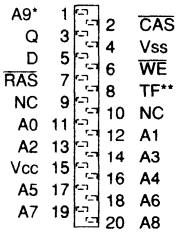
	MARKING
• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

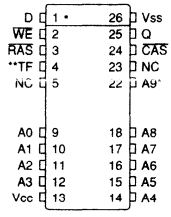
18 Pin DIP (PC, CB)



20 Pin ZIP (ZB)



20 Pin SOJ (DJA)



*Address not used for $\overline{RAS}$ ONLY refresh
**TF = Test Function. V_{IN} must be disconnected or between Vss and Vcc for normal operation.

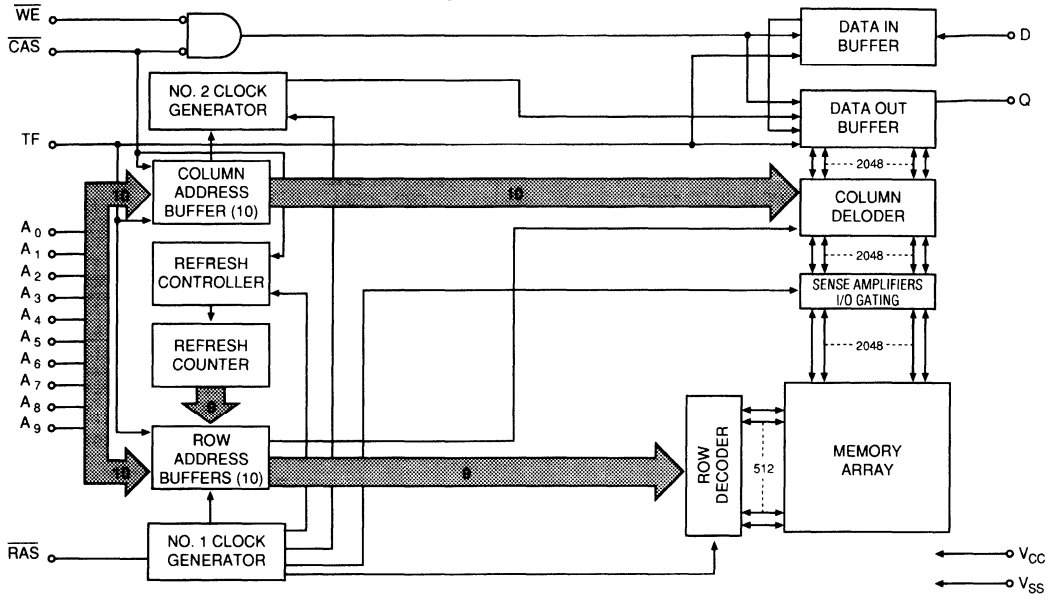
GENERAL DESCRIPTION

The MT4C1024 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin (Q) remains open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh will increment refresh counter for automatic $\overline{RAS}$ addressing.

PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



TRUTH TABLE

Function	RAS	CAS	WE	TF	Addresses tR	Addresses tC	
Standby	H	H	H	X	X	X	High Impedance
READ	L	L	H	X	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	X	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	X	ROW	COL	Valid Data Out, Valid Data In
PAGE-MODE READ	L	H→L→H	H	X	ROW	COL	Valid Data Out, Valid Data Out
PAGE-MODE WRITE	L	H→L→H	L	X	ROW	COL	Valid Data In, Valid Data In
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	X	ROW	COL	Valid Data Out, Valid Data In
RAS ONLY REFRESH	L	H	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	X	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -55°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 600mW
Soldering Temperature (soldering 10 sec) ..... 260°C
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA) Output Low voltage (I_{OUT} = 4.2mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

		MAX				
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}	70	60	50	mA	3, 4
STANDBY CURRENT (TTL) Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	2	2	2	mA	
$\overline{RAS}$ ONLY REFRESH CURRENT Average power supply current, $\overline{RAS}$ ONLYmode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC3}	70	60	50	mA	3
FAST PAGE MODE CURRENT Average power supply current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC4}	50	40	30	mA	3,4
STANDBY CURRENT (CMOS) Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC5}	1	1	1	mA	24
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT Average power supply current, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC6}	70	60	50	mA	3

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_9, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	160		190		220		ns	
READ-WRITE cycle time	t_{RWC}	185		220		255		ns	
FAST PAGE-MODE READ or WRITE cycle time	t_{PC}	45		55		70		ns	
FAST PAGE-MODE READ-WRITE cycle time	t_{PRWC}	70		85		105		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		25		30	ns	15
Access time from column address	t_{AA}		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		55		65	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	t_{RASP}	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{CAS}$ precharge time	t_{CPN}	15		15		20		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	t_{CP}	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	60	25	75	25	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		15		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	20	60	ns	18
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	60		70		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		50		60		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	35	ns	20
$\overline{WE}$ command set-up time	t_{WCS}	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

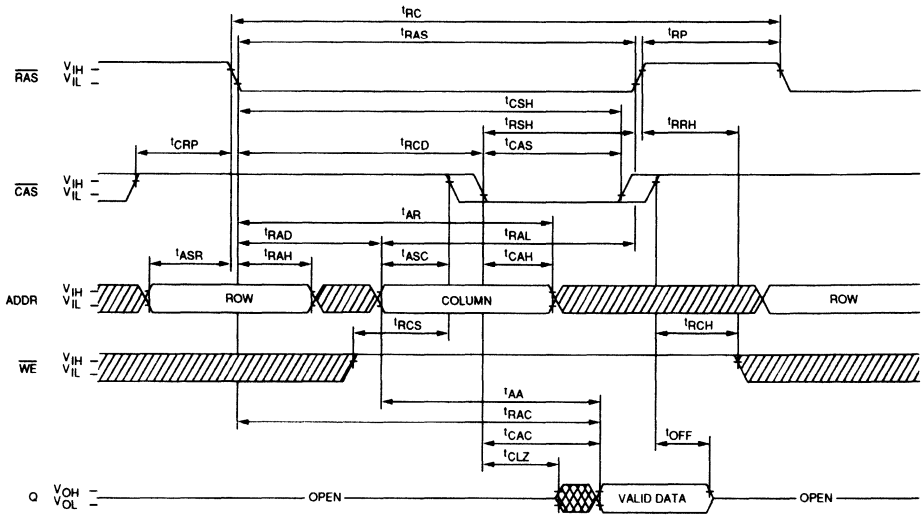
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		85		ns	
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	20		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		100		120		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		25		30		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5

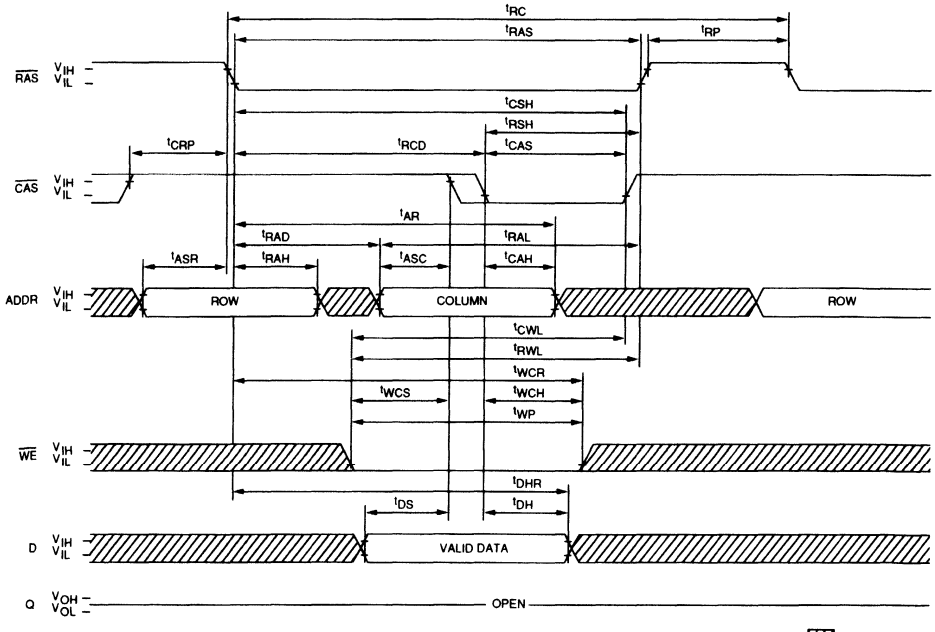
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \ge {}^tRWD$ (min), $^tAWD \ge {}^tAWD$ (min) and $^tCWD \ge {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.
24. All other inputs equal Vcc -0.2V.

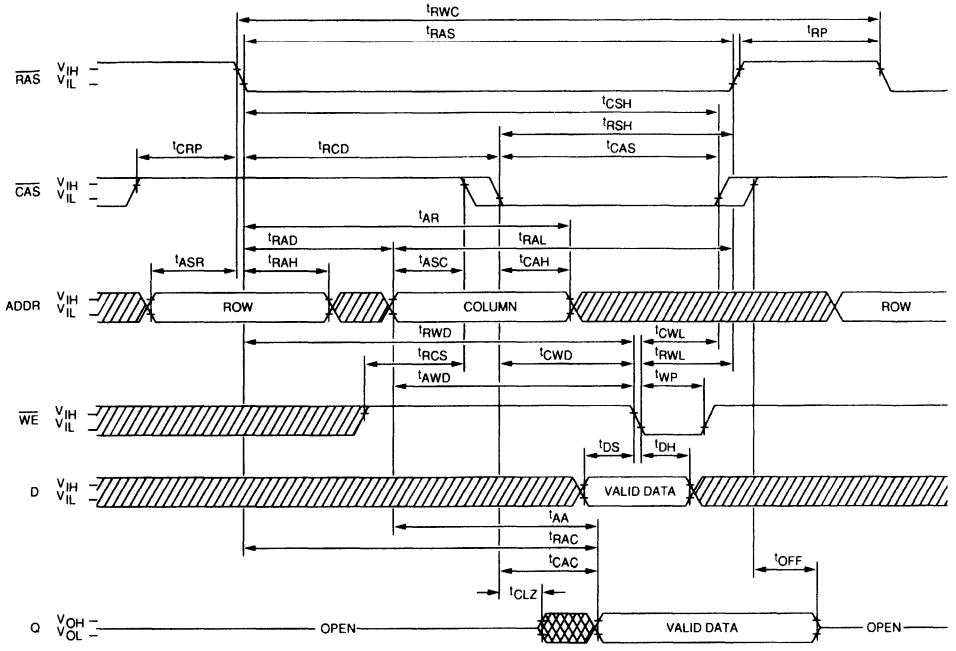
READ CYCLE



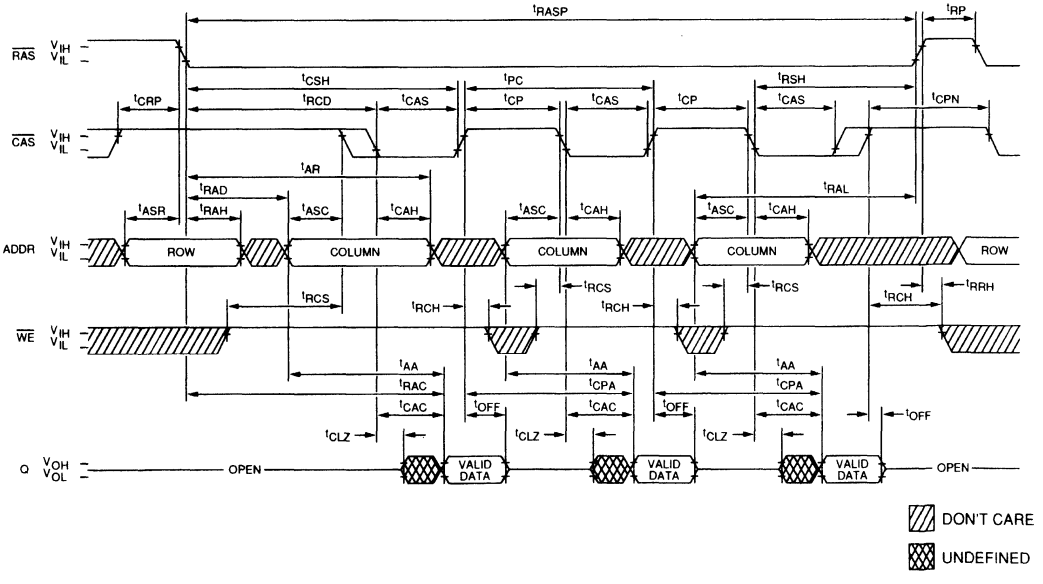
EARLY-WRITE CYCLE



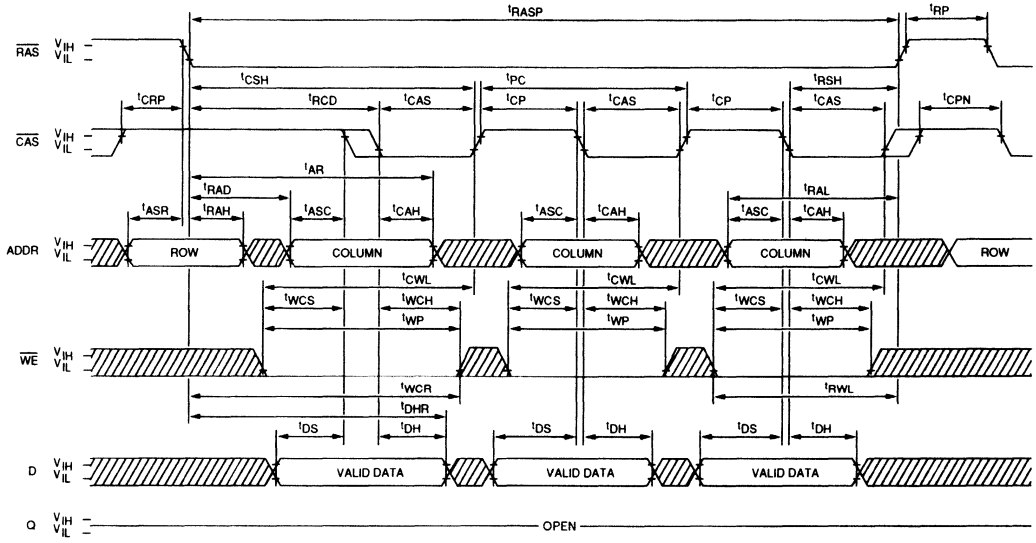
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



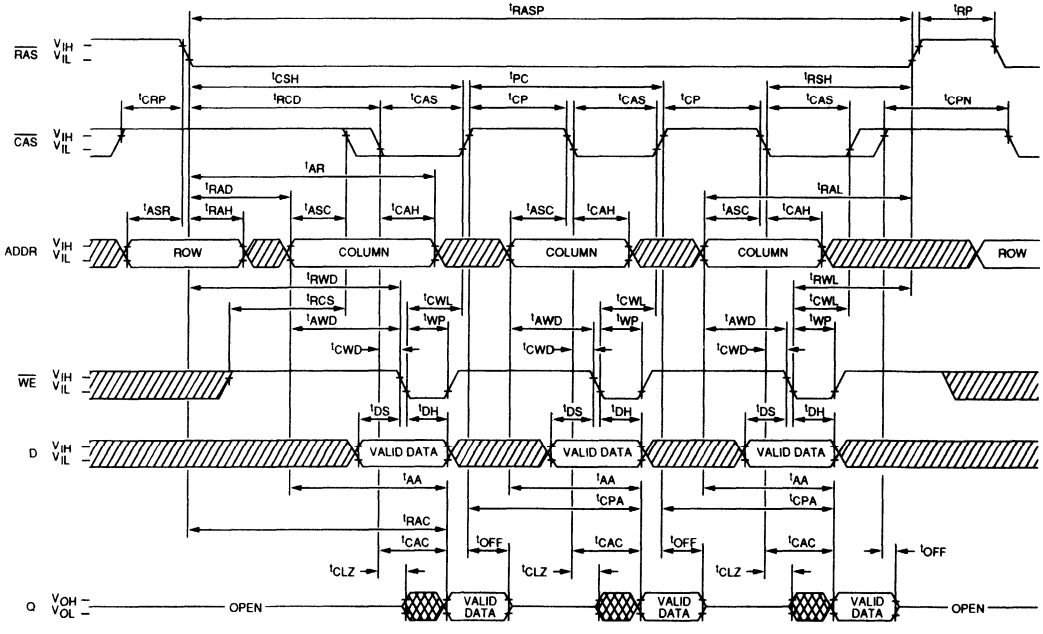
PAGE-MODE READ CYCLE



PAGE-MODE EARLY-WRITE CYCLE

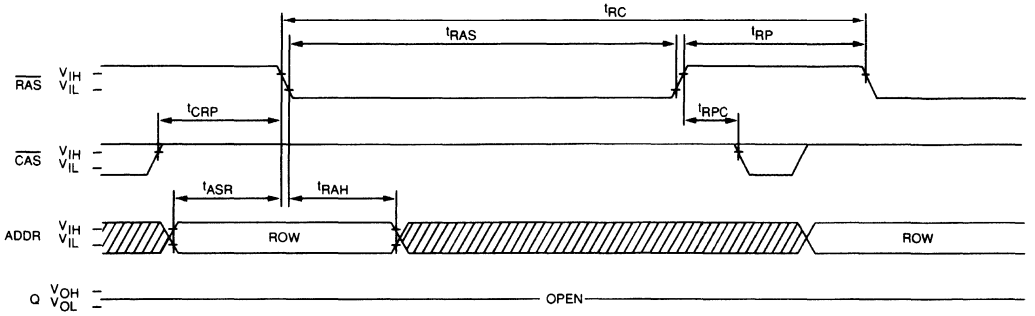


PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



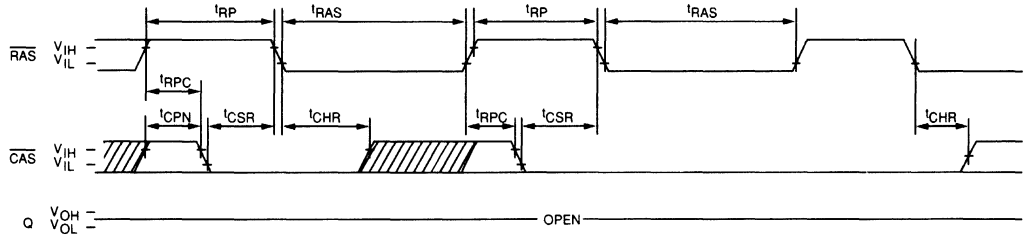
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



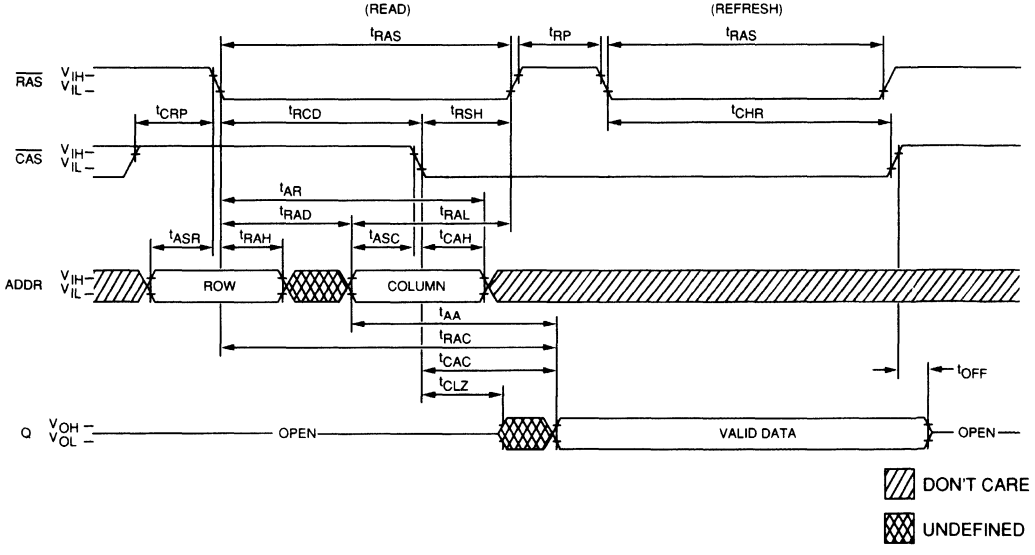
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[23]



DRAM

1MEG x 1 DRAM

NIBBLE MODE

FEATURES

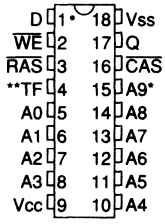
- Industry standard x1 pin-out, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional Nibble Mode access cycle

OPTIONS

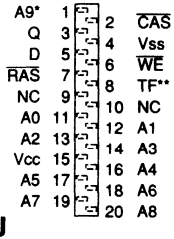
	MARKING
• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

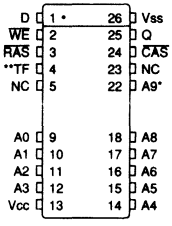
18 Pin DIP (PC, CB)



20 Pin ZIP (ZB)



20 Pin SOJ (DJA)



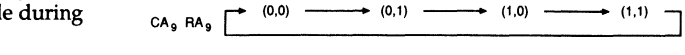
*Address not used for $\overline{RAS}$ ONLY refresh
**TF = Test Function, V_{IN} must be disconnected or between Vss and Vcc for normal operation.

GENERAL DESCRIPTION

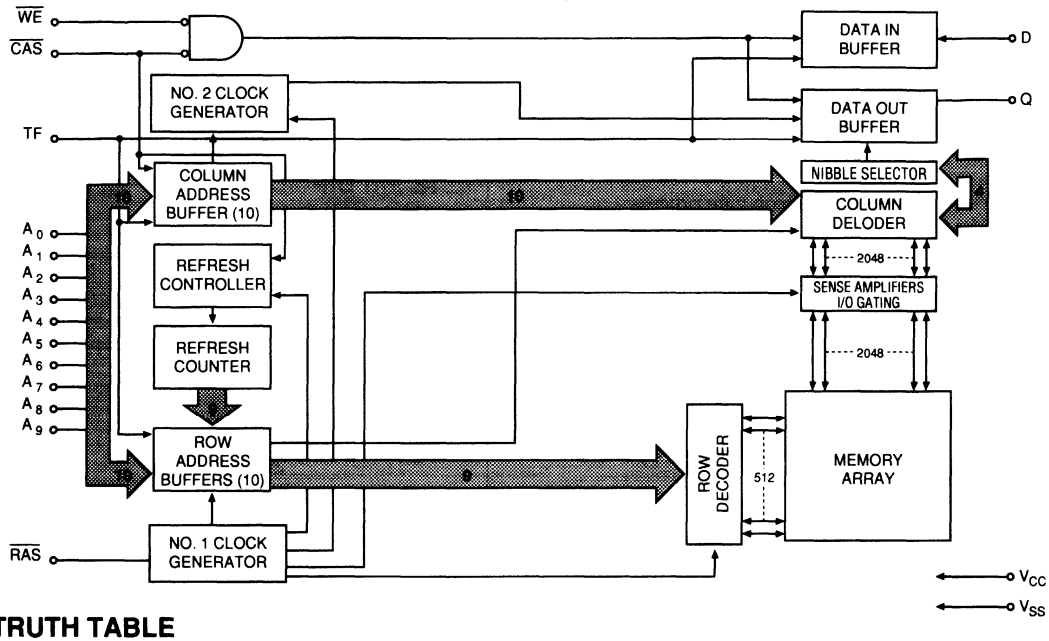
The MT4C1025 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh will increment refresh counter for automatic $\overline{RAS}$ addressing.

NIBBLE MODE operation allows faster sequential serial data operations (READ, WRITE or READ-MODIFY-WRITE) up to 4 bits. The first of 4 bits is accessed in the usual manner with $\overline{CAS}$ address A9 (nibble MSB) and $\overline{RAS}$ address A9 (nibble LSB) selecting one of 4 bits within a nibble for initial access. By holding $\overline{RAS}$ LOW, $\overline{CAS}$ can be toggled incrementing the nibble address field in modulo 4 fashion with wrap around (see below).



FUNCTIONAL BLOCK DIAGRAM
NIBBLE MODE



TRUTH TABLE

Function	RAS	CAS	WE	TF	Addresses tR	Addresses tC	
Standby	H	H	H	X	X	X	High Impedance
READ	L	L	H	X	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	X	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	X	ROW	COL	Valid Data Out, Valid Data In
NIBBLE READ	L	H→L→H	H	X	ROW	COL	Valid Data Out, Valid Data Out
NIBBLE WRITE	L	H→L→H	L	X	ROW	COL	Valid Data In, Valid Data In
NIBBLE READ-WRITE	L	H→L→H	H→L→H	X	ROW	COL	Valid Data Out, Valid Data In
RAS ONLY REFRESH	L	H	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	X	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA) Output Low voltage (I_{OUT} = 4.2mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MAX -8	MAX -10	MAX -12	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}	70	60	50	mA	3, 4
OPERATING CURRENT: NIBBLE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}	70	60	50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}	3	2	2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}	1	1	1	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}	70	60	50	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	70	60	50	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	150		180		220		ns	
READ-MODIFY-WRITE cycle time	t_{RWC}	175		210		255		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		25		30	ns	15
Access time from column address	t_{AA}		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		55		65	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{RAS}$ precharge time	t_{RP}	60		80		90		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		20		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	60	10	75	15	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		10		15		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		20		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	40	20	50	15	60	ns	18
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	60		75		110		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		50		60		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	25	ns	20
$\overline{WE}$ command set-up time	t_{WCS}	0		0		0		ns	21
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	t_{WCR}	60		75		80		ns	
Write command pulse width	t_{WP}	15		20		25		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

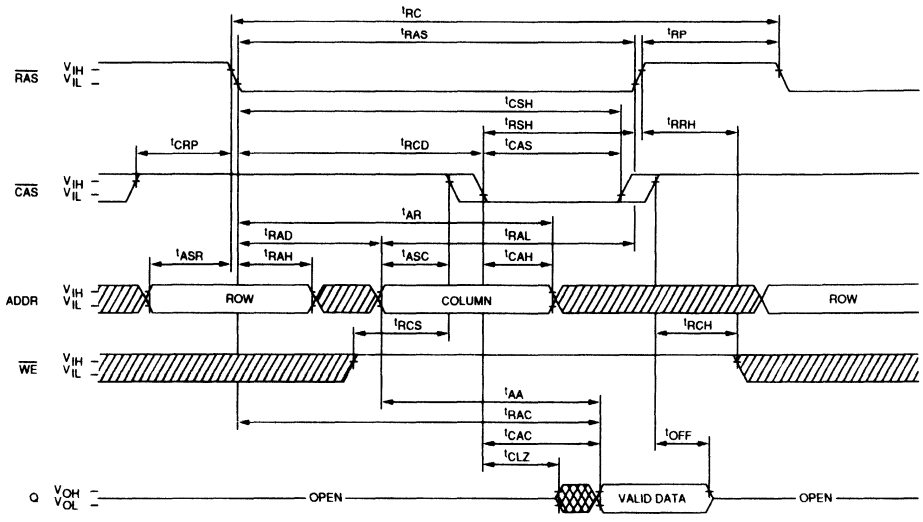
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		110		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		100		120		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		25		35		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5
$\overline{RAS}$ pulse width (NIBBLE MODE)	^tRASN	80	100,000	100	100,000	120	100,000	ns	
$\overline{CAS}$ precharge time (NIBBLE MODE)	^tNCP	10		10		15		ns	
NIBBLE MODE cycle time	^tNC	40		45		55		ns	
NIBBLE MODE READ-MODIFY-WRITE cycle time	^tNRWC	65		75		85		ns	
NIBBLE MODE access time	^tNCAC		20		20		35	ns	15
NIBBLE MODE pulse width	^tNCAS	20		25		35		ns	
NIBBLE MODE $\overline{CAS}$ precharge time	^tNCP	10		10		10		ns	
NIBBLE MODE $\overline{RAS}$ hold time	^tNRSH	20		25		30		ns	
NIBBLE MODE $\overline{CAS}$ to $\overline{WE}$ delay time	^tNCWD	20		25		35		ns	
NIBBLE MODE $\overline{WE}$ command to $\overline{RAS}$ lead time	^tNRWL	20		25		30		ns	
NIBBLE MODE $\overline{WE}$ command to $\overline{CAS}$ lead time	^tNCWL	20		25		30		ns	

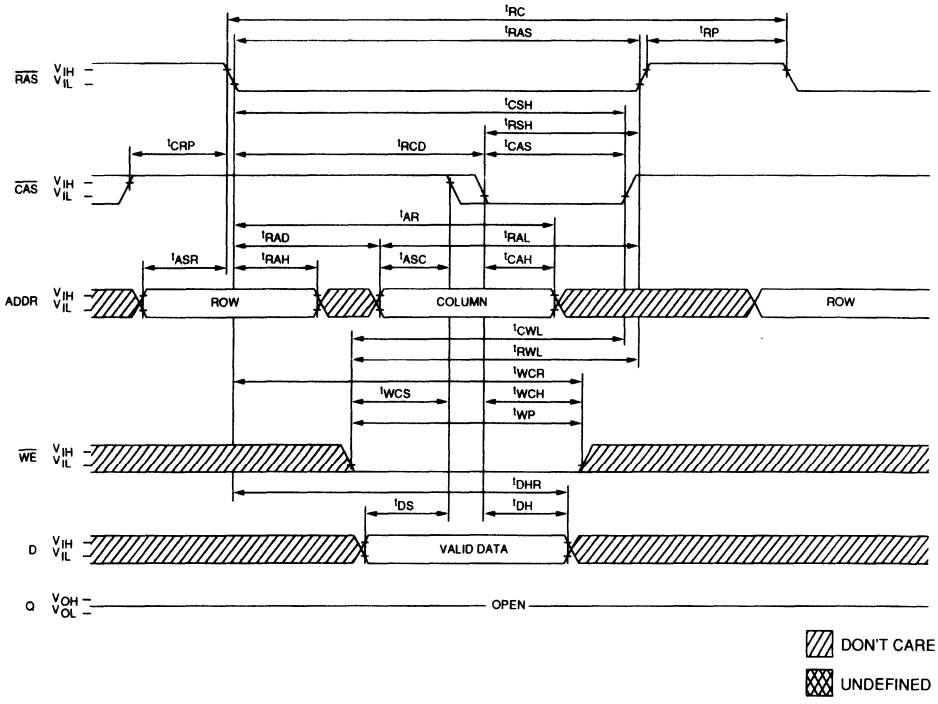
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (min), $^tAWD \geq {}^tAWD$ (min) and $^tCWD \geq {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

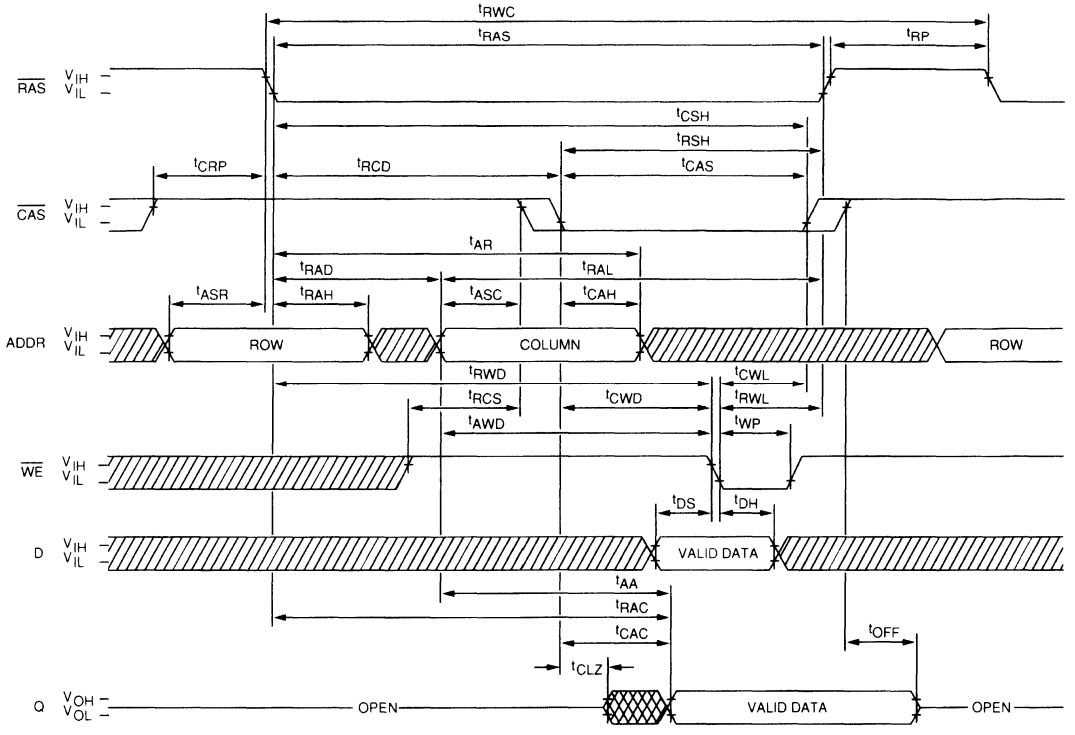
READ CYCLE



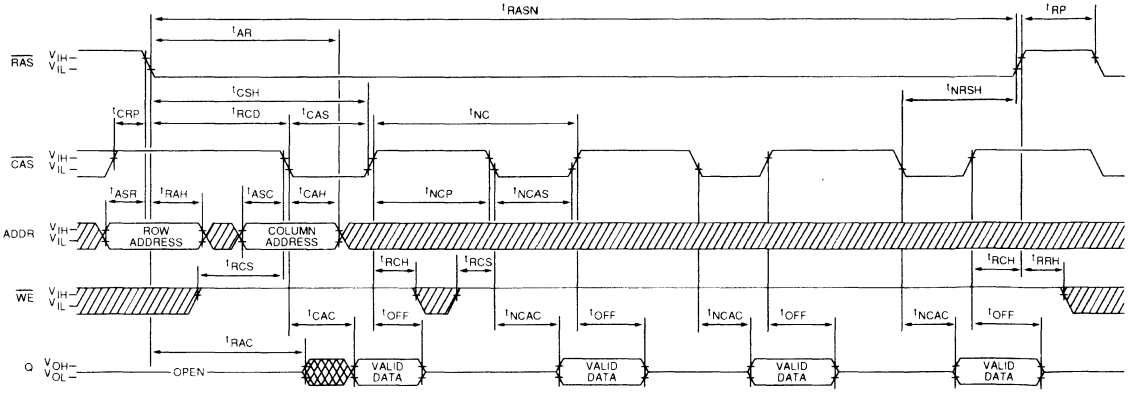
EARLY-WRITE CYCLE



READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



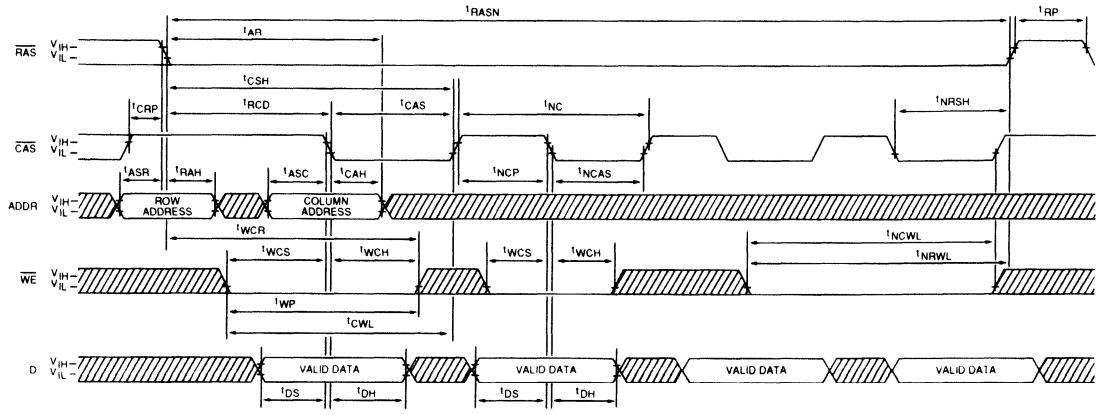
NIBBLE MODE READ CYCLE



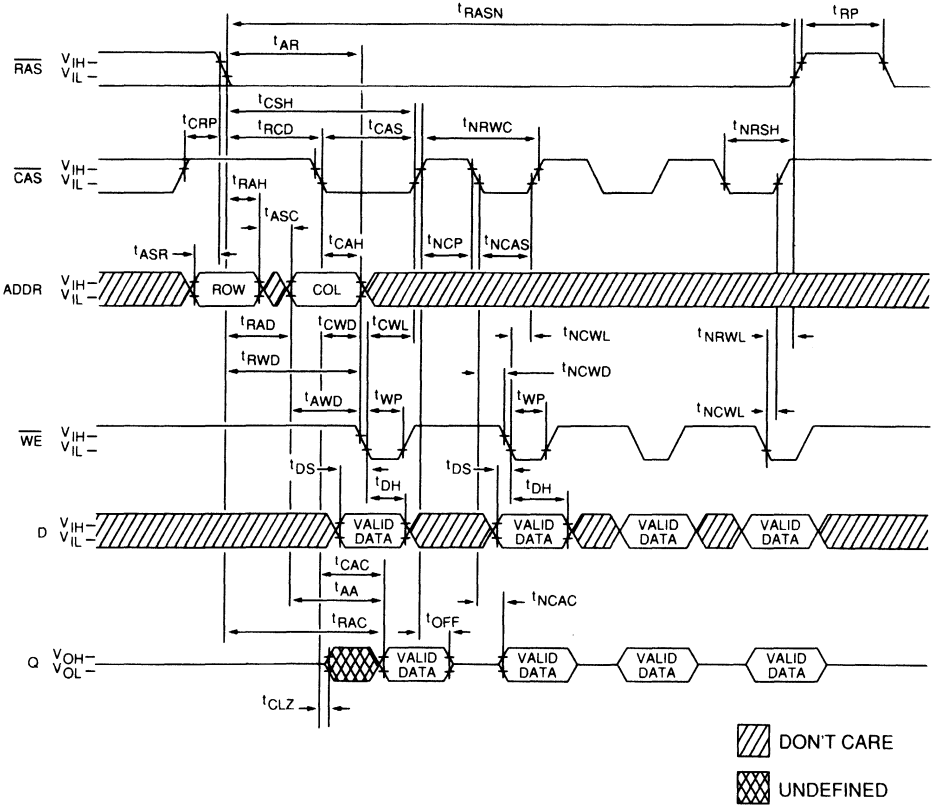
DON'T CARE

UNDEFINED

NIBBLE MODE EARLY-WRITE CYCLE

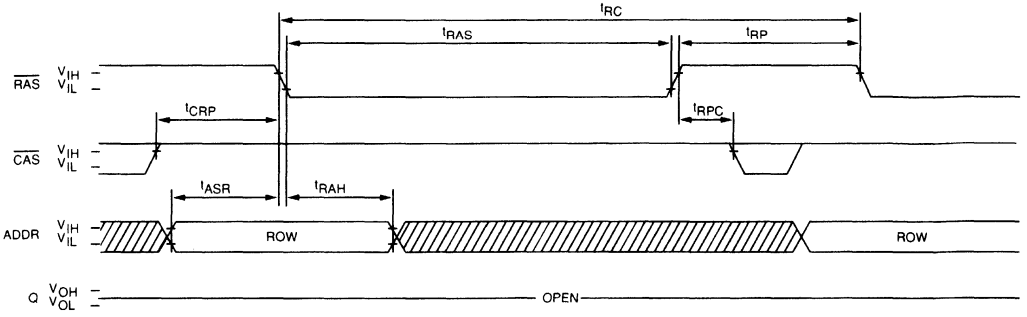


NIBBLE MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



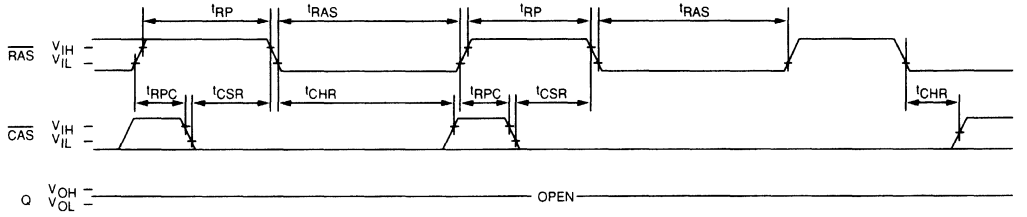
$\overline{RAS}$ ONLY REFRESH CYCLE

($ADDR = A_0 - A_8$; A_9 and $\overline{WE}$ = DON'T CARE.)



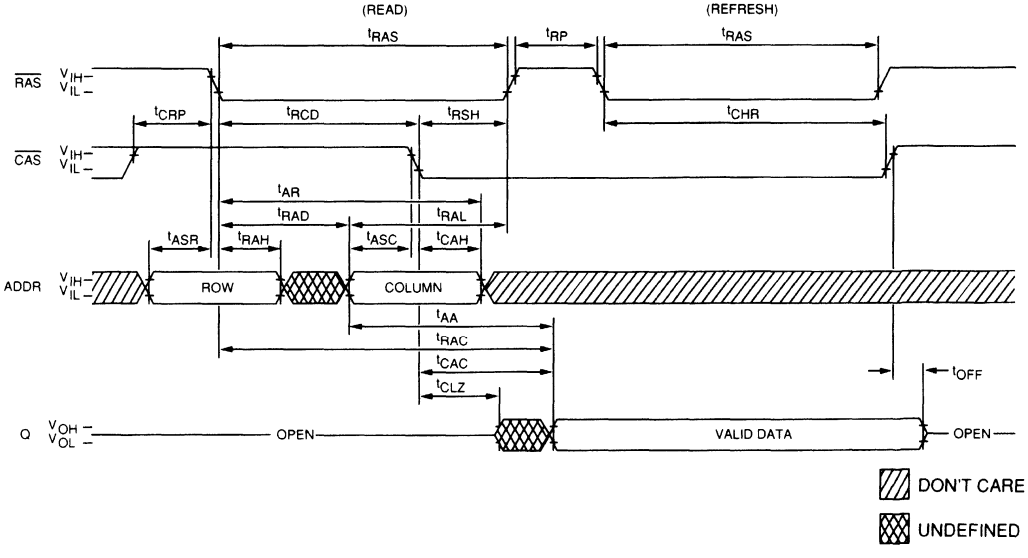
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

($A_0 - A_9$ and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[23]



DRAM

1MEG x 1 DRAM

STATIC COLUMN

FEATURES

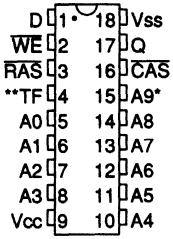
- Industry standard x1 pin-out, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional Static Column access cycle

OPTIONS

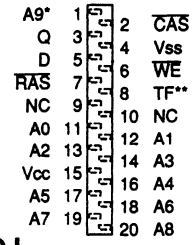
	MARKING
• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

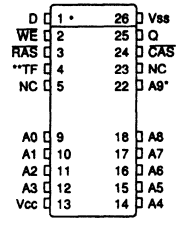
18 Pin DIP (PC, CB)



20 Pin ZIP (ZB)



20 Pin SOJ (DJA)



*Address not used for $\overline{RAS}$ ONLY refresh
**TF = Test Function, V_{IN} must be disconnected or between Vss and Vcc for normal operation.

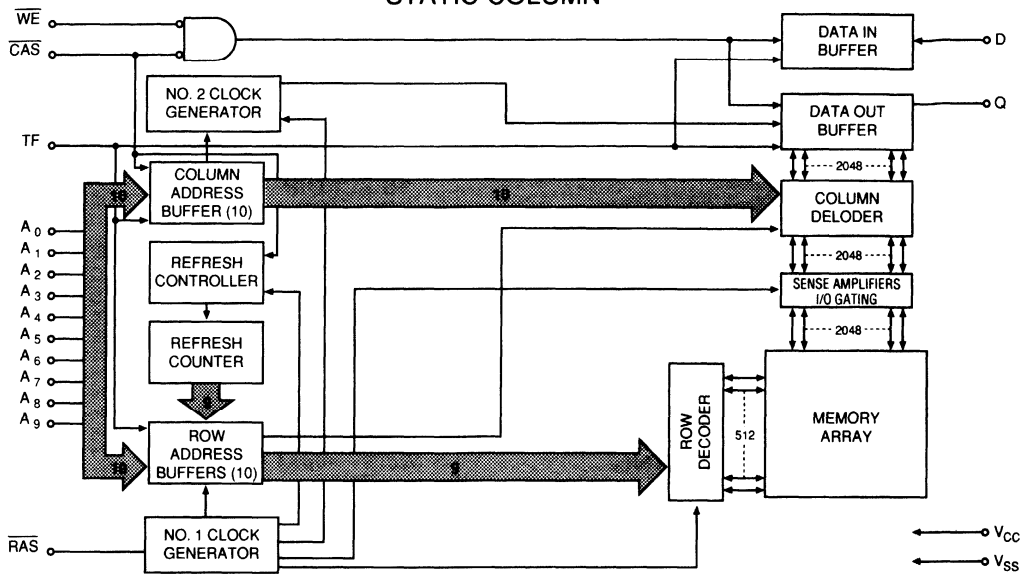
GENERAL DESCRIPTION

The MT4C1026 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh will increment refresh counter for automatic $\overline{RAS}$ addressing.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



TRUTH TABLE

Function	RAS	CAS	WE	TF	Addresses tR	Addresses tC	
Standby	H	H	H	X	X	X	High Impedance
READ	L	L	H	X	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	X	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	X	ROW	COL	Valid Data Out, Valid Data In
STATIC COLUMN READ	L	L	H	X	ROW	COL→COL	Valid Data Out, Valid Data Out
STATIC COLUMN WRITE	L	L	L	X	ROW	COL→COL	Valid Data In, Valid Data Out
STATIC COLUMN READ-WRITE	L	L	H→L→H	X	ROW	COL→COL	Valid Data Out, Valid Data In
RAS ONLY REFRESH	L	H	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	X	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

		MAX				
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}	70	60	50	mA	3, 4
OPERATING CURRENT: STATIC COLUMN ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}	70	60	50	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}	3	2	2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}	1	1	1	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}	70	60	50	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}	70	60	50	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		180		220	ns		
READ-MODIFY-WRITE cycle time	^tRWC	175		210		255		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		30	ns	15
Access time from column address	^tAA		40		50		60	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		30		ns	
$\overline{RAS}$ precharge time	^tRP	60		70		90		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	10		15		20		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	25	75	15	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	40	20	50	20	60	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	90		115		115		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	25	ns	20
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		80		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

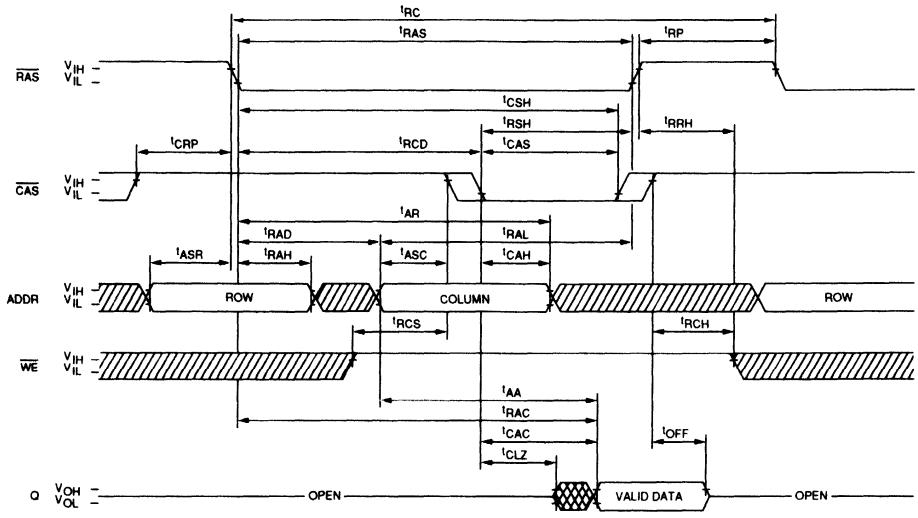
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
$\overline{WE}$ inactive time	^tWI	10		10		10		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		80		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		100		110		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		25		30		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	80	100,000	100	100,000	120	100,000	ns	
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		10		15		ns	
STATIC COLUMN MODE cycle time	^tSC	45		55		65		ns	
STATIC COLUMN READ-MODIFY-WRITE cycle time	^tSRMW	80		100		160		ns	
Last Write to column address delay time	^tLWAD	20	35	25	45	30	55	ns	
Last Write to column address hold time	^tAHLW	75		95		115		ns	
Output data hold time from column address	^tAOH	5		5		5		ns	
Output data enable from Write	^tOW		20		25		25	ns	

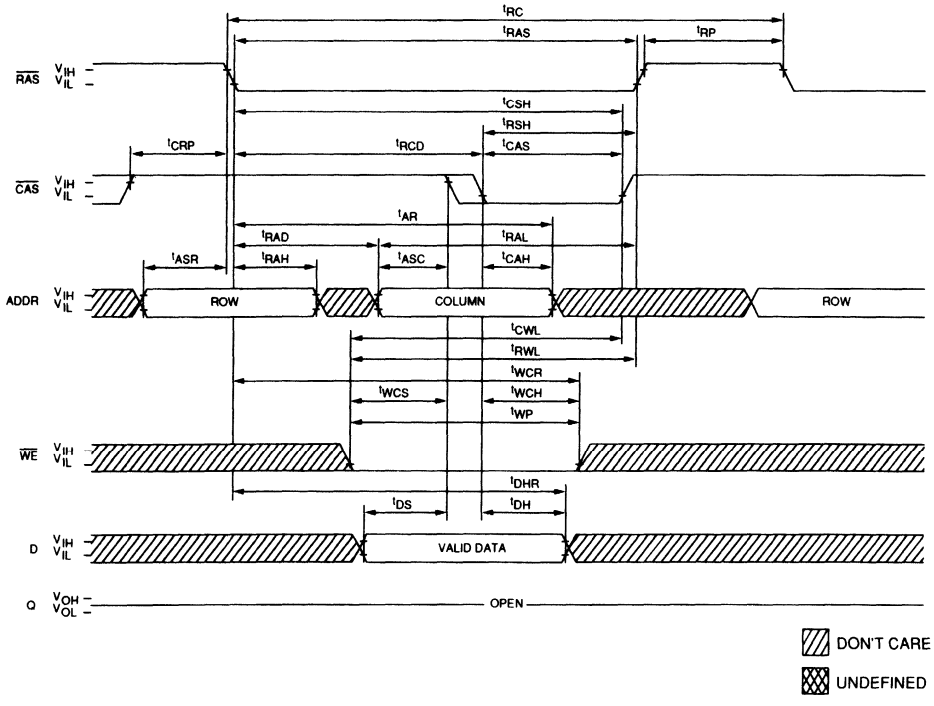
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \ge {}^tRWD$ (min), $^tAWD \ge {}^tAWD$ (min) and $^tCWD \ge {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

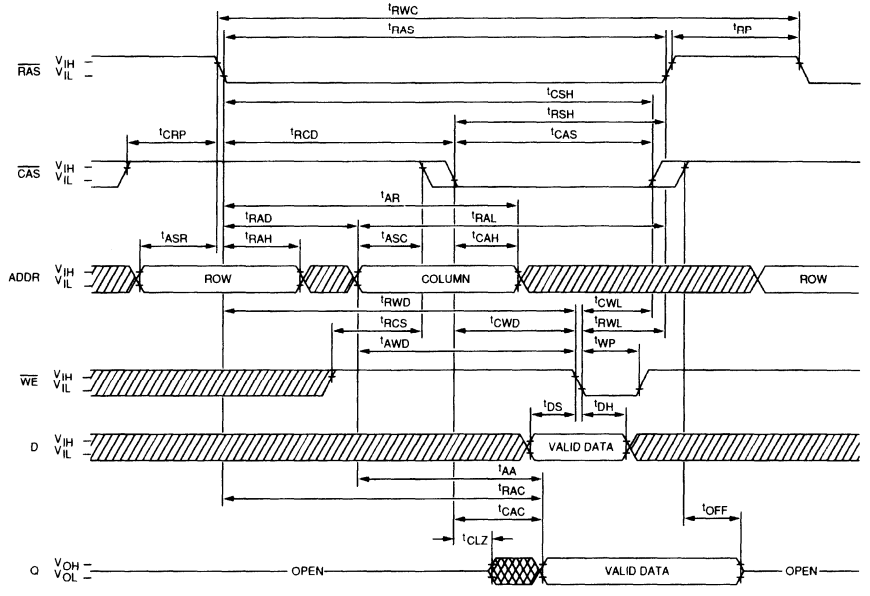
READ CYCLE



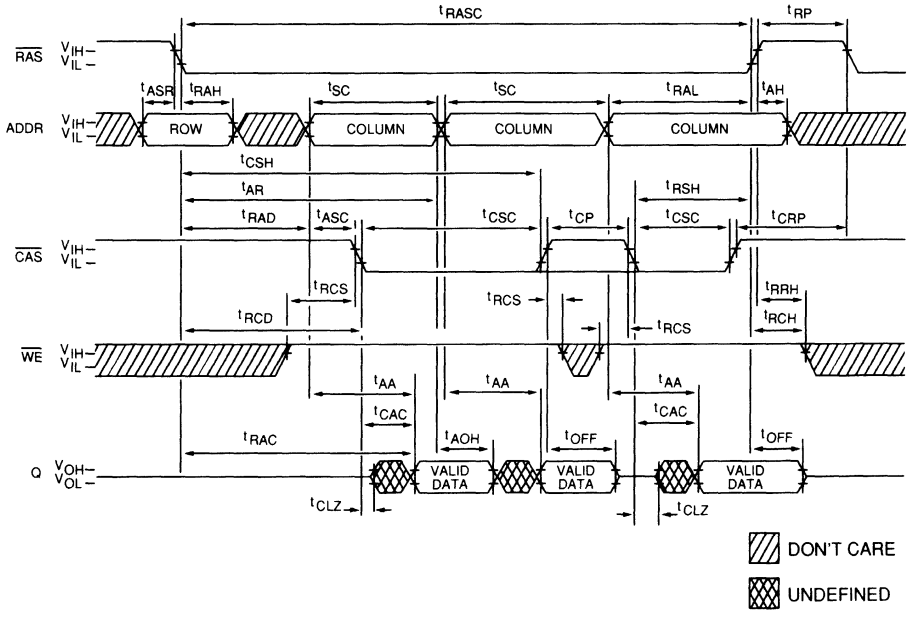
EARLY-WRITE CYCLE



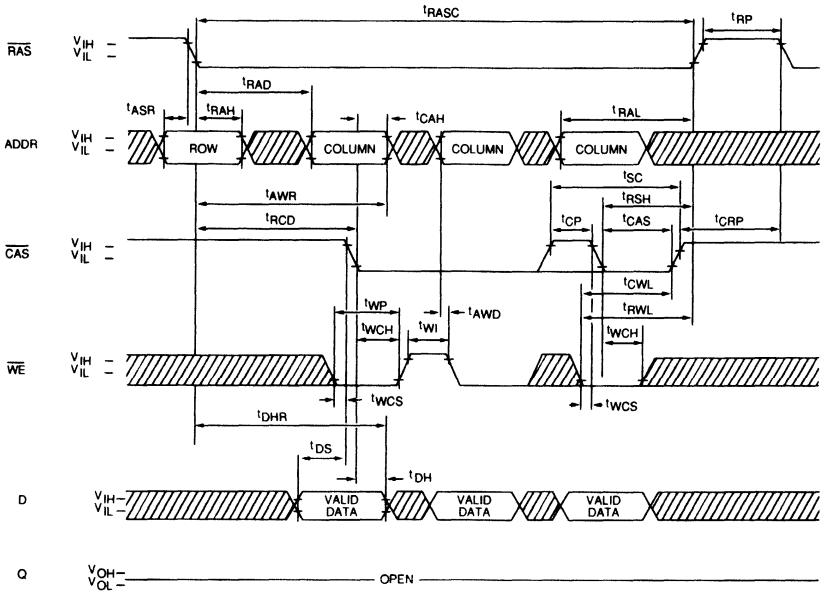
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



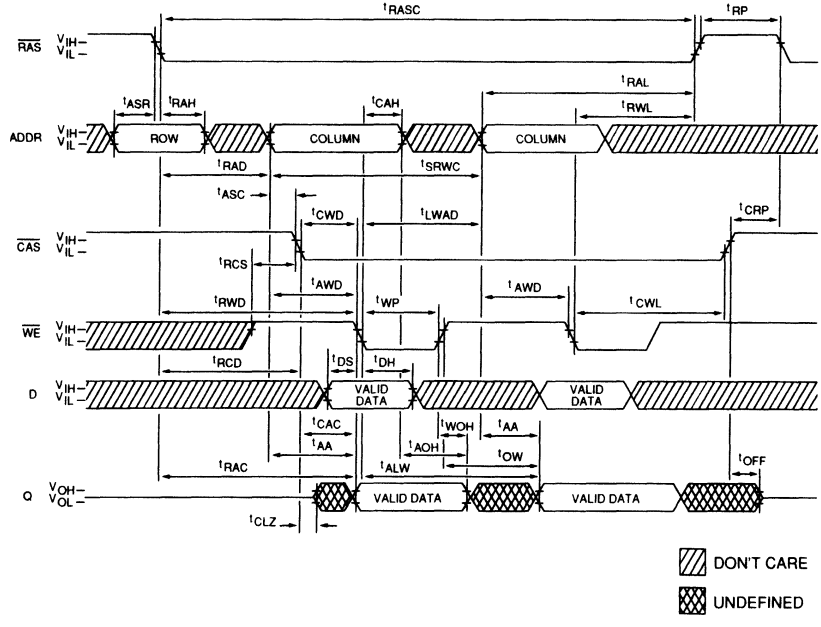
STATIC COLUMN READ CYCLE



STATIC COLUMN EARLY-WRITE CYCLE

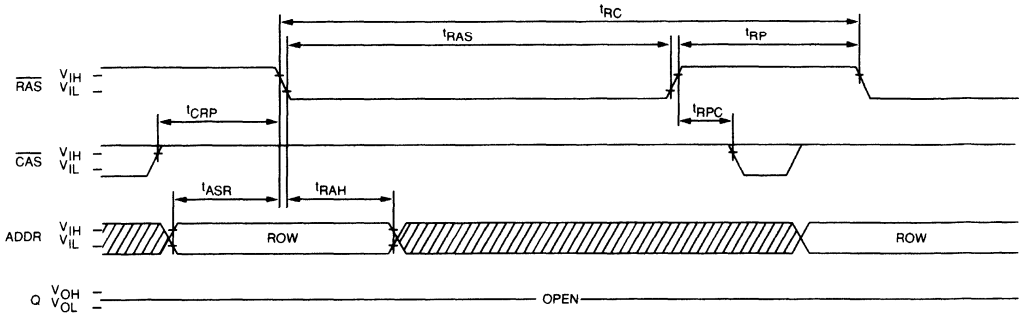


STATIC COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



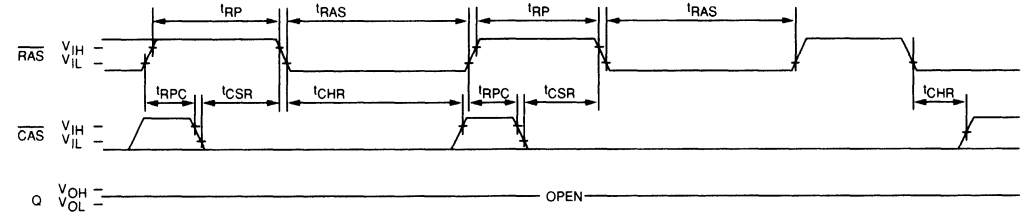
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



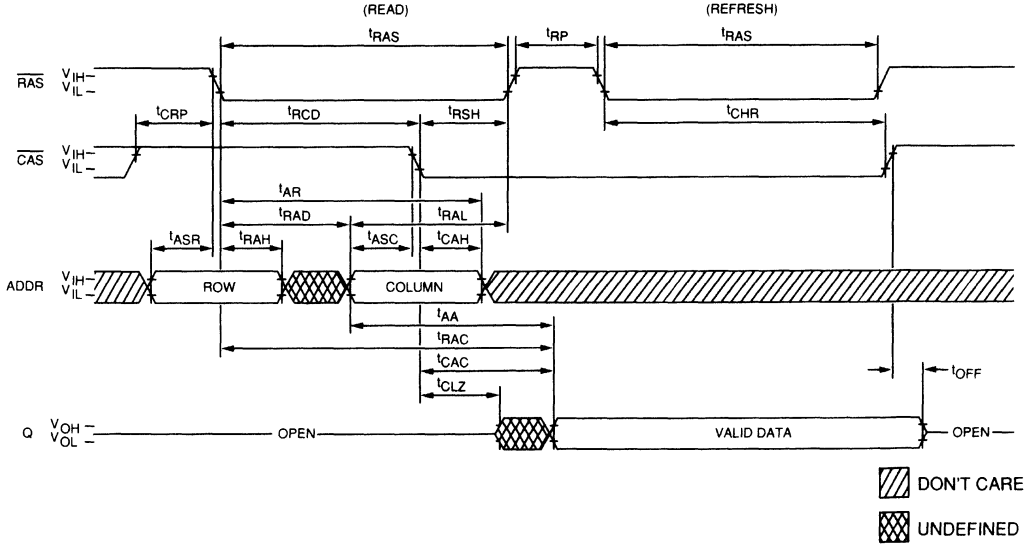
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[23]



DRAM

1MEG x 4 DRAM

FAST PAGE MODE

FEATURES

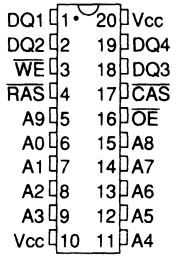
- Industry standard x4 pin-out, timing, functions and packages
- High performance CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby, 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024 cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional Fast Page Mode access cycle

OPTIONS

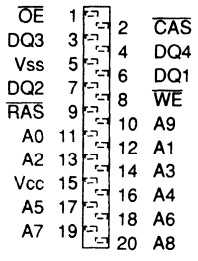
	MARKING
• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

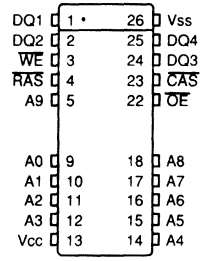
20 Pin DIP



20 Pin ZIP



20 Pin SOJ



NOTE: packaging information to be determined

GENERAL DESCRIPTION

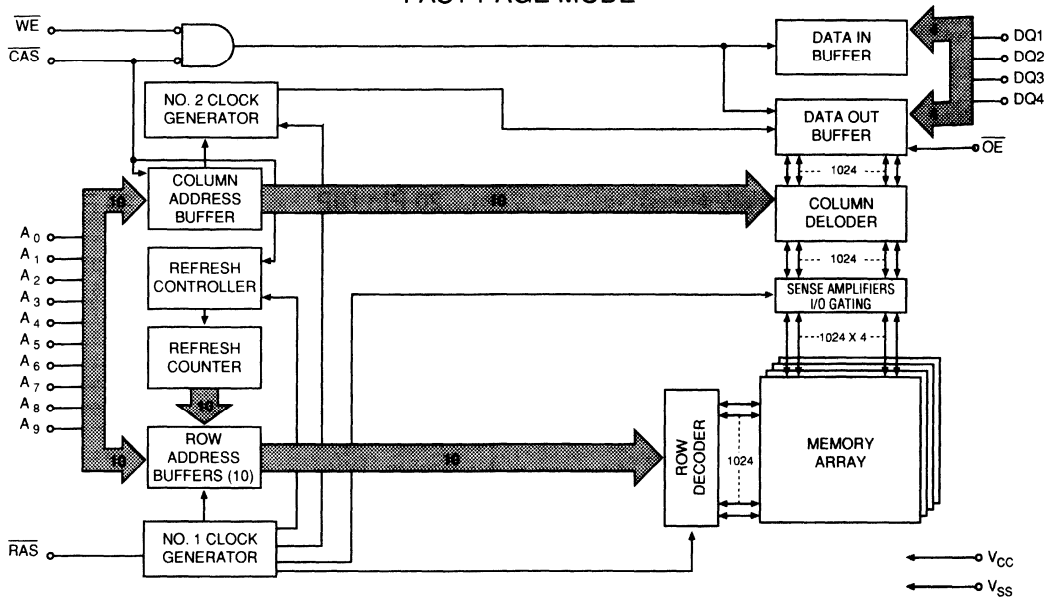
The MT4C4001 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains low (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The 4 data inputs and 4 data outputs are routed through 4 pins using common I/O and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the PAGE MODE operation.

DRAM

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



TRUTH TABLE

Function	RAS	CAS	WE	Addresses tR	Addresses tC	
Standby	H	H	H	X	X	High Impedance
READ	L	L	H	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In
PAGE MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out
PAGE MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In
PAGE MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input ($0V \le V_{IN} \le 6.5V$, all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, $0V \le V_{OUT} \le 5.5V$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA) Output Low voltage (I_{OUT} = 4.2mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

		MAX				
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}	100	85	60	mA	3, 4
STANDBY CURRENT (TTL) Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	3	2	2	mA	
$\overline{RAS}$ ONLY REFRESH CURRENT Average power supply current, $\overline{RAS}$ ONLY mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC3}	100	85	60	mA	3
FAST PAGE MODE CURRENT Average power supply current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC4}	60	50	30	mA	3,4
STANDBY CURRENT (CMOS) Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC5}	1	1	1	mA	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT Average power supply current, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC6}	100	85	60	mA	3

DRAM

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	160		190		220		ns	
READ-MODIFY-WRITE cycle time	t_{RWC}	205		245		295		ns	
PAGE-MODE READ or WRITE cycle time	t_{PC}	50		60		70		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		25		35	ns	15
Output Enable	t_{OE}		25		25		30	ns	
Access time from column address	t_{AA}		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		55		65	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	t_{RASP}	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		35		ns	
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	35	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{CAS}$ precharge time	t_{CPN}	15		15		20		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	t_{CP}	15	25	15	25	15	25	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	60	25	75	35	85	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		15		20		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	40	20	50	30		ns	18
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	60		75		90		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		50		60		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	25	0	25	ns	20
Output Disable	t_{OD}		25		25	30	25	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

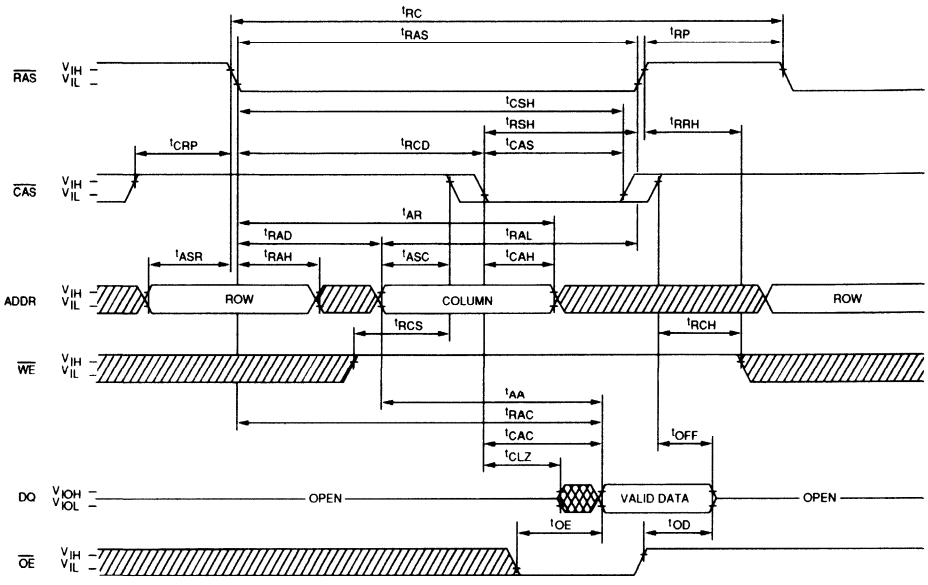
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
FAST PAGE MODE READ-MODIFY-WRITE cycle time	^tPRWC	100		115		140		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		90		ns	
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	110		135		160		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	70		85		100		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	25		25		75		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	20		20		30		ns	5

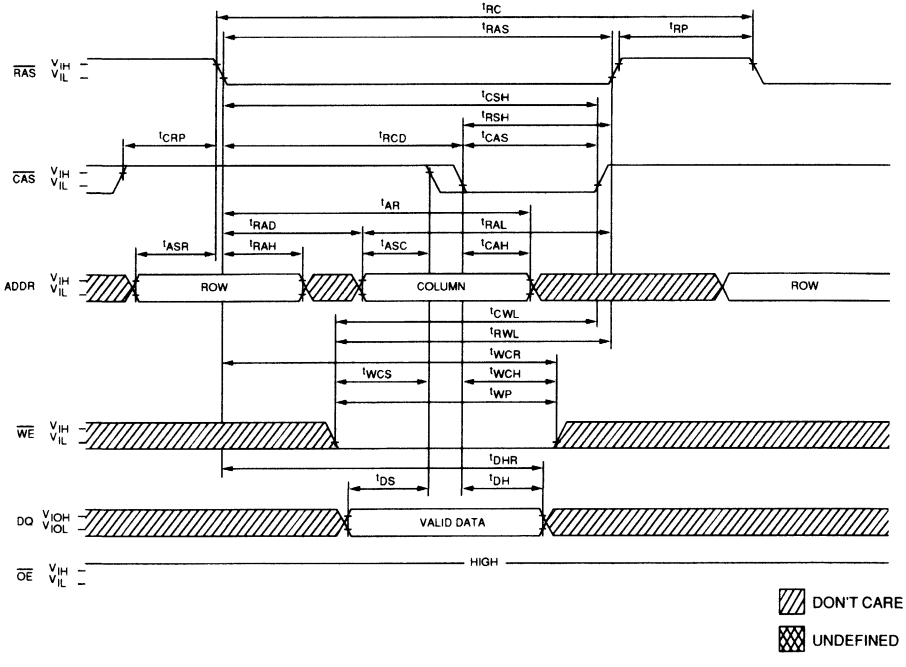
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \ge {}^tRWD$ (min), $^tAWD \ge {}^tAWD$ (min) and $^tCWD \ge {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a READ-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.

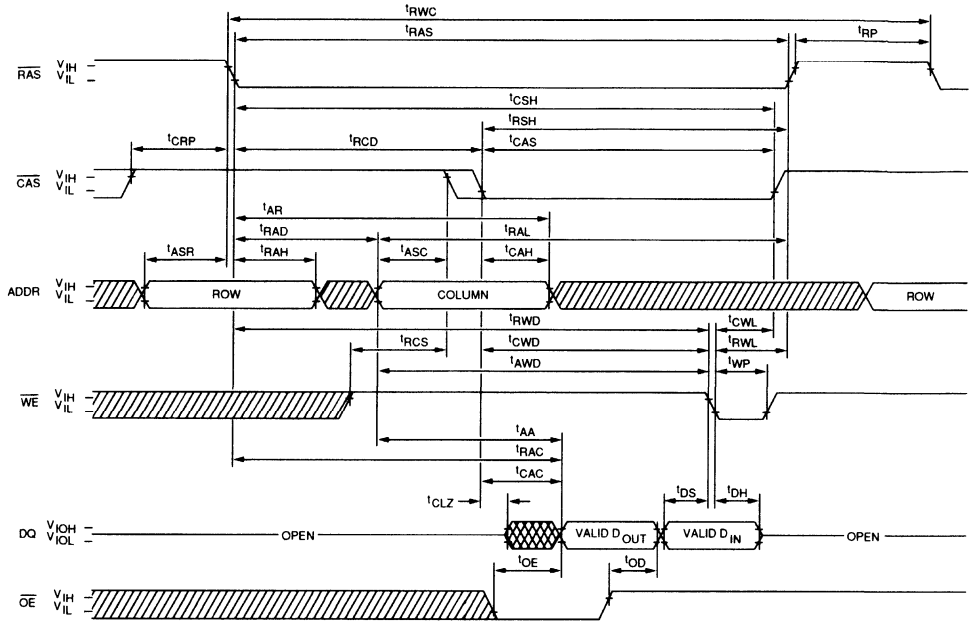
READ CYCLE



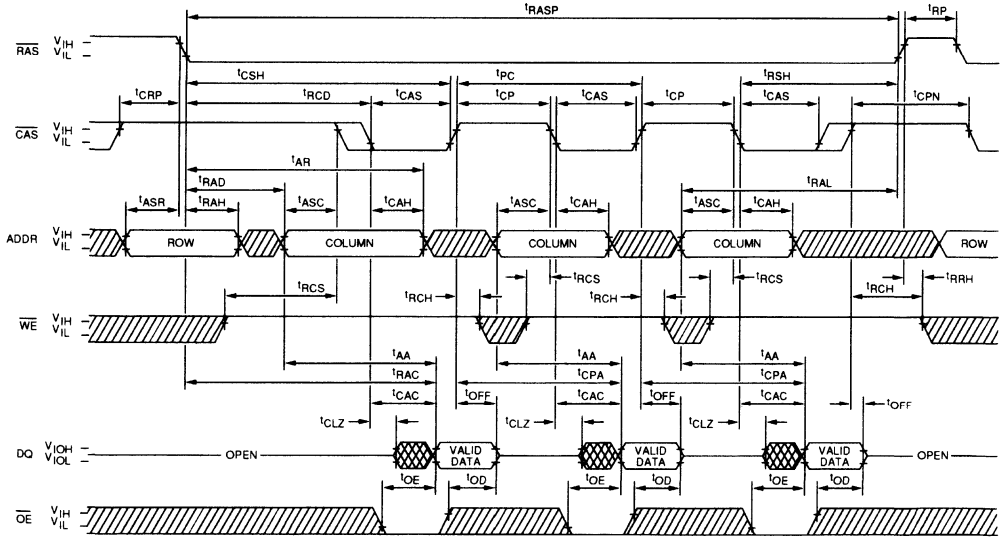
EARLY-WRITE CYCLE



READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



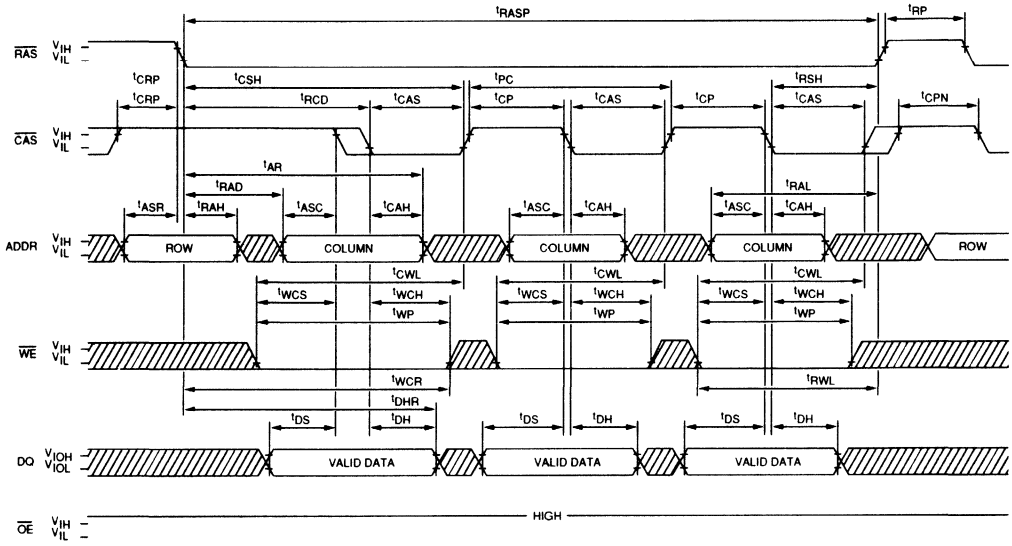
PAGE-MODE READ CYCLE



DON'T CARE

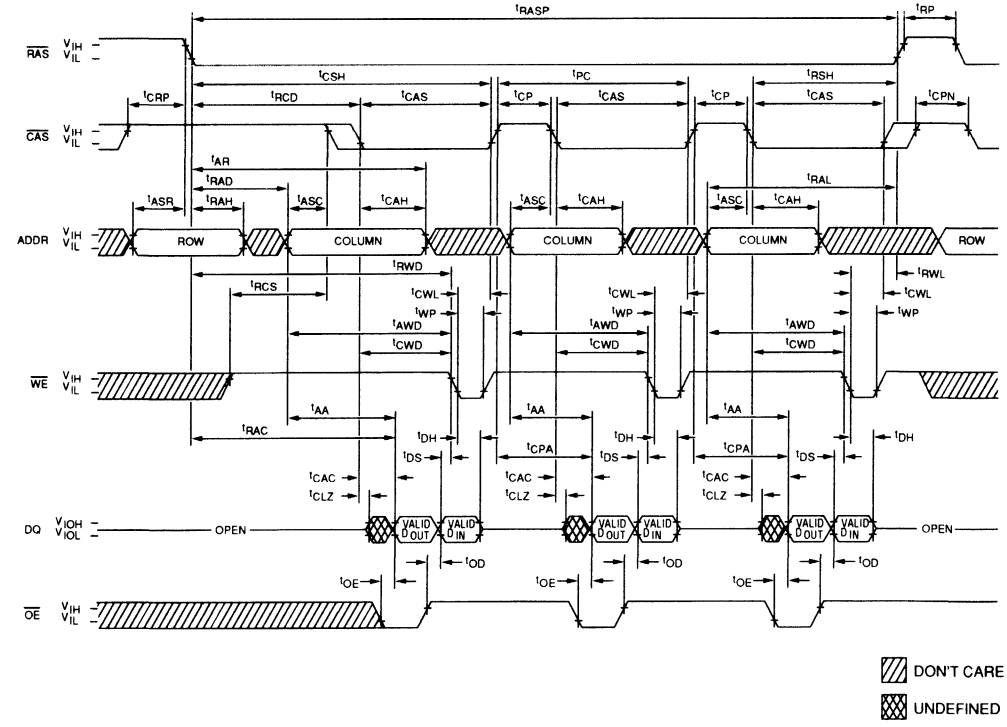
UNDEFINED

PAGE-MODE EARLY-WRITE CYCLE



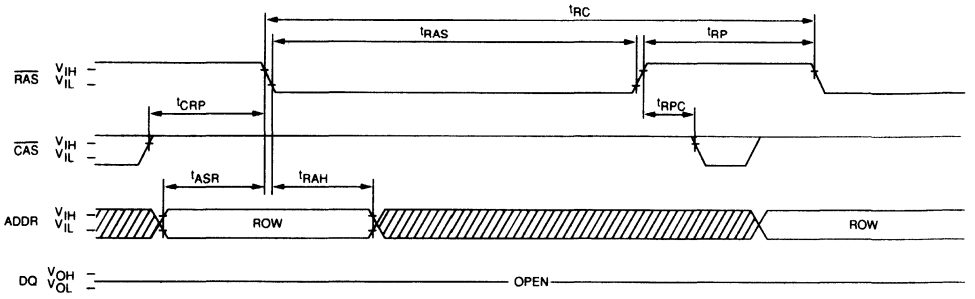
PAGE-MODE READ-WRITE CYCLE

(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



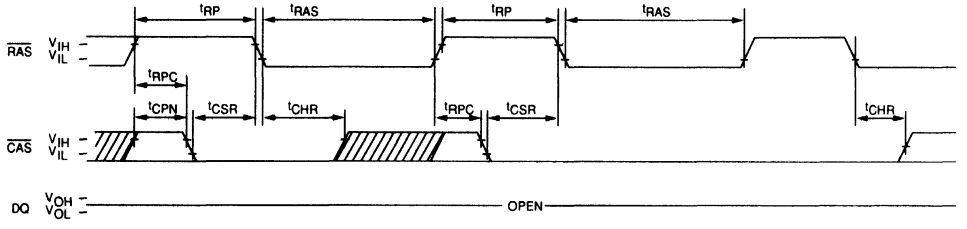
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_9; $\overline{WE}$ = DON'T CARE.)



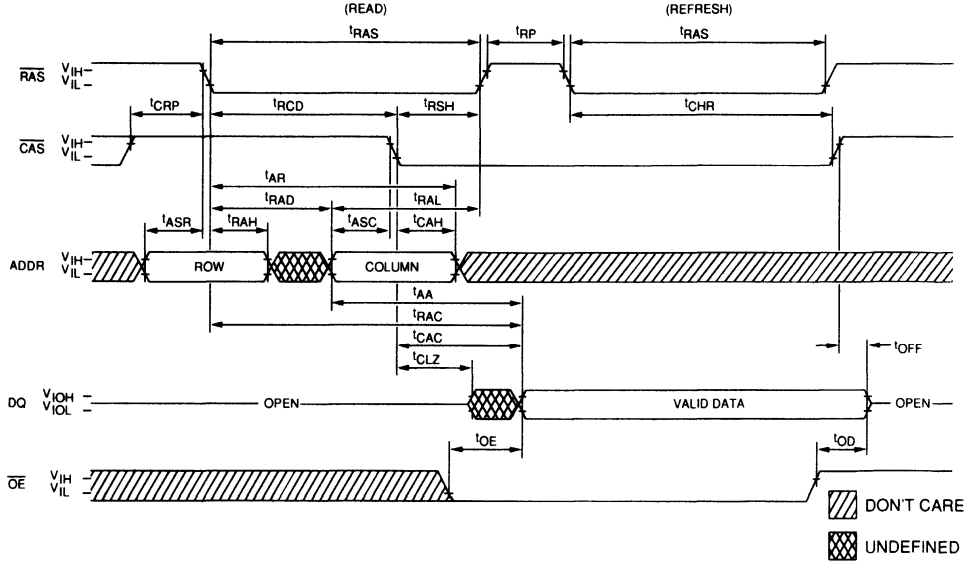
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH, $\overline{OE}$=LOW)[24]



DRAM

1MEG x 4 DRAM

STATIC COLUMN

FEATURES

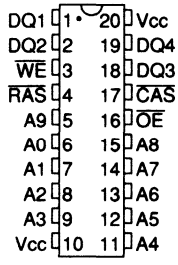
- Industry standard x4 pin-out, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024 cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional Static Column access cycle

OPTIONS

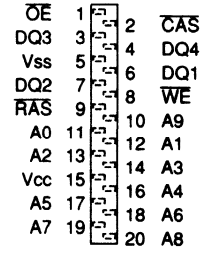
	MARKING
• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

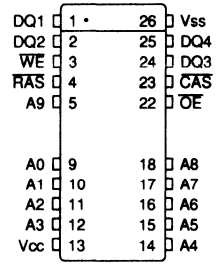
20 Pin DIP



20 Pin ZIP



20 Pin SOJ



NOTE: Package information to be determined

GENERAL DESCRIPTION

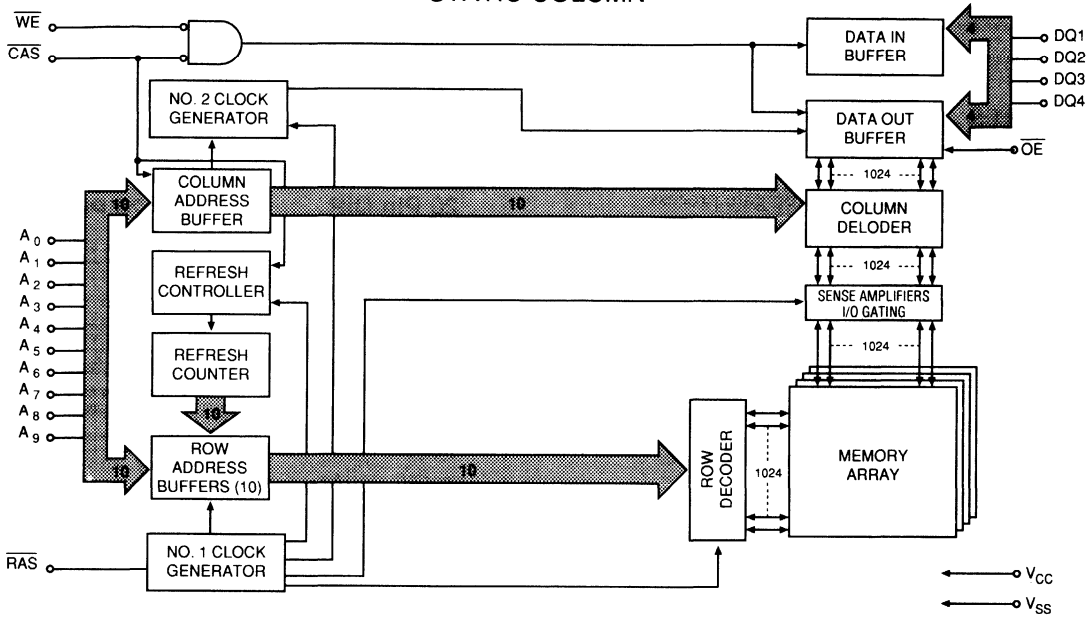
The MT4C4003 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The 4 data inputs and 4 data outputs are routed through 4 pins using common I/O and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

The STATIC COLUMN cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

FUNCTIONAL BLOCK DIAGRAM

STATIC COLUMN



TRUTH TABLE

Function	RAS	CAS	WE	Addresses tR	Addresses tC	
Standby	H	H	H	X	X	High Impedance
READ	L	L	H	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In
STATIC COLUMN READ	L	L	H	ROW	COL COL	Valid Data Out Valid Data Out
STATIC COLUMN WRITE	L	L	L	ROW	COL COL	Valid Data In Valid Data In
STATIC COLUMN READ-WRITE	L	L	H→L→H	ROW	COL COL	Valid Data Out, Valid Data In
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

		MAX				
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}	100	85	60	mA	3, 4
STANDBY CURRENT (TTL) Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	3	2	2	mA	
$\overline{RAS}$ ONLY REFRESH CURRENT Average power supply current, $\overline{RAS}$ ONLY mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC3}	100	85	60	mA	3
STATIC COLUMN CURRENT Average power supply current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC4}	60	50	30	mA	3,4
STANDBY CURRENT (CMOS) Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC5}	1	1	1	mA	24
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT Average power supply current, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC6}	100	85	60	mA	3

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_9	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	160		190		220		ns	
READ-MODIFY-WRITE cycle time	^tRWC	205		245		295		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		35	ns	15
Output Enable	^tOE		25		25		35	ns	
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		55		65	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		35		ns	
$\overline{RAS}$ precharge time	^tRP	70		80		90		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	35	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	15		15		20		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	25	75	35	85	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		10		15		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		15		20		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	40	20	50	25	60	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	95		115		140		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	35	ns	20
Output Disable	^tOD		20		20		35	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

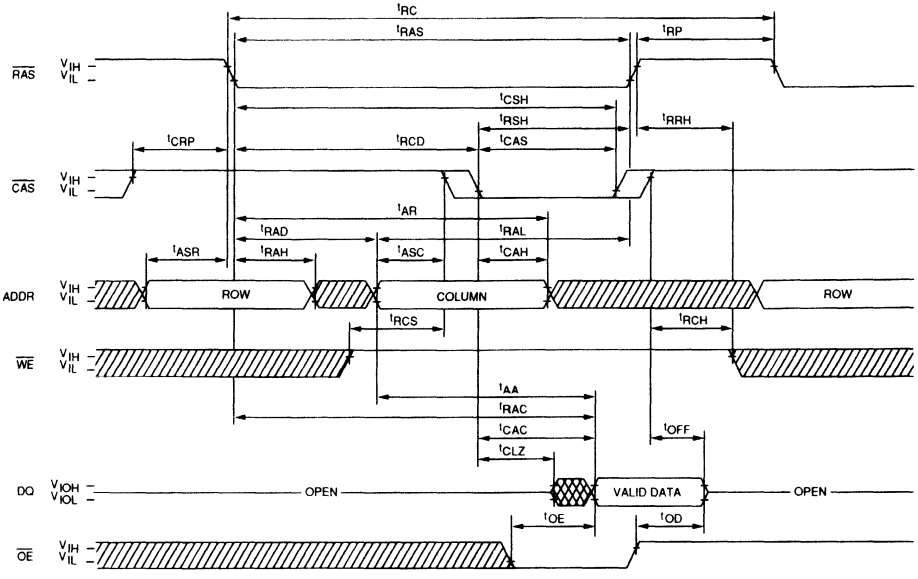
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		90		ns	
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		35		ns	
Write inactive time	^tWI	10		10		10		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	110		135		155		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	70		85		100		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		60		75		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	20		20		30		ns	5
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	80	100,000	100	100,000	120	100,000	ns	
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10	25	10	25	15	30	ns	
STATIC COLUMN MODE cycle time	^tSC	45		55		65		ns	
STATIC COLUMN READ-MODIFY-WRITE cycle time	^tSRMW	110		135		160		ns	
Last write to column address delay time	^tLWAD	20	35	25	45	30	55	ns	
Last write to column address hold time	^tAHLW	75		95		115		ns	
$\overline{RAS}$ hold time precharged to $\overline{OE}$	^tROH	10		20		20		ns	
Output data hold time from column address	^tAOH	5		5		5		ns	
Output data enable from write	^tOW		20		30		40	ns	
$\overline{OE}$ to data delay	^tOED	20		25		30		ns	
$\overline{OE}$ command hold time	^tOEH	20		25		30		ns	
Access time from last Write	^tALW		75		95		115	ns	

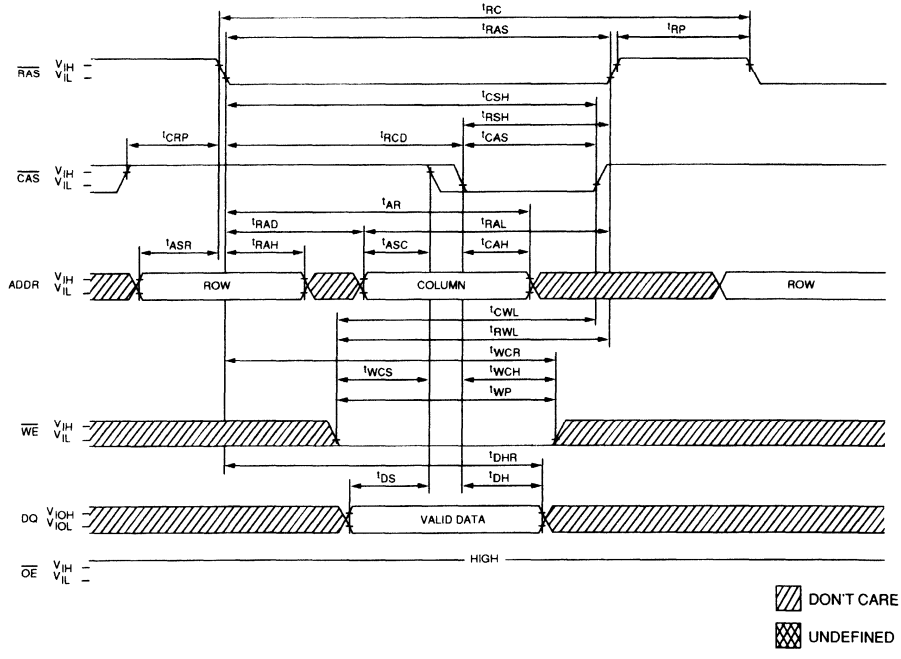
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (min), $^tAWD \geq {}^tAWD$ (min) and $^tCWD \geq {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a READ-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.

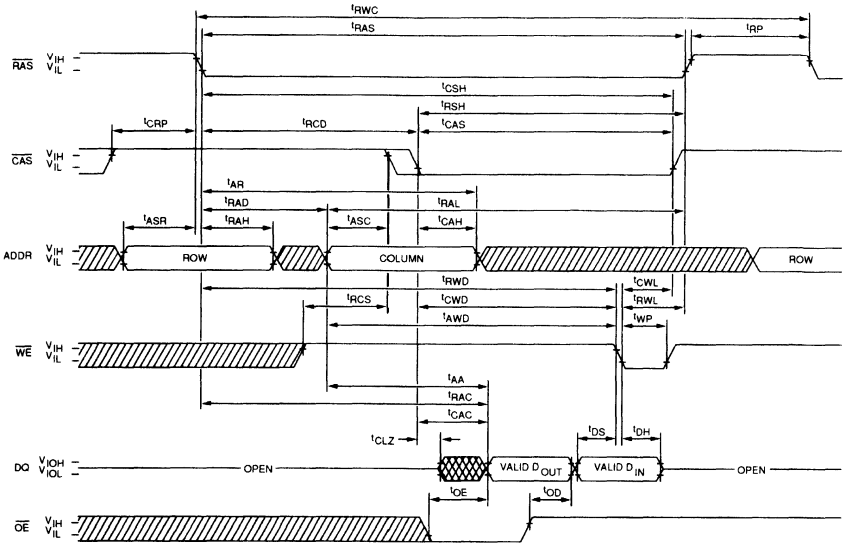
READ CYCLE



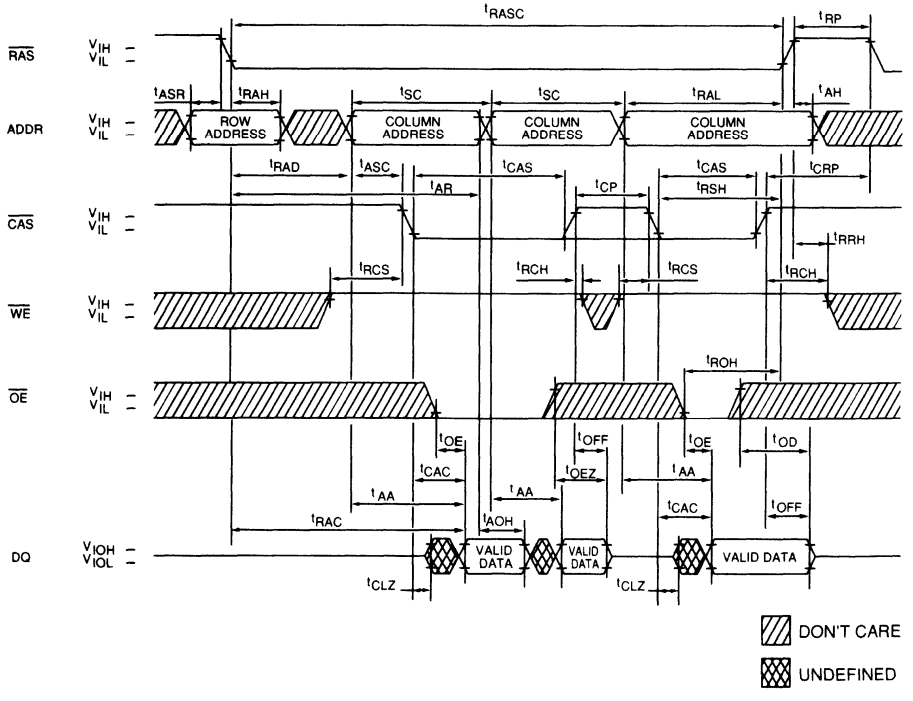
EARLY-WRITE CYCLE



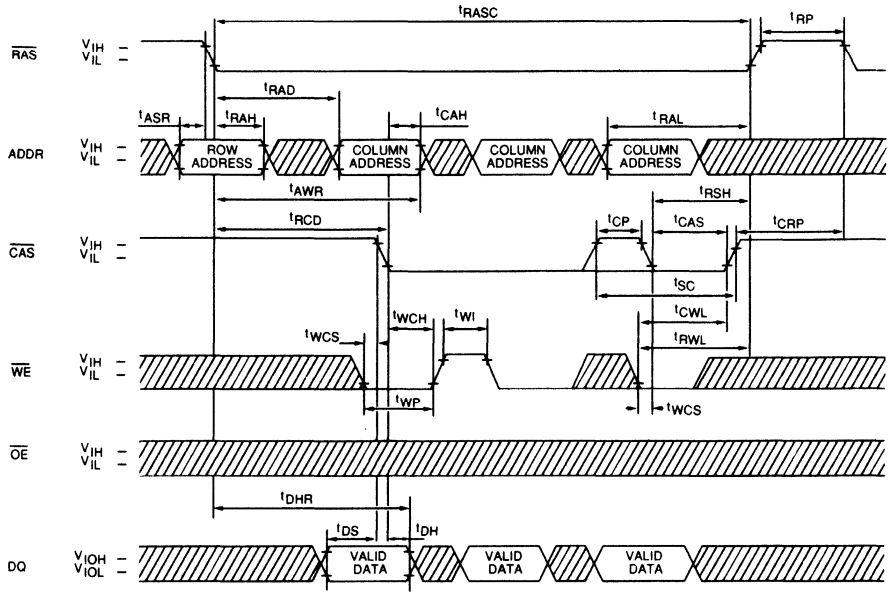
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



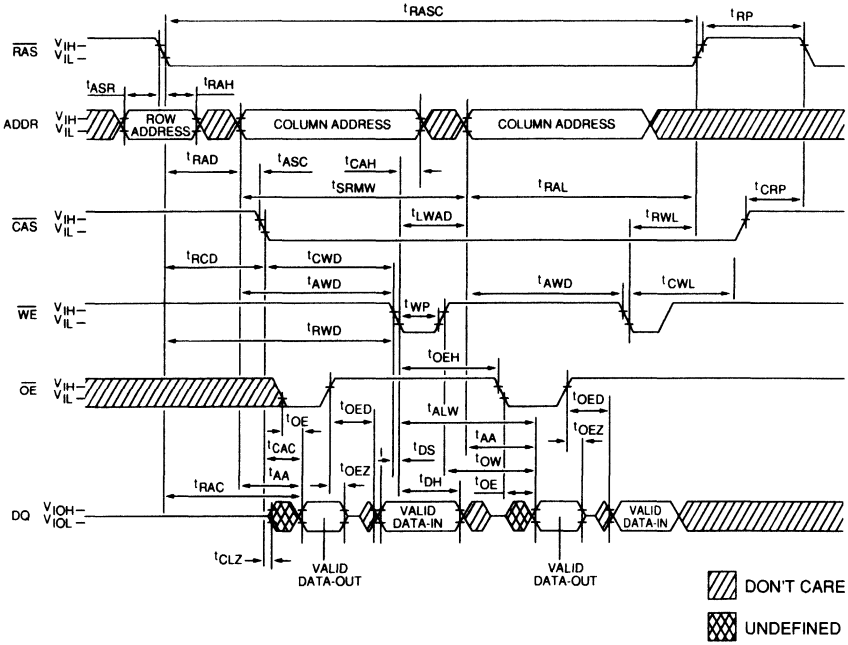
STATIC COLUMN READ CYCLE



STATIC COLUMN EARLY-WRITE CYCLE

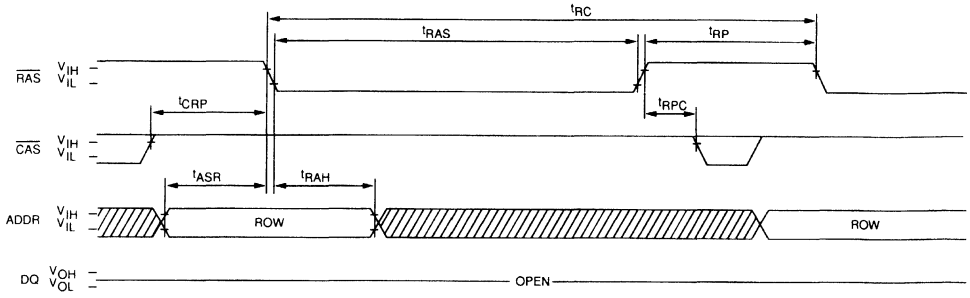


STATIC COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



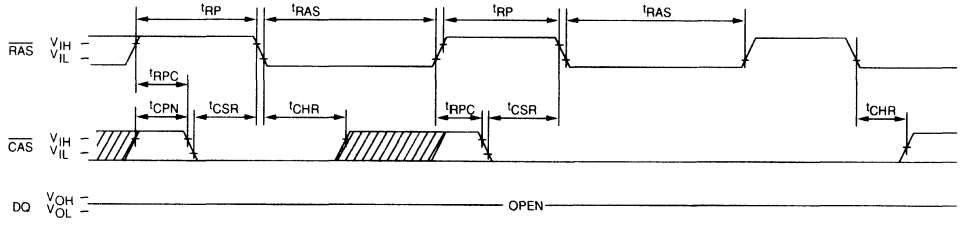
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_9; $\overline{WE}$ = DON'T CARE.)



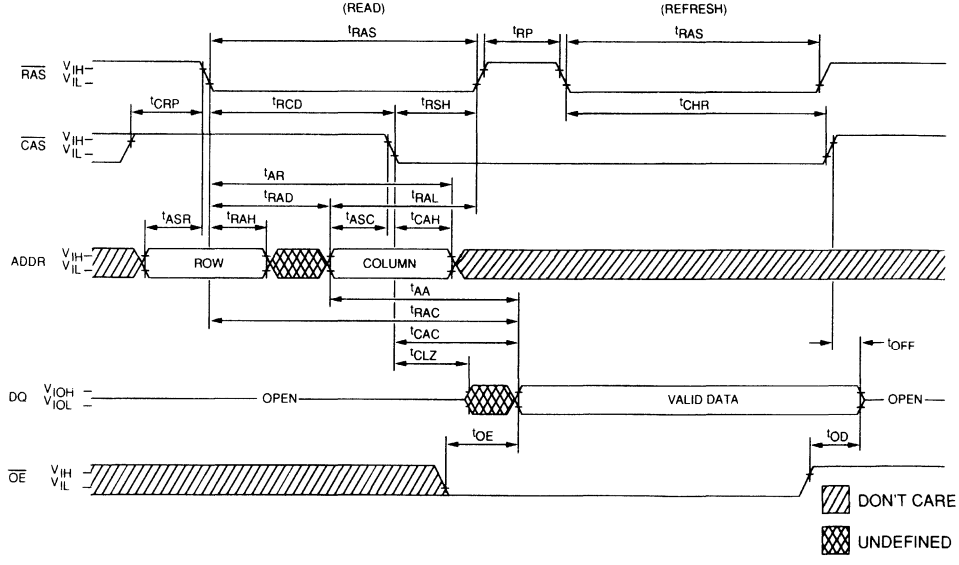
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH, $\overline{OE}$=LOW)[24]



DRAM

4MEG x 1 DRAM

FAST PAGE MODE

FEATURES

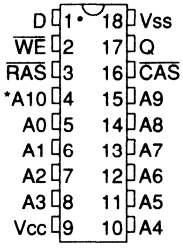
- Industry standard x1 pin-out, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024 cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional Fast Page Mode access cycle

OPTIONS

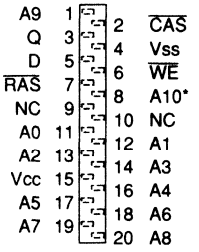
	MARKING
• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

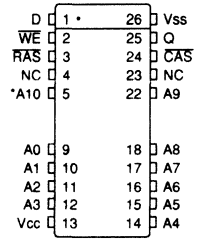
20 Pin DIP



20 Pin ZIP



20 Pin SOJ



*Address not used for $\overline{RAS}$ ONLY refresh
NOTE: Packaging information to be determined

GENERAL DESCRIPTION

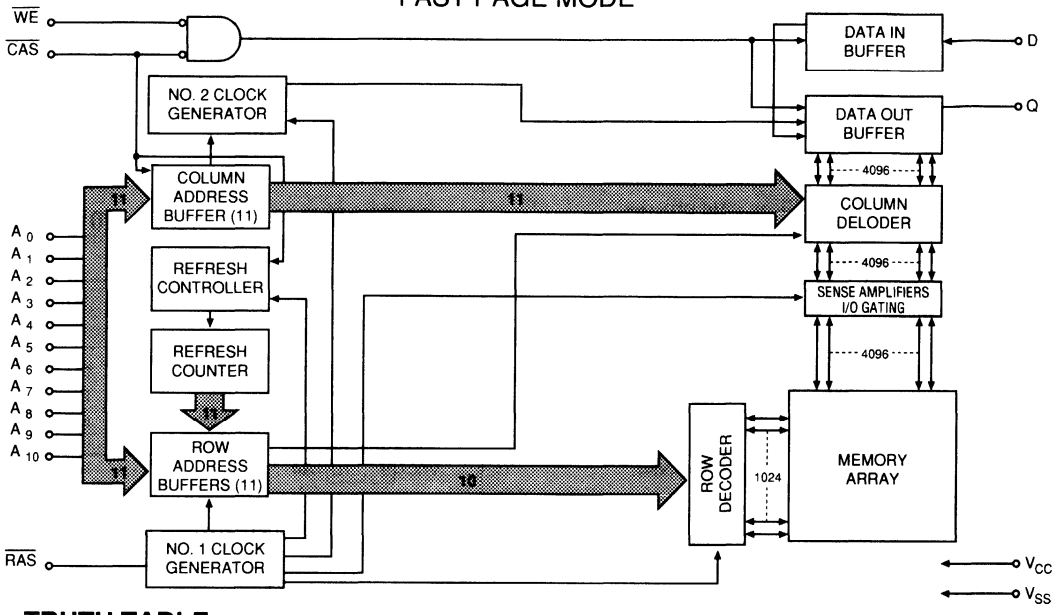
The MT4C1004 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A10) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM

FAST PAGE MODE



TRUTH TABLE

Function	RAS	CAS	WE	Addresses tR	Addresses tC	
Standby	H	H	H	X	X	High Impedance
READ	L	L	H	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In
PAGE MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out
PAGE MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In
PAGE MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input ($0V \le V_{IN} \le 6.5V$, all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, $0V \le V_{OUT} \le 5.5V$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA) Output Low voltage (I_{OUT} = 4.2mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

		MAX				
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}	100	85	60	mA	3, 4
STANDBY CURRENT (TTL) Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	3	2	2	mA	
$\overline{RAS}$ ONLY REFRESH CURRENT Average power supply current, $\overline{RAS}$ ONLY mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC3}	100	85	60	mA	3
FAST PAGE MODE CURRENT Average power supply current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC4}	60	50	30	mA	3,4
STANDBY CURRENT (CMOS) Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC5}	1	1	1	mA	24
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT Average power supply current, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC6}	100	85	60	mA	3

DRAM

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_{10}, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	160		190		220		ns	
READ-MODIFY-WRITE cycle time	^tRWC	185		220		255		ns	
PAGE-MODE READ or WRITE cycle time	^tPC	50		60		70		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		35	ns	15
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		55		60	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		35		ns	
$\overline{RAS}$ precharge time	^tRP	70		80		90		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	35	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	15		15		20		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	15	25	15	25	15	25	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	25	75	30	85	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	12		15		20		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	40	20	50	30	60	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		75		110		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		10		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	25	0	25	ns	20
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

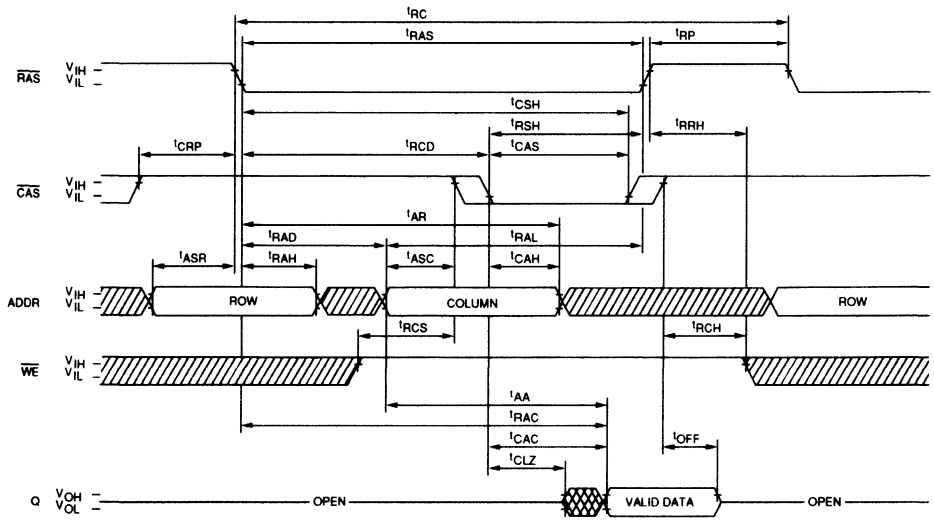
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		110		ns	
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		110		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		100		120		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	25		25		35		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	20		20		30		ns	5

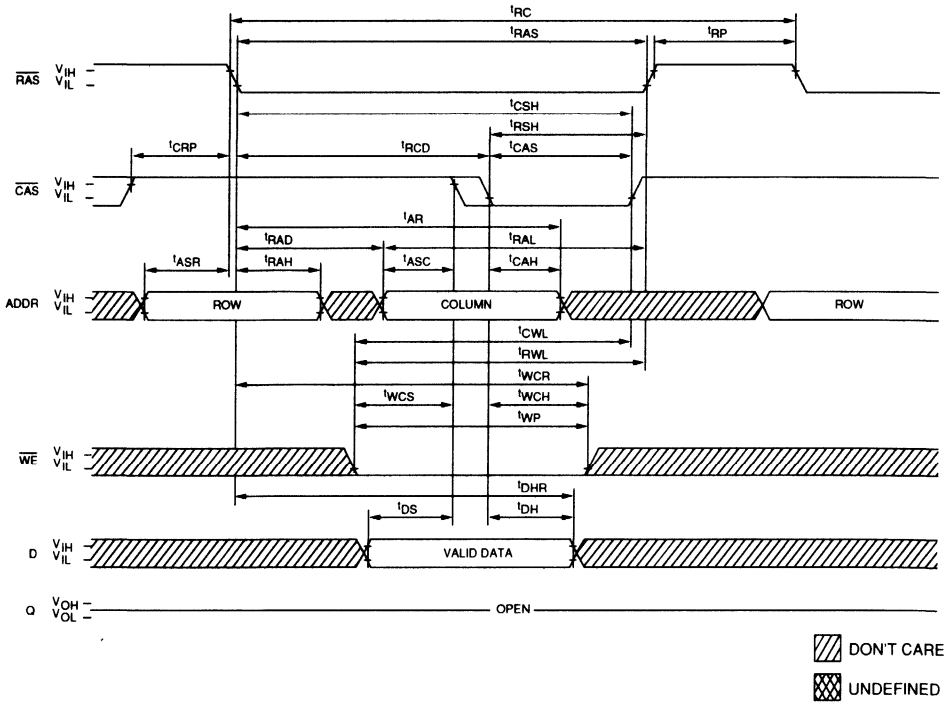
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (min), $^tAWD \ge {}^tAWD$ (min) and $^tCWD \ge {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

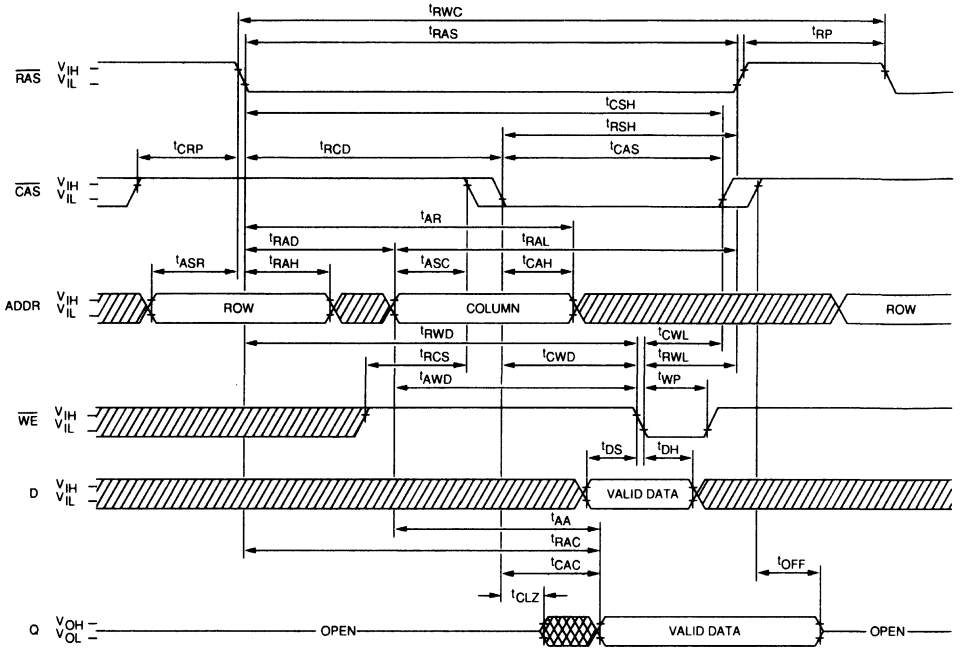
READ CYCLE



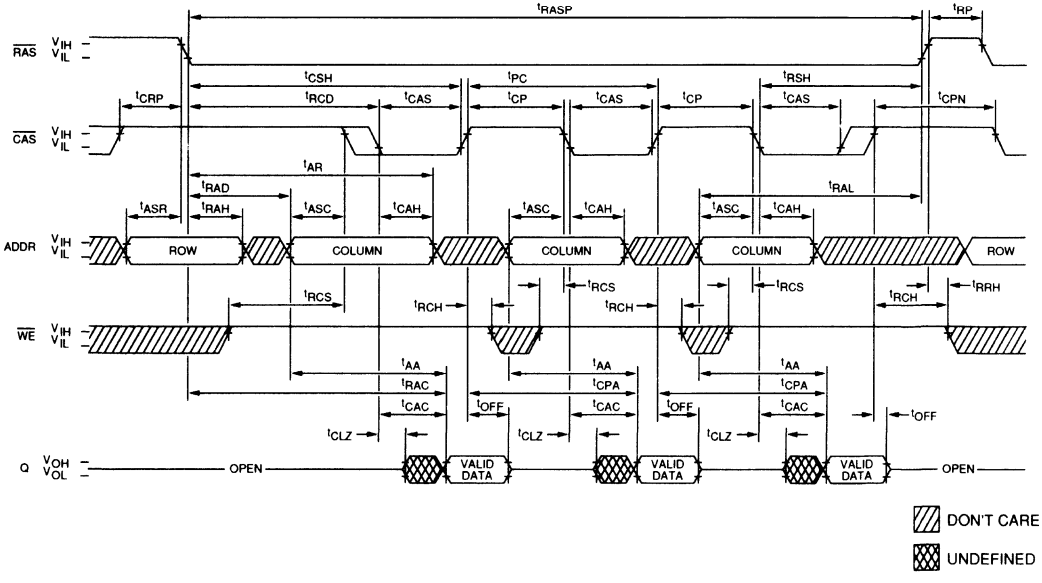
EARLY-WRITE CYCLE



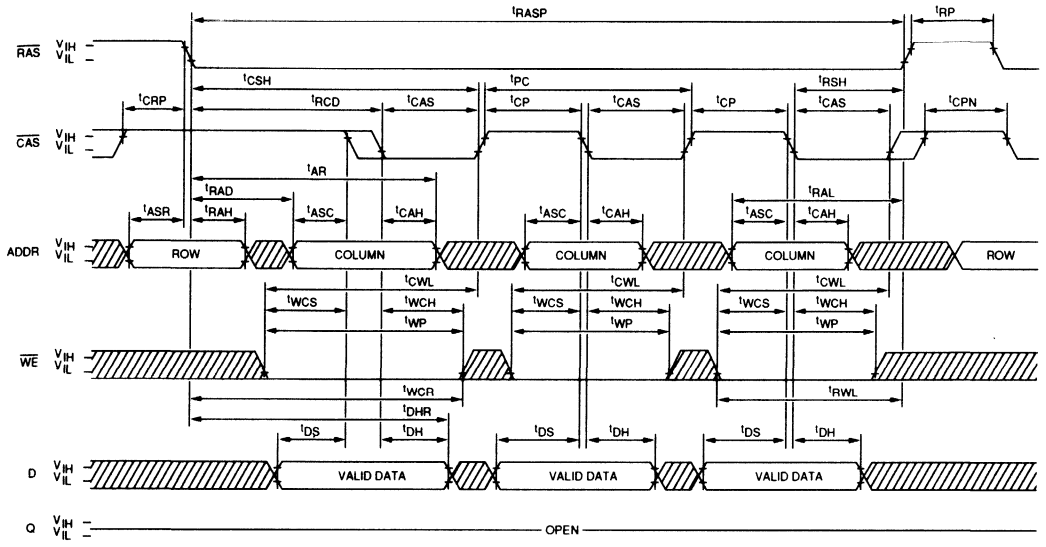
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE

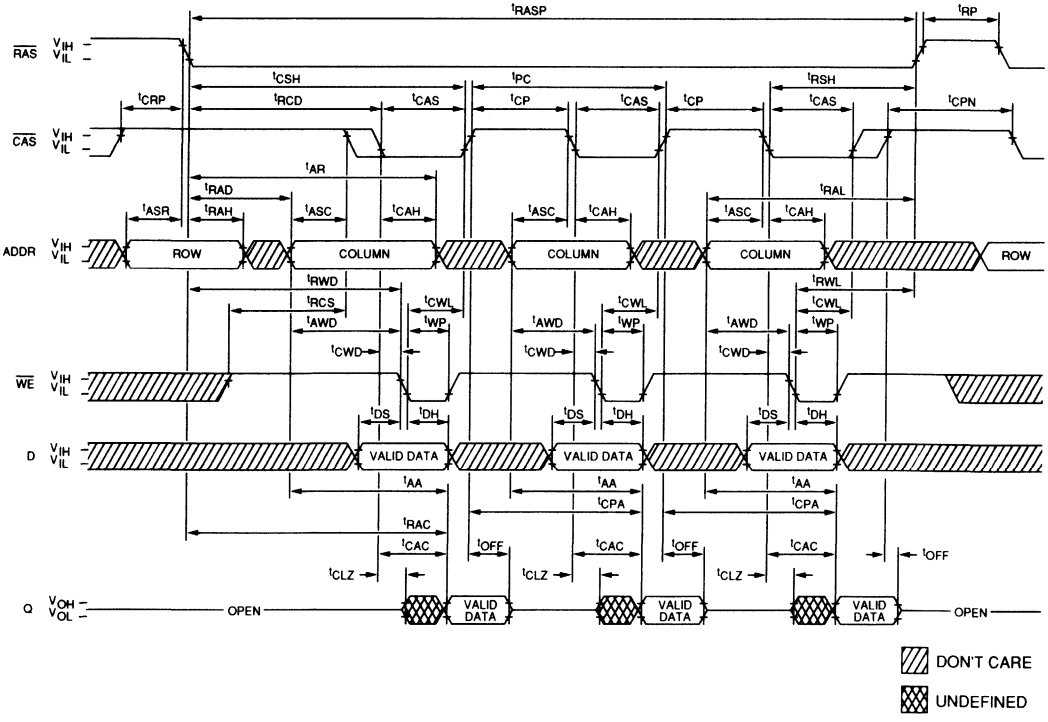


PAGE-MODE EARLY-WRITE CYCLE



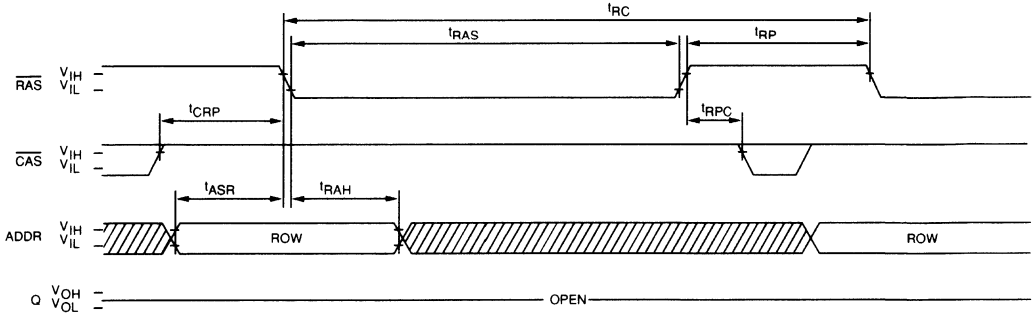
PAGE-MODE READ-WRITE CYCLE

(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



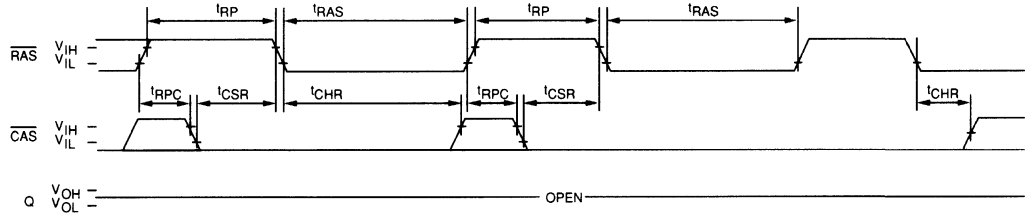
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_9; A_{10} and $\overline{WE}$ = DON'T CARE.)



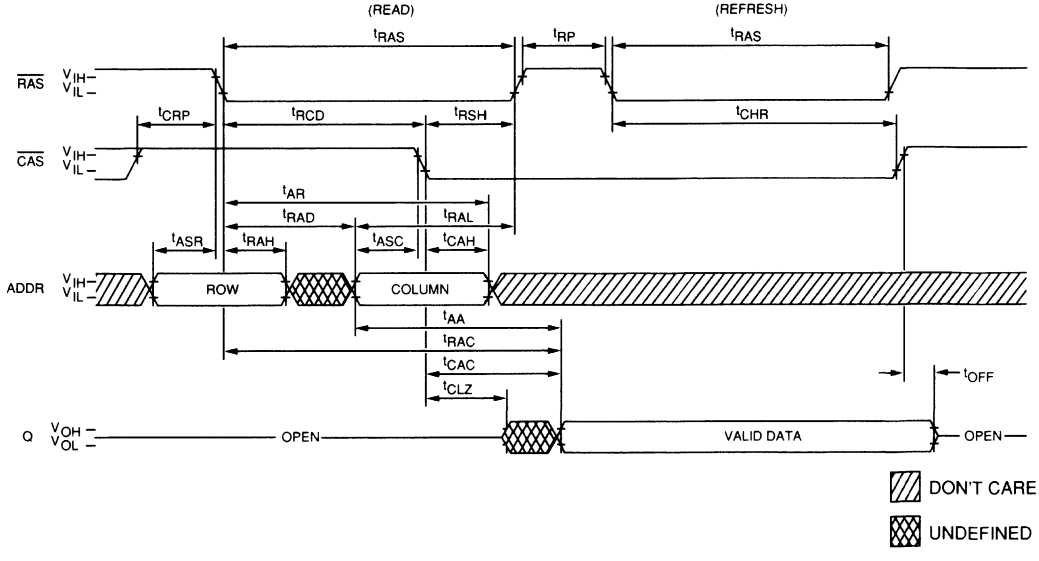
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_{10} and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[23]



DRAM

4MEG x 1 DRAM

NIBBLE MODE

FEATURES

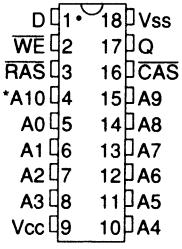
- Industry standard x1 pin-out, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply.
- Low power, 5mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024 cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional Nibble Mode access cycle

OPTIONS

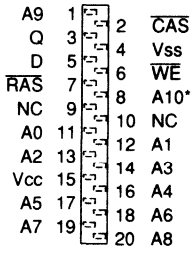
	MARKING
• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

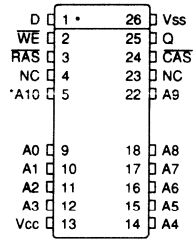
20 Pin DIP



20 Pin ZIP



20 Pin SOJ



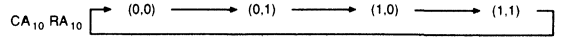
*Address not used for $\overline{RAS}$ ONLY refresh
NOTE: Packaging information to be determined

GENERAL DESCRIPTION

The MT4C1005 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

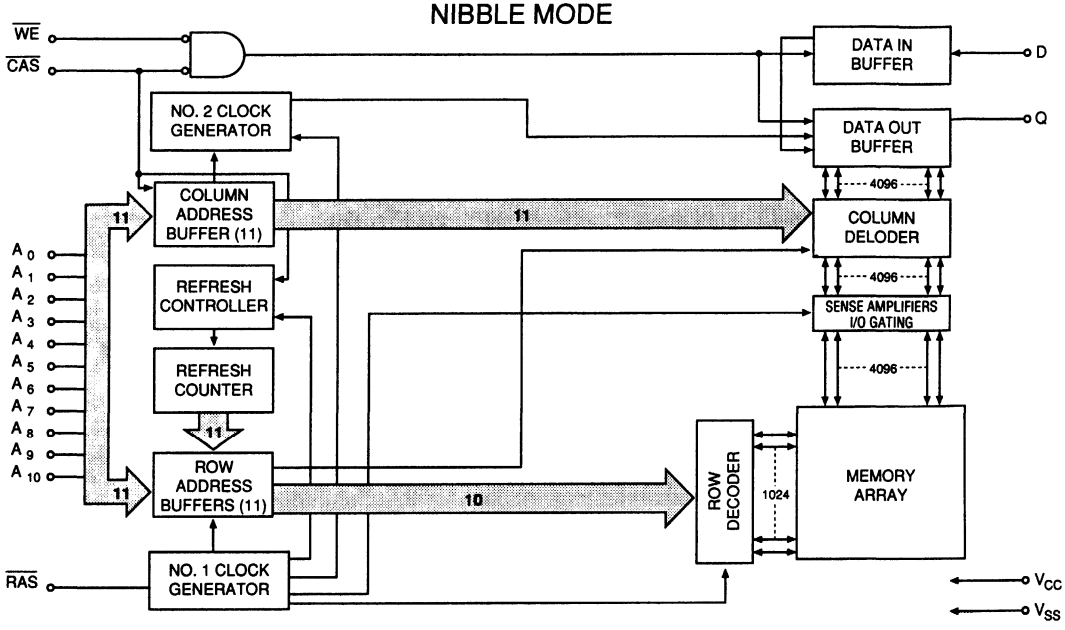
Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

NIBBEL MODE operation allows faster sequential serial data operations (READ, WRITE or READ-MODIFY-WRITE) up to 4 bits. The first of 4 bits is accessed in the usual manner with $\overline{CAS}$ address A9 (nibble MSB) and $\overline{RAS}$ address A9 (nibble LSB) selecting one of 4 bits within a nibble for initial access. By holding $\overline{RAS}$ LOW, $\overline{CAS}$ can be toggled incrementing the nibble address field in modulo 4 fashion with wrap around (see below).



FUNCTIONAL BLOCK DIAGRAM

NIBBLE MODE



TRUTH TABLE

Function	RAS	CAS	WE	Addresses tR	Addresses tC	
Standby	H	H	H	X	X	High Impedance
READ	L	L	H	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In
NIBBLE MODE READ	L	H→L→H, L→H→L	H	ROW	COL	Valid Data Out, Valid Data Out
NIBBLE MODE WRITE	L	H→L→H, L→H→L	L	ROW	COL	Valid Data In, Valid Data In
NIBBLE MODE READ-WRITE	L	H→L→H, L→H→L	H→L→H	ROW	COL	Valid Data Out, Valid Data In
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1, 25
INPUT LEAKAGE CURRENT any input ($0V \le V_{IN} \le 6.5V$, all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, $0V \le V_{OUT} \le 5.5V$)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ± 10%)

		MAX				
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}	100	85	60	mA	3, 4
STANDBY CURRENT (TTL) Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	3	2	2	mA	
$\overline{RAS}$ ONLY REFRESH CURRENT Average power supply current, $\overline{RAS}$ ONLY mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC3}	100	85	60	mA	3
NIBBLE MODE CURRENT Average power supply current, ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC4}	60	50	30	mA	3,4
STANDBY CURRENT (CMOS) Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC5}	1	1	1	mA	24
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT Average power supply current, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC6}	100	85	60	mA	3

DRAM

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_{10}, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	150		180		220		ns	
READ-MODIFY-WRITE cycle time	^tRWC	175		210		255		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		35	ns	15
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		55		65	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		35		ns	
$\overline{RAS}$ precharge time	^tRP	60		70		90		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	35	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	10		15		20		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	25	75	35	85	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		10		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		15		20		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	40	20	50	30	60	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		75		110		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	25	0	25	ns	20
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		80		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

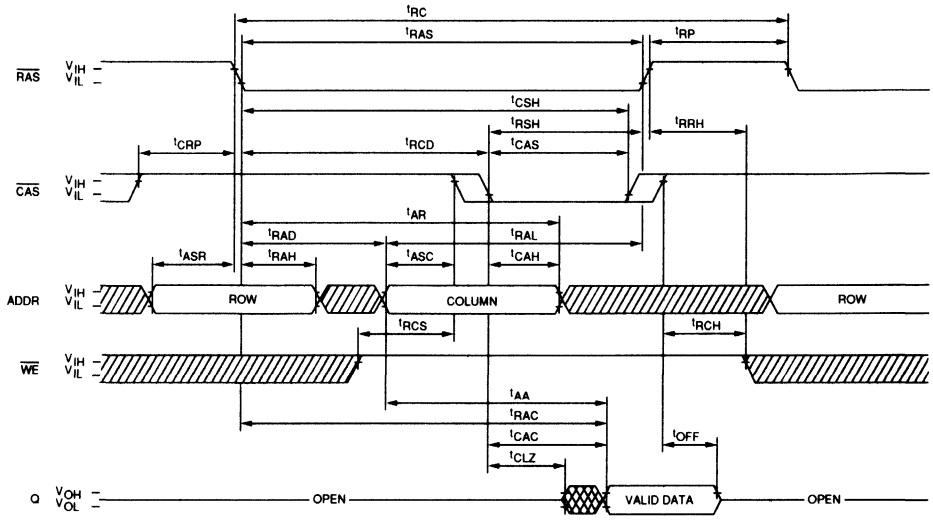
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		110		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		100		120		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		25		35		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0			0	ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5
$\overline{RAS}$ pulse width (NIBBLE MODE)	^tRASN	80	100,000	100	100,000	120	100,000	ns	
$\overline{CAS}$ precharge time (NIBBLE MODE)	^tNCP	10		10		15		ns	
NIBBLE MODE cycle time	^tNC	40		45		55		ns	
NIBBLE MODE READ-MODIFY-WRITE cycle time	^tNRWC	65		75		85		ns	
NIBBLE MODE access time	^tNCAC	20		25		30		ns	15
NIBBLE MODE pulse width	^tNCAS	20		25		30		ns	
NIBBLE MODE $\overline{CAS}$ precharge time	^tNCP	10		10		15		ns	
NIBBLE MODE $\overline{RAS}$ hold time	^tNRSH	20		25		30		ns	
NIBBLE MODE $\overline{CAS}$ to $\overline{WE}$ delay time	^tNCWD	20		25		30		ns	
NIBBLE MODE $\overline{WE}$ command to $\overline{RAS}$ load time	^tNRWL	20		25		30		ns	
NIBBLE MODE $\overline{WE}$ command to $\overline{CAS}$ load time	^tNCWL	20		25		30		ns	

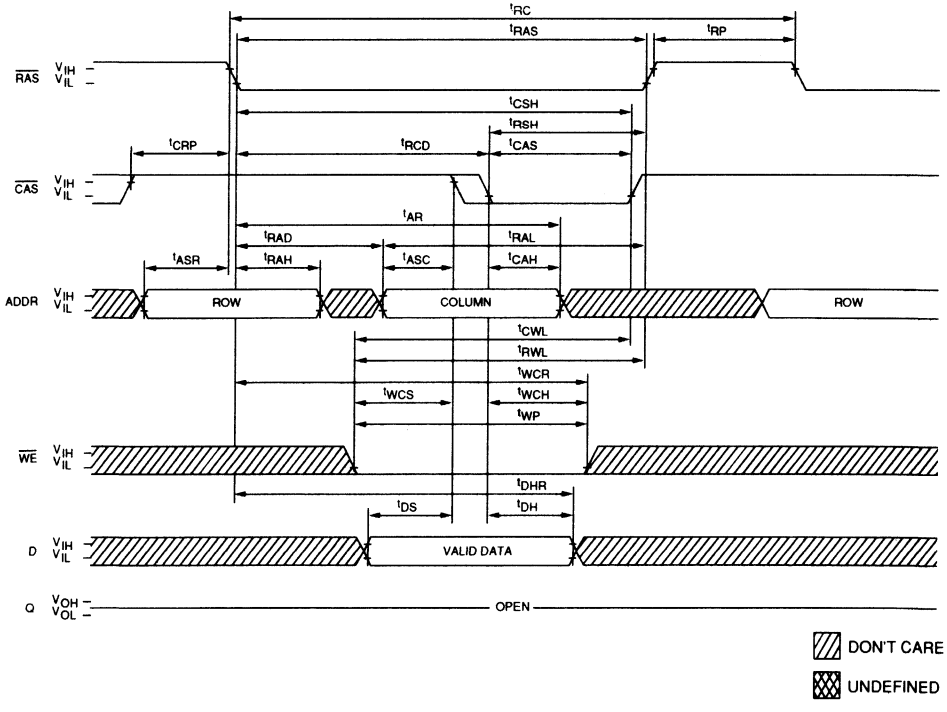
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq ^tRWD$ (min), $^tAWD \geq ^tAWD$ (min) and $^tCWD \geq ^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

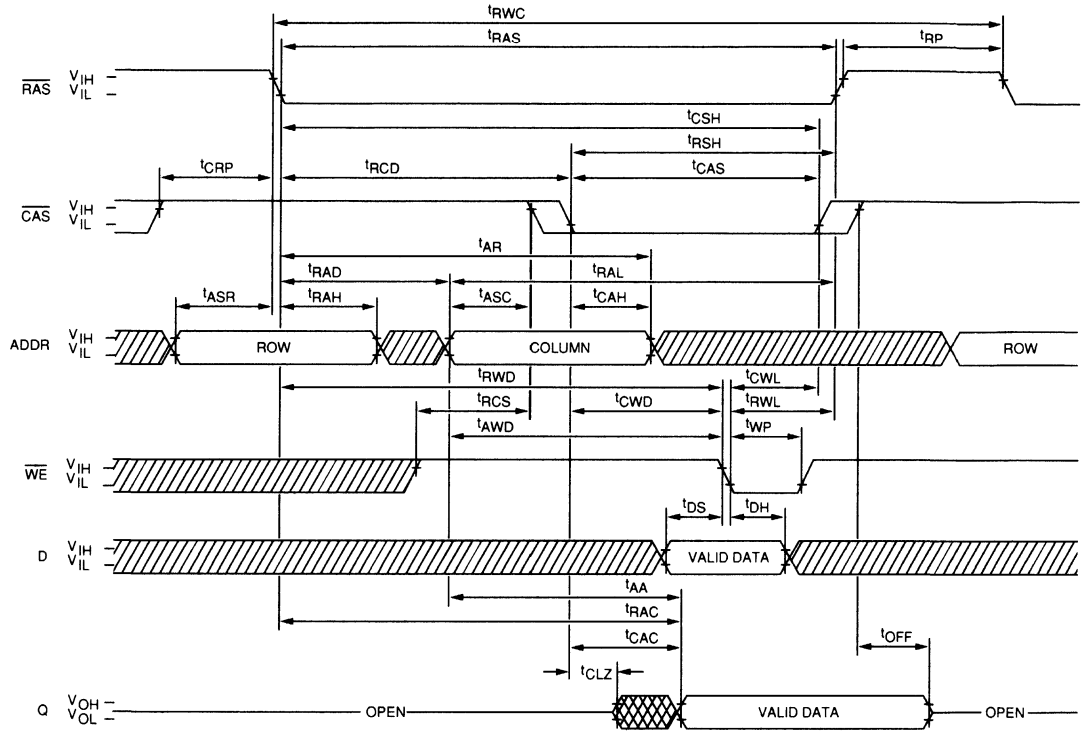
READ CYCLE



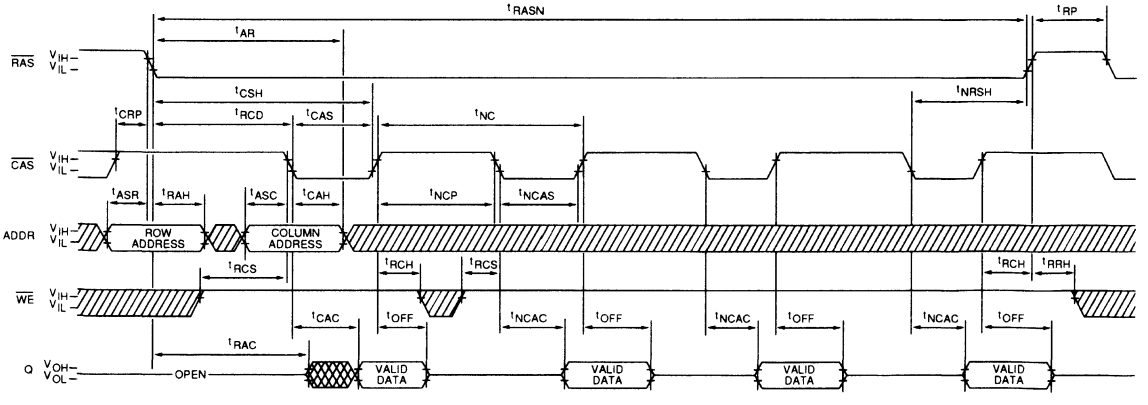
EARLY-WRITE CYCLE



READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



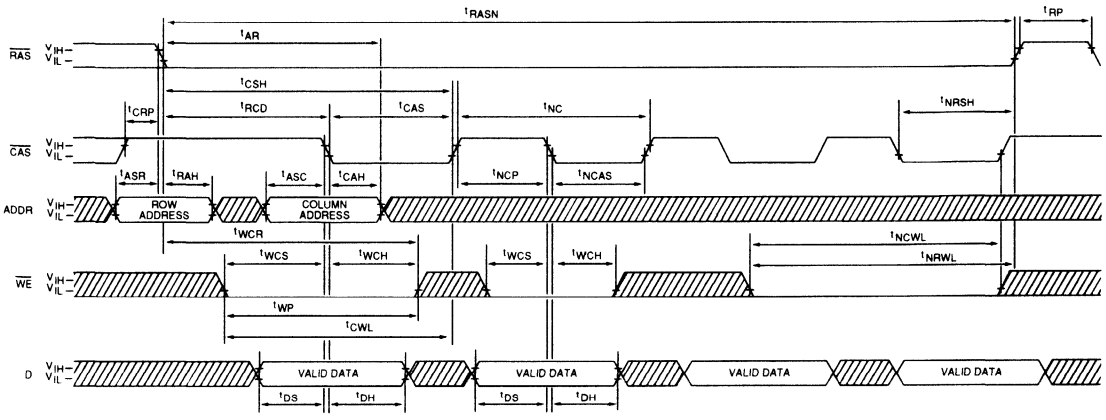
NIBBLE MODE READ CYCLE



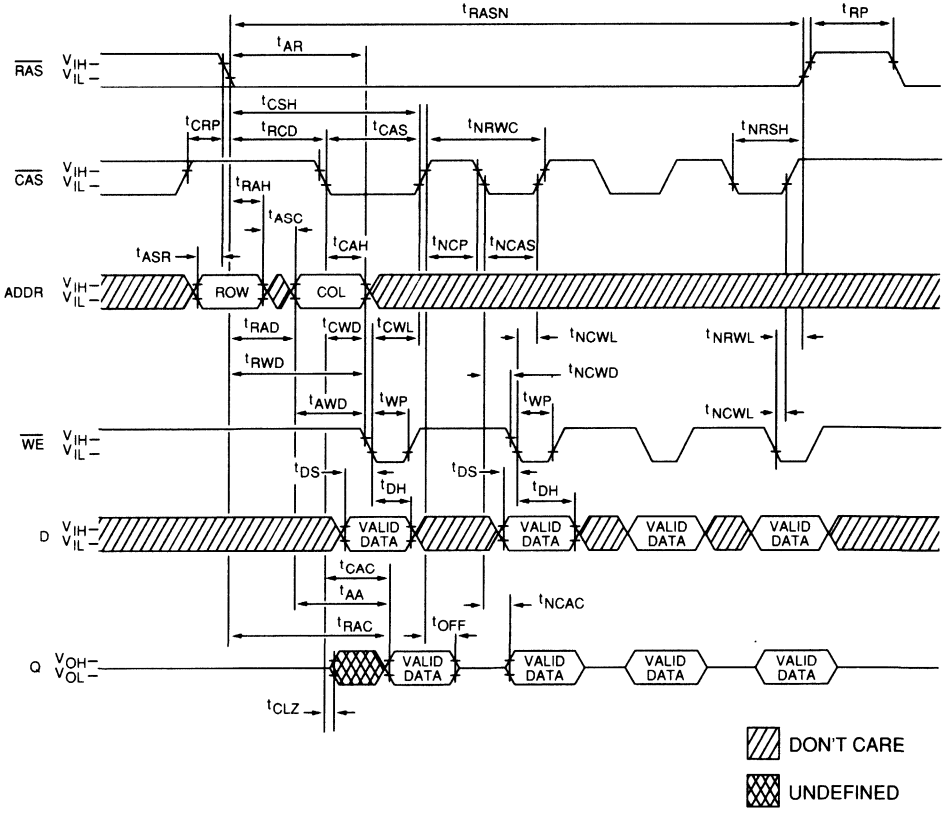
DON'T CARE

UNDEFINED

NIBBLE MODE EARLY-WRITE CYCLE



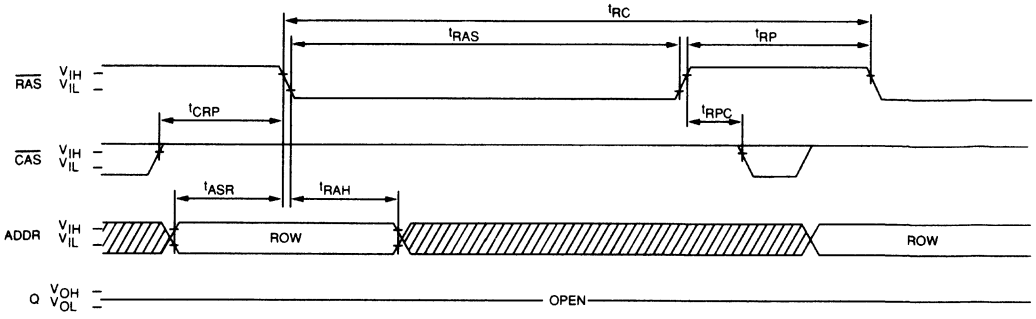
NIBBLE MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



DRAM

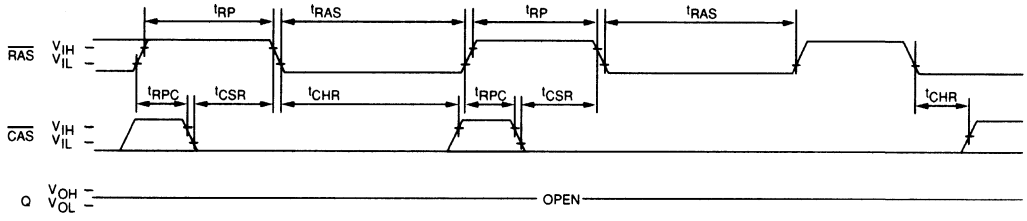
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_9; A_{10} and $\overline{WE}$ = DON'T CARE.)



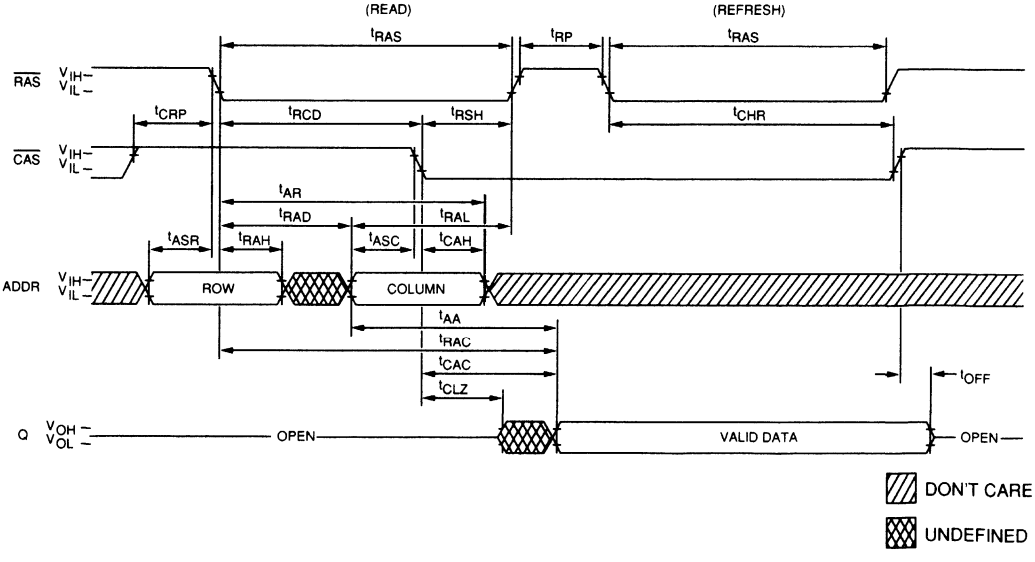
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_{10} and $\overline{WE}$ = DON'T CARE



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[23]



DRAM

4MEG x 1 DRAM

STATIC COLUMN

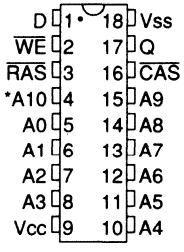
FEATURES

- Industry standard x1 pin-out, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply.
- Low power, 5mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1024 cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional Static Column access cycle

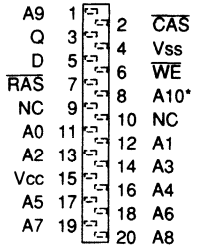
OPTIONS	MARKING
• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
Plastic SOJ	DJ

PIN ASSIGNMENT (Top View)

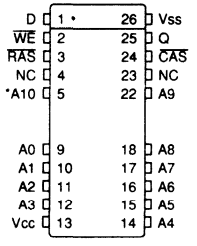
20 Pin DIP



20 Pin ZIP



20 Pin SOJ



*Address not used for $\overline{RAS}$ ONLY refresh
NOTE: Packaging information to be determined

GENERAL DESCRIPTION

The MT4C1006 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$).

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level.

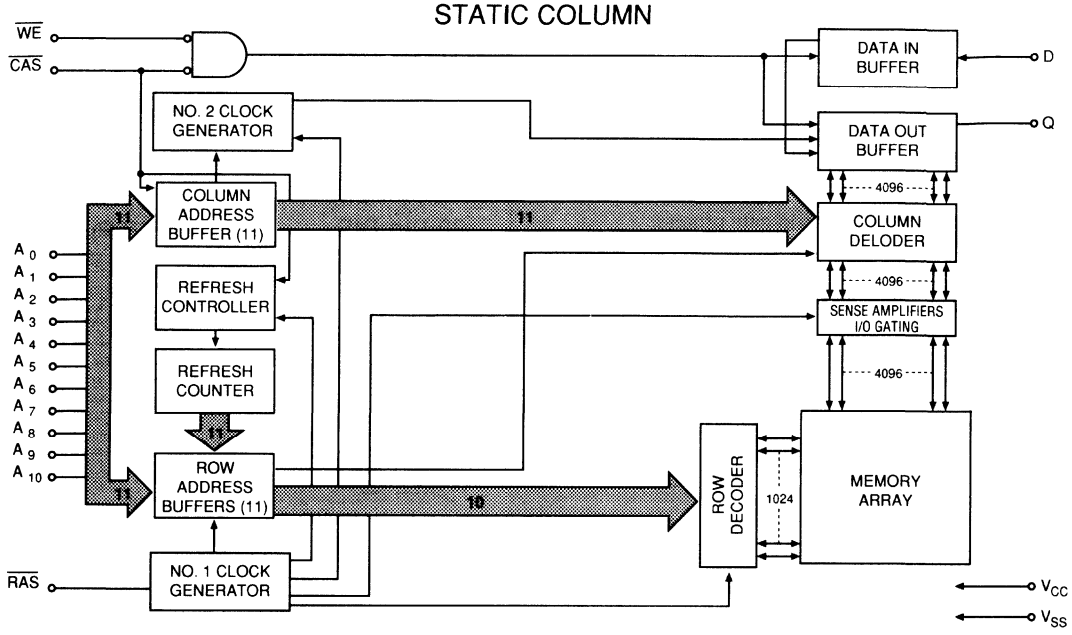
Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 1024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary.

The STATIC COLUMN cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

FUNCTIONAL BLOCK DIAGRAM

STATIC COLUMN



TRUTH TABLE

Function	RAS	CAS	WE	Addresses tR	Addresses tC	
Standby	H	H	H	X	X	High Impedance
READ	L	L	H	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In
STATIC COLUMN READ	L	L	H	ROW	COL COL	Valid Data Out, Valid Data Out
STATIC COLUMN WRITE	L	L	L	ROW	COL COL	Valid Data In Valid Data In
STATIC COLUMN READ-WRITE	L	L	H→L→H	ROW	COL COL	Valid Data Out, Valid Data In
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0 volts)	I_I	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA) Output Low voltage (I_{OUT} = 4.2mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

(Notes : 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; Vcc = 5.0V ± 10%)

		MAX				
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}	100	85	60	mA	3, 4
STANDBY CURRENT (TTL) Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	3	2	2	mA	
$\overline{RAS}$ ONLY REFRESH CURRENT Average power supply current, $\overline{RAS}$ ONLY mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC3}	100	85	60	mA	3
STATIC COLUMN CURRENT Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC4}	60	50	30	mA	3,4
STANDBY CURRENT (CMOS) Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC5}	1	1	1	mA	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT Average power supply current, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC6}	100	85	60	mA	3

DRAM

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_{10}, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	160		190		220		ns	
READ-MODIFY-WRITE cycle time	^tRWC	185		220		255		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		35	ns	15
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		55		65	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		35		ns	
$\overline{RAS}$ precharge time	^tRP	70		80		90		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	35	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	15		15		20		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	25	75	35	85	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		10		15		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		15		20		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	40	20	50	25	60	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	95		115		140		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	25	ns	20
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

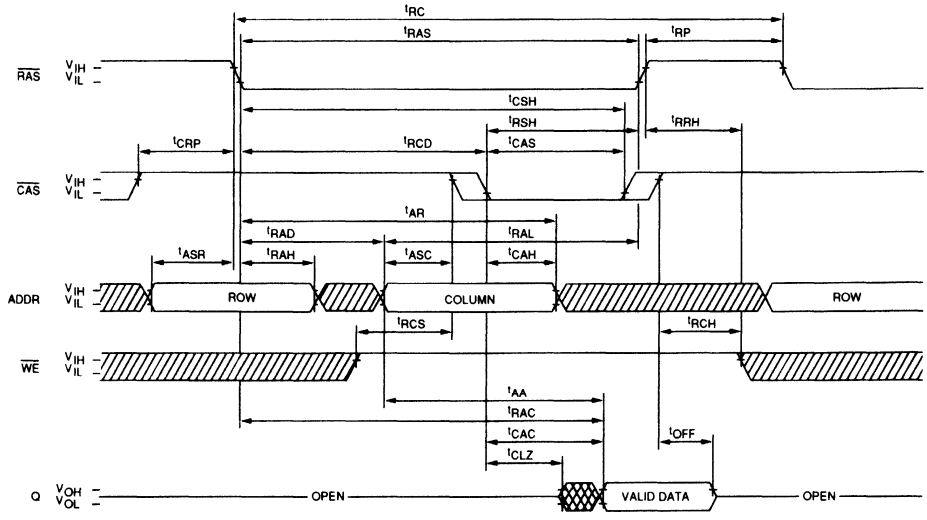
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		90		ns	
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		25		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		100		120		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		100		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		25		35		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	20		20		30		ns	5
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	80	100,000	100	100,000	120	100,000	ns	
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		10		15		ns	
STATIC COLUMN MODE cycle time	^tSC	45		55		65		ns	
STATIC COLUMN READ-MODIFY-WRITE cycle time	^tSRMW	80		100		160		ns	
Last write to column address delay time	^tLWAD	20	35	25	45	30	55	ns	
Last write to column address hold time	^tAHLW	75		95		115		ns	
Output data hold time from column address	^tAOH	5	—	5	—	5	—	ns	
Output data enable from write	^tOW	—	20	—	25	—	30	ns	

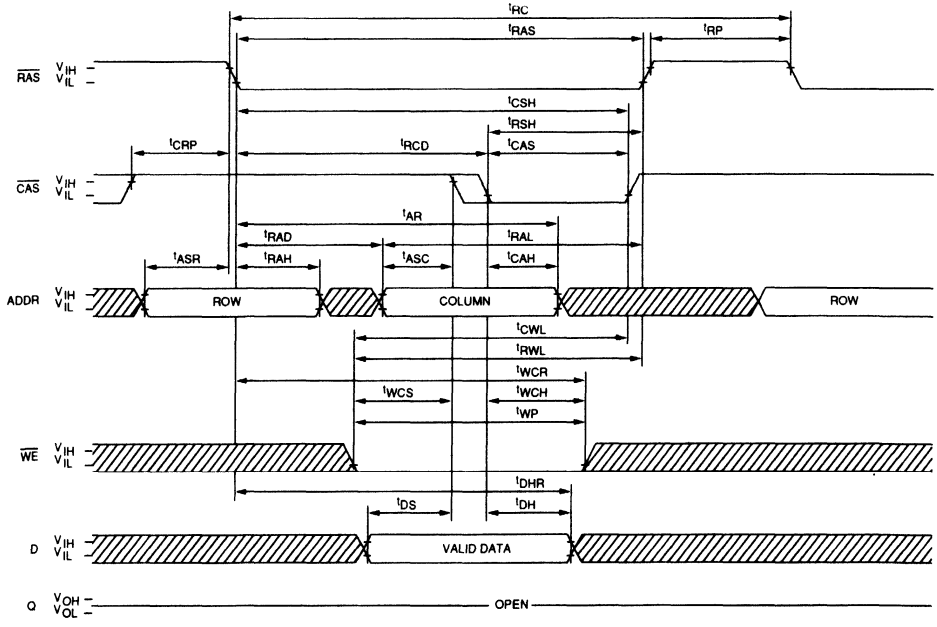
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \geq {}^tRWD$ (min), $^tAWD \geq {}^tAWD$ (min) and $^tCWD \geq {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

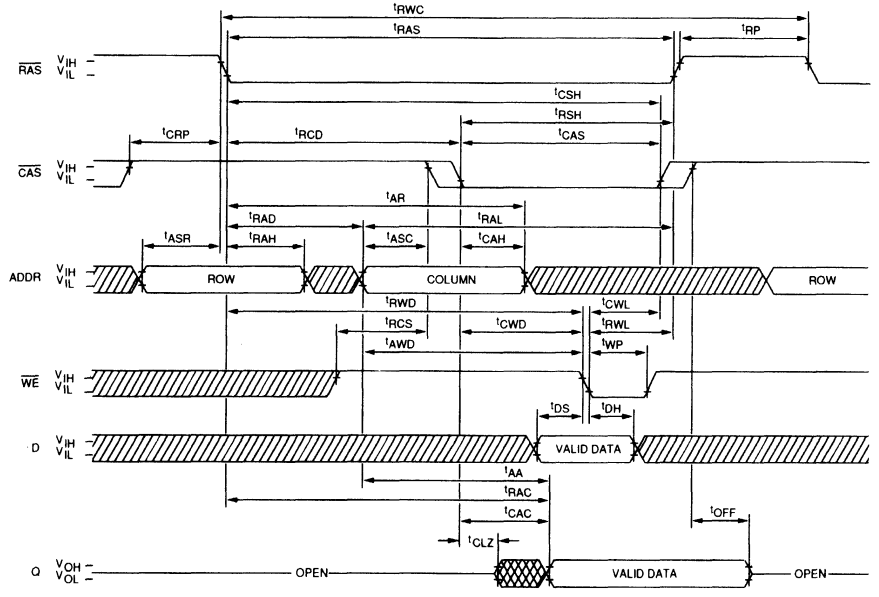
READ CYCLE



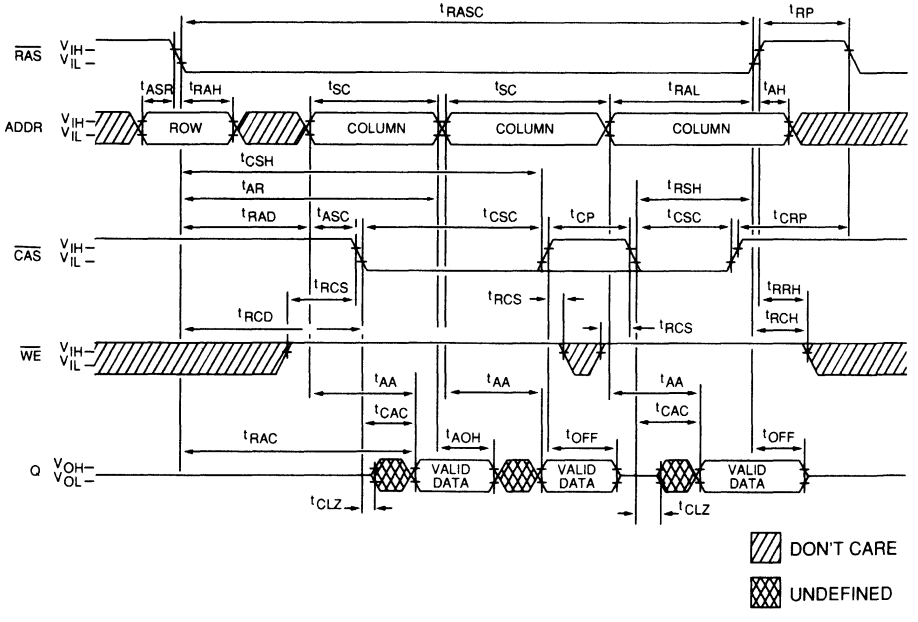
EARLY-WRITE CYCLE



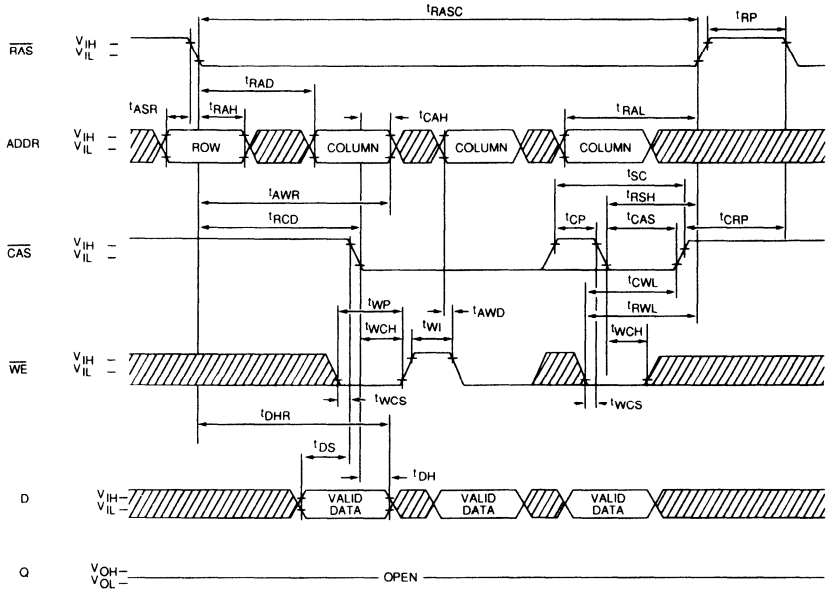
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



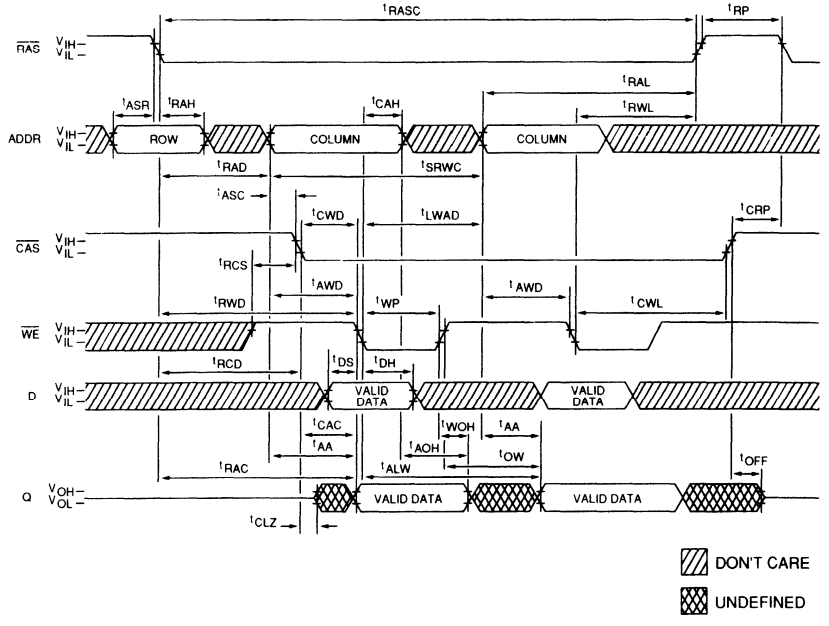
STATIC COLUMN READ CYCLE



STATIC COLUMN EARLY-WRITE CYCLE

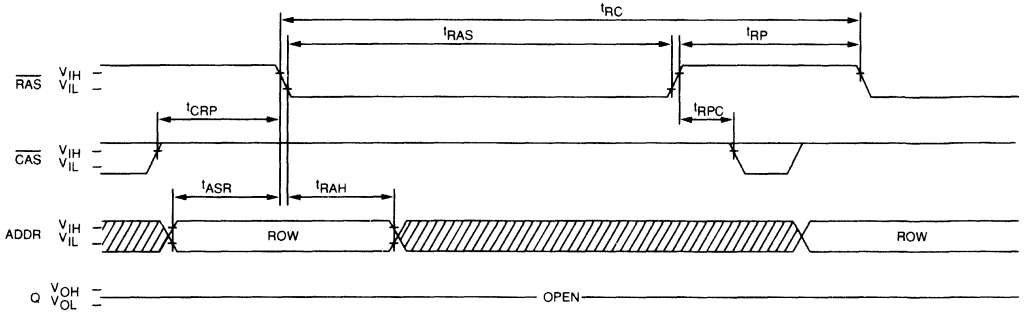


STATIC COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



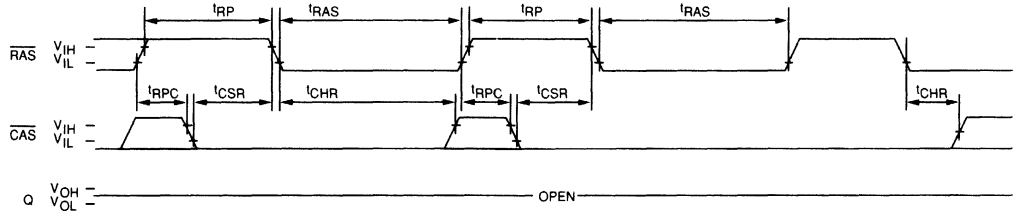
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_9; A_{10} and $\overline{WE}$ = DON'T CARE.)



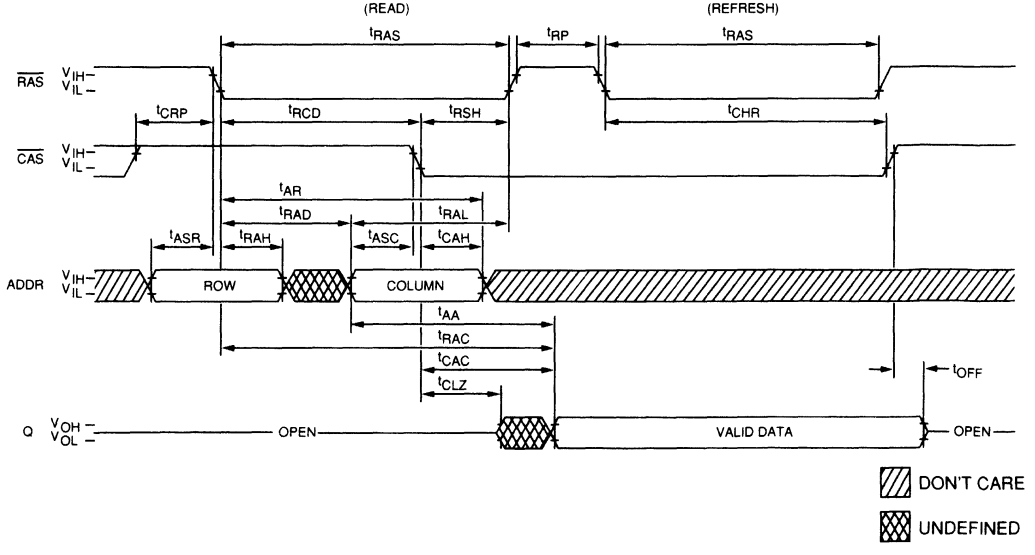
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_{10} and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[23]



DYNAMIC RAMs 1

DYNAMIC RAM MODULES 2

MULTIPORT DYNAMIC RAMs 3

STATIC RAMs 4

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CACHE DATA RAMs 6

FIFO MEMORIES 7

APPLICATION INFORMATION 8

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DRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package			Process	Page
				Standby	Active	SIP	SIMM	ZIP		
64K x 8	Page Mode	MT8068M,MN	100,120,150	45mw	450mw	30	30		NMOS	2-3
64K x 9	Page Mode	MT9068M,MN	100,120,150	45mw	450mw	30	30		NMOS	2-13
256K x 4	Page Mode (low profile)	MT4259M,MN	80,100,120,150	60mw	600mw	30	30		NMOS	2-23
256K x 5	Page Mode (low profile)	MT85259M,MN	80,100,120,150	75mw	750mw	30	30		NMOS	2-33
256K x 8	Page Mode (low profile)	MT8259DMN	80,100,120,150	135mw	1350mw	30	30		NMOS	2-43
256K x 8	Fast Page Mode (512 cycle/8ms)	MT8C8256M,MN	80,100,120	120mw	1200mw	30	30		CMOS	2-53
256K x 8	Page Mode	MT8259M,MN	80,100,120,150	120mw	1200mw	30	30		NMOS	2-63
256K x 9	Page Mode (low profile)	MT9259DMN	80,100,120,150	135mw	1350mw	30	30		NMOS	2-73
256K x 9	Page Mode (512 cycle/8ms)	MT8C9256M,MN	80,100,120	135mw	1350mw	30	30		C/NMOS	2-83
256K x 9	Page Mode	MT9259M,MN	80,100,120,150	135mw	1350mw	30	30		NMOS	2-93
256K x 36	Page Mode (512 cycle/8ms)	MT8C36256M,ZN	80,100,120	100mw	2000mw		72	72	C/NMOS	2-103
512K x 36	Page Mode (512 cycle/8ms)	MT8C36512DM,DZN	80,100,120	100mw	2000mw		72	72	C/NMOS	2-113
1MEG x 8	Fast Page Mode	MT8C8024M,MN	80,100,120,150	40mw	1400mw	30	30		CMOS	2-123
1MEG x 8	Fast Page Mode (low profile)	MT8C8024DMN	80,100,120	40mw	1400mw	30	30		CMOS	2-133
1MEG x 8	Nibble Mode	MT8C8025M,MN	80,100,120	45mw	1575mw	30	30		CMOS	2-143
1MEG x 8	Static Column	MT8C8026M,MN	80,100,120	45mw	1575mw	30	30		CMOS	2-153
1MEG x 9	Fast Page Mode	MT8C9024M,MN	80,100,120	45mw	1575mw	30	30		CMOS	2-163
1MEG x 9	Fast Page Mode (low profile)	MT8C9024DMN	80,100,120	45mw	1575mw	30	30		CMOS	2-173
1MEG x 9	Nibble Mode	MT8C9025M,MN	80,100,120	45mw	1575mw	30	30		CMOS	2-183
1MEG x 9	Static Column	MT8C9026M,MN	80,100,120	45mw	1575mw	30	30		CMOS	2-193

DRAM MODULE

64K x 8 DRAM

FEATURES

- Industry standard pin-out in a 30-pin single-in-line memory module
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 45mW standby; 450mW active, typical
- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

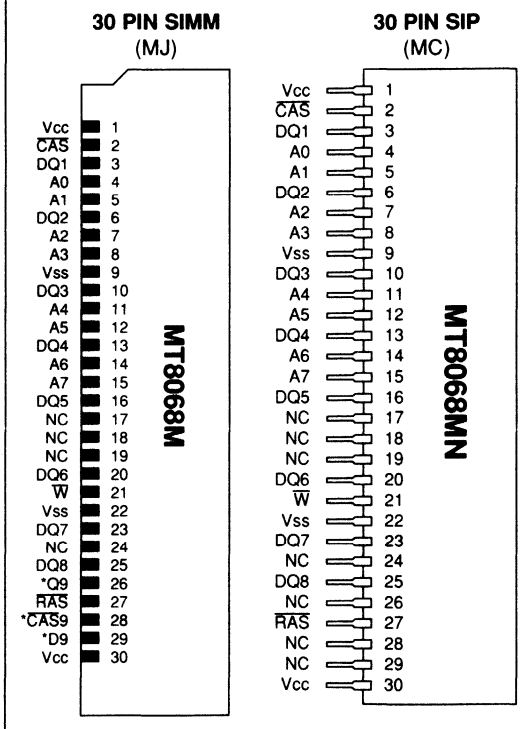
- Timing

80ns access	- 8
100ns access	-10
120ns access	-12
150ns access	-15

- Packages:

Leadless 30-pin SIMM	M
Leaded 30-pin SIP	MN

PIN ASSIGNMENT (Top View)

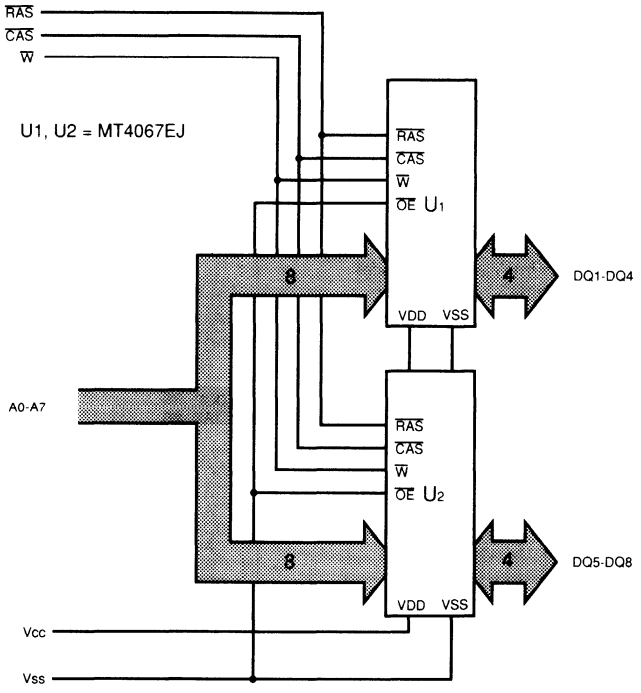


GENERAL DESCRIPTION

The MT8068M/MN is a randomly accessed solid-state memory containing 65,536 words organized in a x8 configuration. The 14 address bits are entered 7 bits at a time using $\overline{RAS}$ to latch the first 7 bits and $\overline{CAS}$ the latter 7 bits. If the $\overline{WE}$ pin goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open until the next $\overline{CAS}$ cycle.

By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined page boundary. Returning $\overline{RAS}$ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Function	RAS	CAS	WE	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 8 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts	I_I	-80	80	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-80	80	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	15	15	15	15	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	195	165	165	135	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	195	165	165	135	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	165	120	120	105	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	195	165	165	135	mA	2,19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_7	C_{I1}		15	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		24	pF	18
Input/Output Capacitance: DQ	C_{IO}		7	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

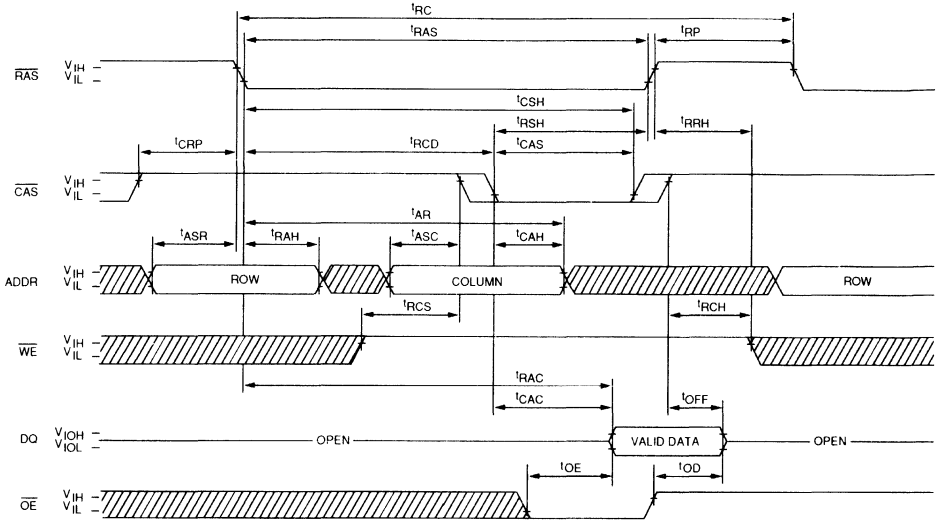
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	200		250		295		345		ns	
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
Output Enable	^tOE		25		25		30		40	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output butter turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
Output Disable	^tOD		25		30		30		35	ns	
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time reference to $\overline{RAS}$	^tDHR	35		60		65		70		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	50		70		90		110		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	90		120		150		185		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	22
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	21
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$) refresh	^tCSR	10		15		20		20		ns	21
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		0		ns	21

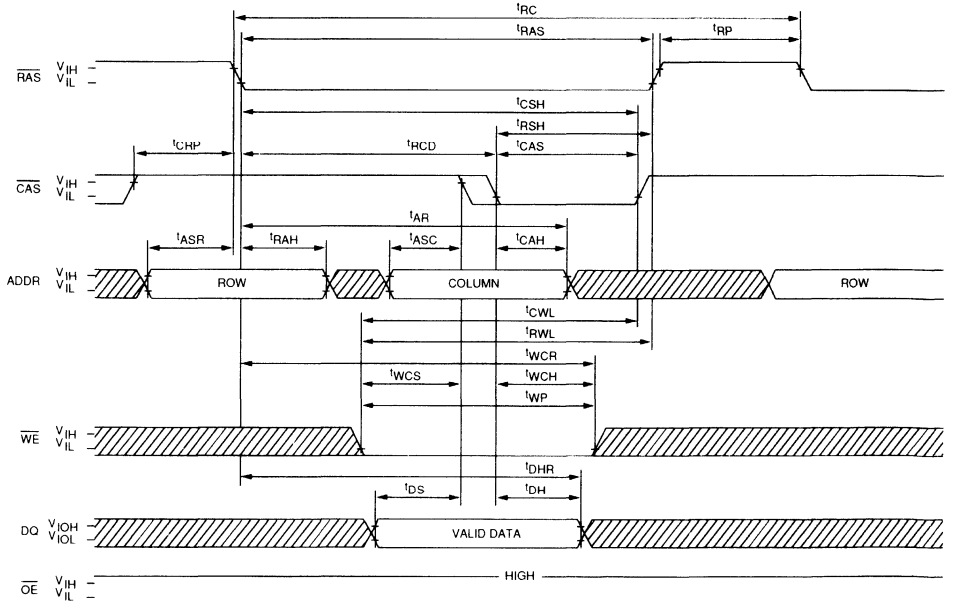
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \ge ^tCWD$ (min) and $^tRWD \ge ^tRWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. During a READ cycle if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, (V_{IH}) Q goes open. If $\overline{OE}$ is tied permanently LOW, a READ-MODIFY-WRITE operation is not possible.
21. On-chip refresh and address counters are enabled.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.

READ CYCLE



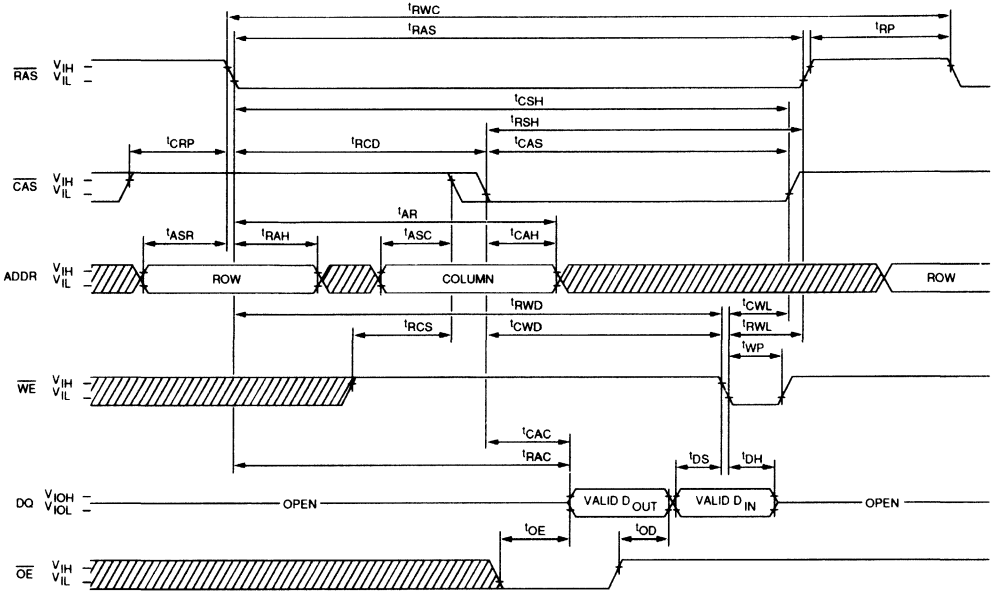
EARLY-WRITE CYCLE



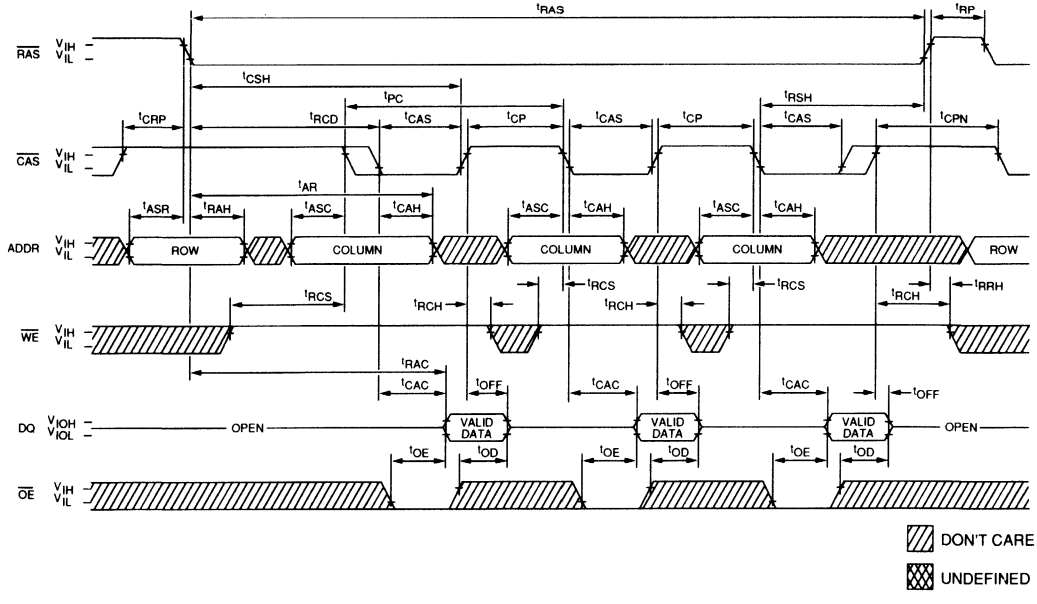
DON'T CARE

UNDEFINED

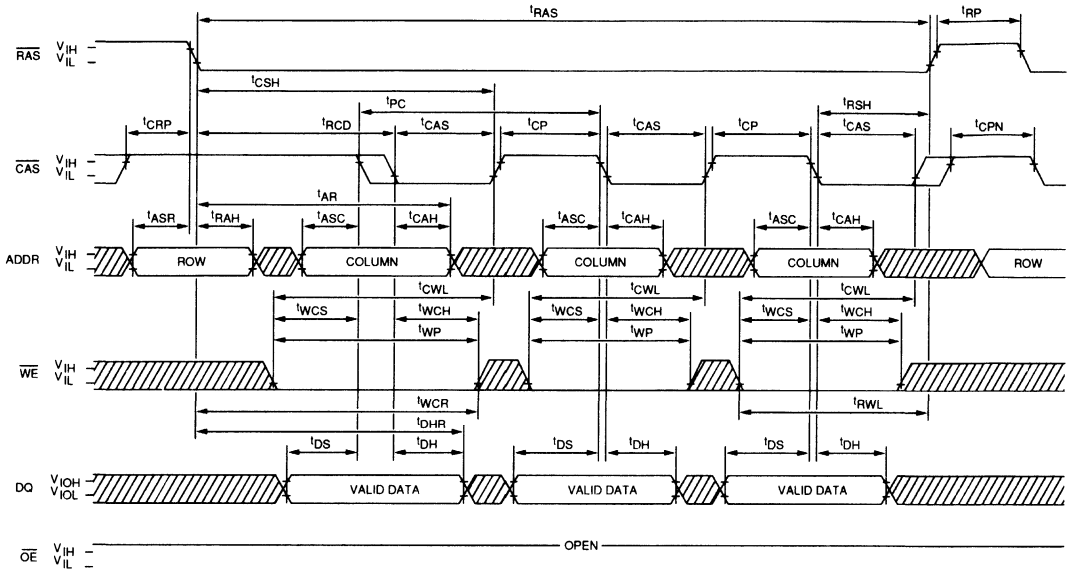
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE

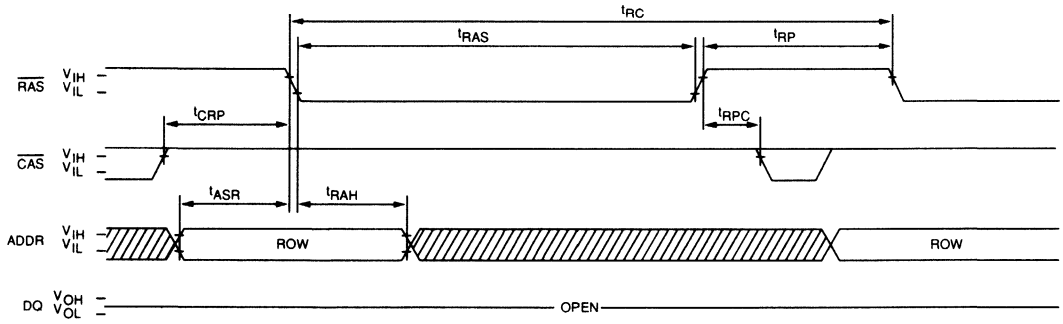


PAGE-MODE EARLY-WRITE CYCLE



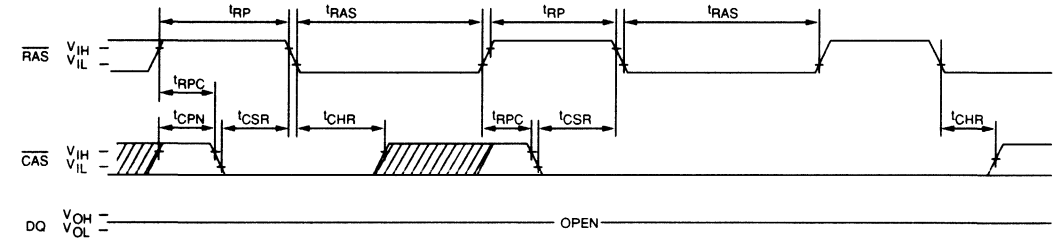
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; $\overline{WE}$ = DON'T CARE.)



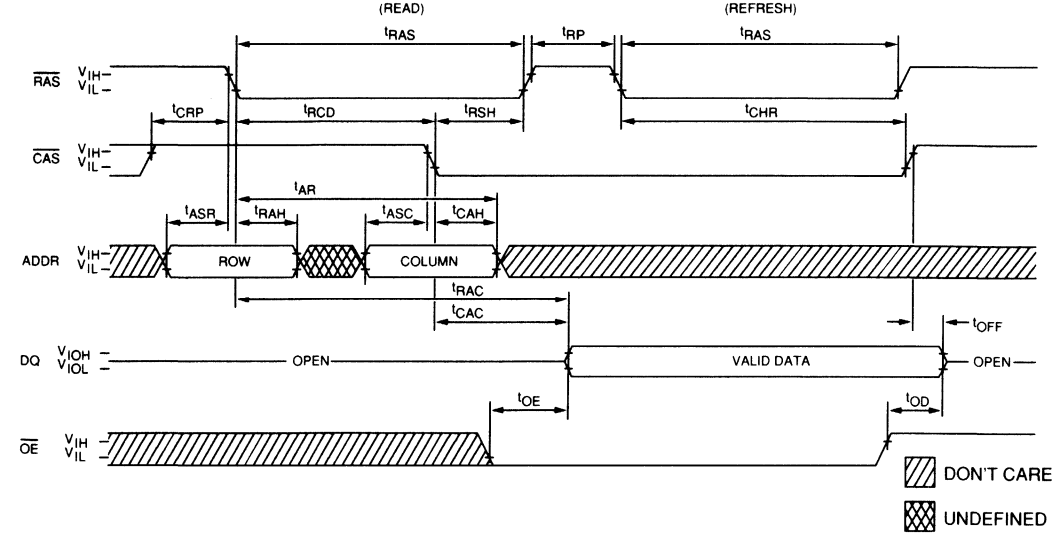
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_7, $\overline{WE}$, $\overline{OE}$ = DON'T CARE.)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[22]



DRAM MODULE

64K x 9 DRAM

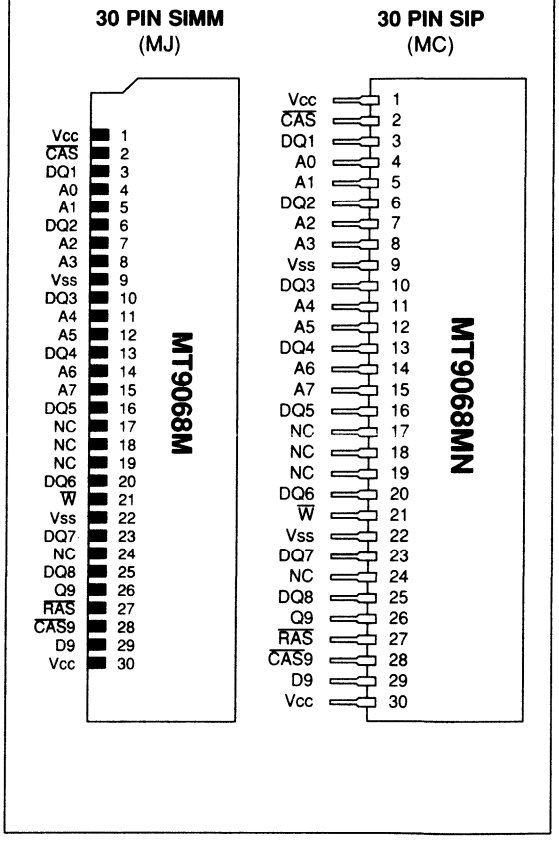
FEATURES

- Industry standard pin-out in a 30-pin single-in-line memory module
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 45mW standby; 450mW active, typical
- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS

	MARKING
• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
150ns access	-15
• Packages:	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	MN

PIN ASSIGNMENT (Top View)

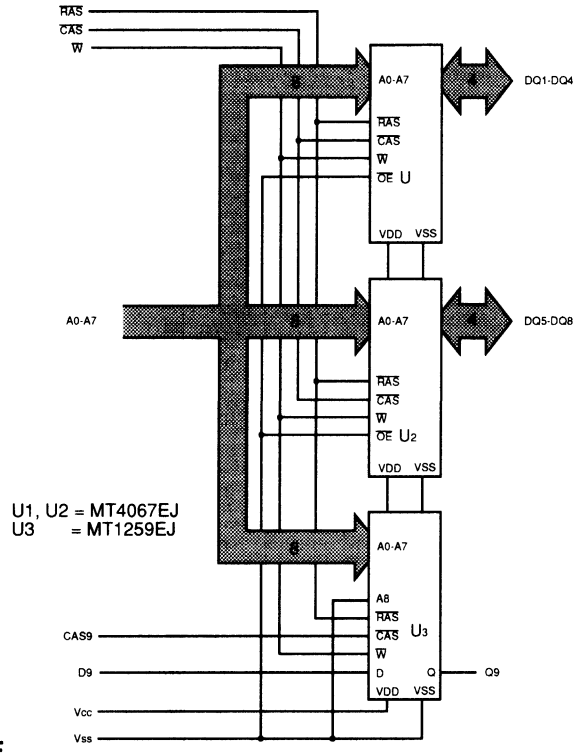


GENERAL DESCRIPTION

The MT9068M/MN is a randomly accessed solid-state memory containing 65,536 words organized in a x9 configuration. The 16 address bits are entered 8 bits at a time using $\overline{RAS}$ to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits. If the $\overline{WE}$ pin goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open until the next $\overline{CAS}$ cycle.

By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined page boundary. Returning $\overline{RAS}$ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



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PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 9 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts	I_I	-90	90	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-90	90	µA	
OUTPUT LEVELS Output High (Logic1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -8	MAX -10	MAX -12	MAX -15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	15	15	15	15	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	195	165	165	135	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	195	165	165	135	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	165	120	120	105	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	195	165	165	135	mA	2,19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: D	C_{I1}		7	pF	18
Input Capacitance: A_0-A_7	C_{I2}		15	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I3}		24	pF	18
Output Capacitance: Q	C_{O2}		7	pF	18
Input/Output Capacitance: DQ	C_{O1}		7	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

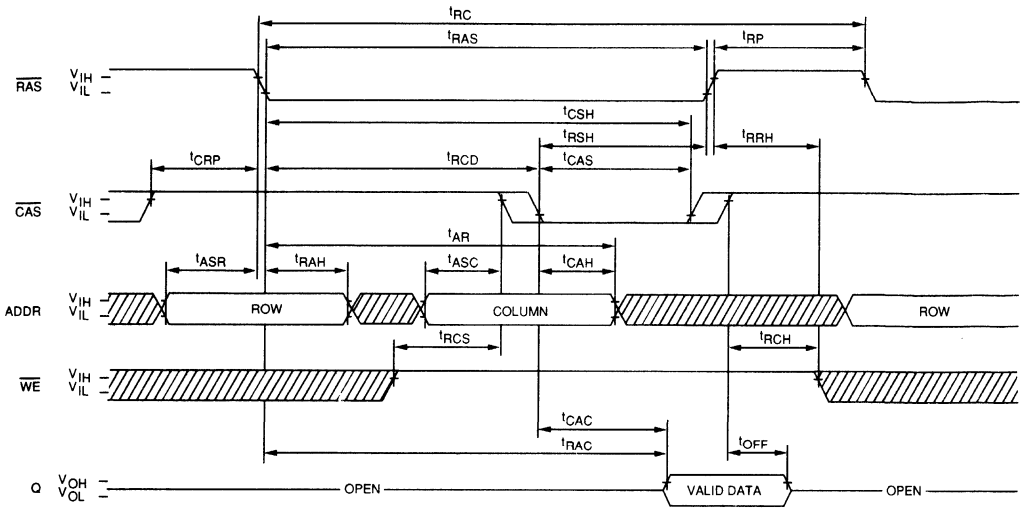
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	180		220		255		295		ns	
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	30		40		50		60		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	70		90		110		135		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	21
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	20
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$) refresh	^tCSR	10		15		20		20		ns	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		0		ns	20

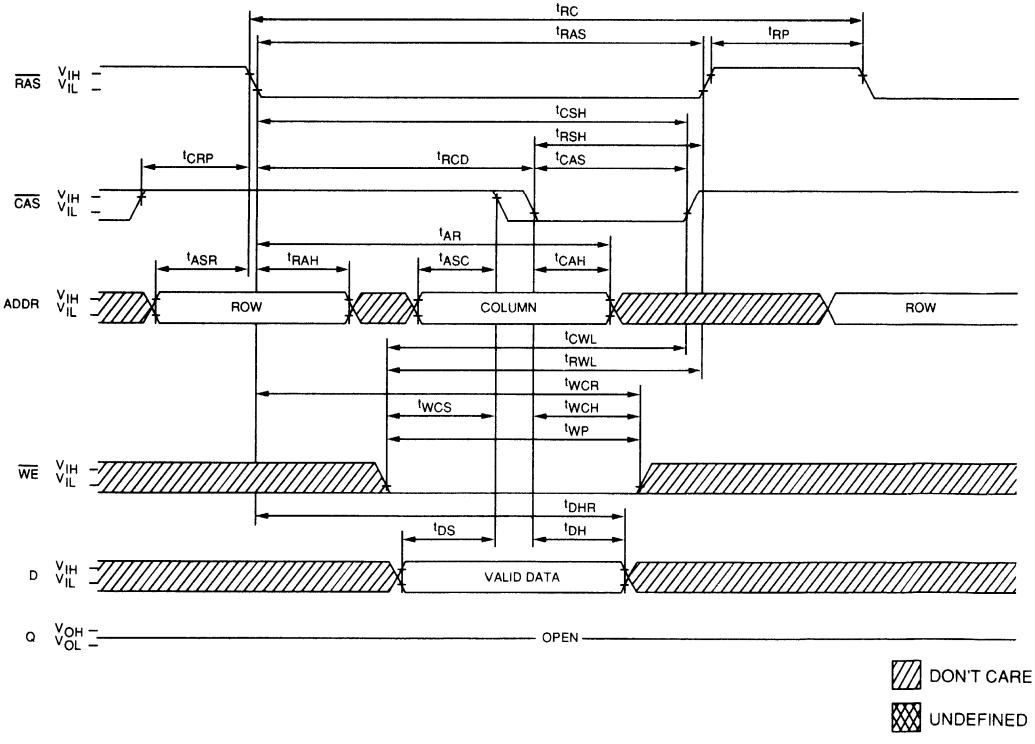
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq ^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \geq ^tCWD$ (min) and $^tRWD \geq ^tRWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. On-chip refresh and address counters are enabled.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

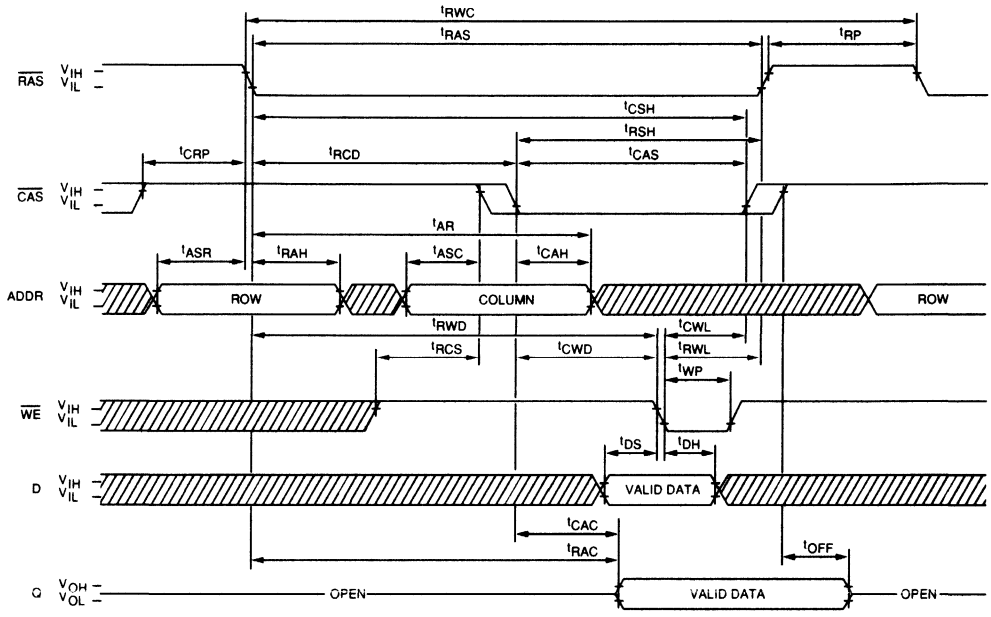
READ CYCLE



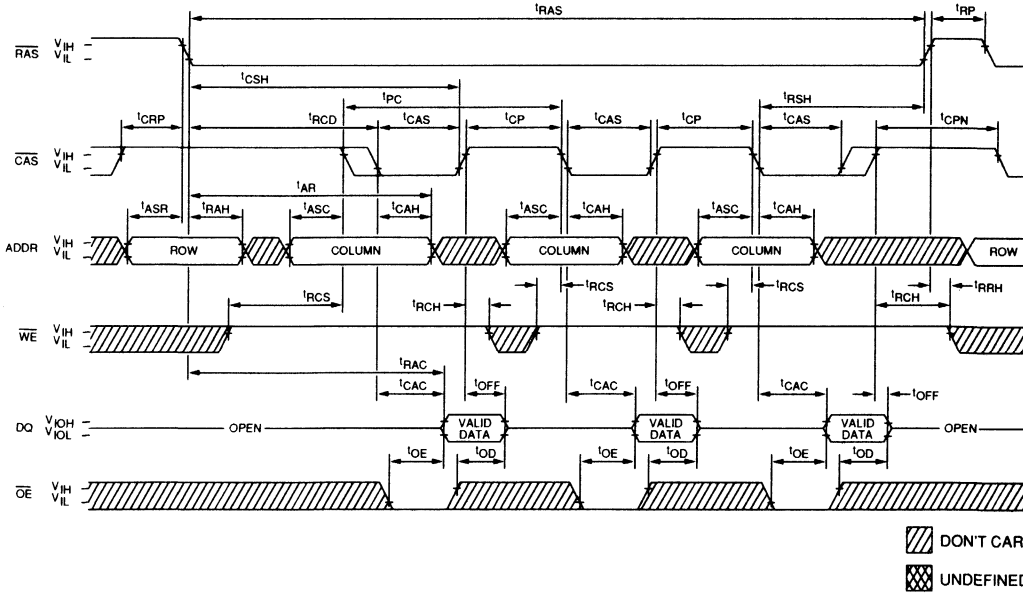
EARLY-WRITE CYCLE



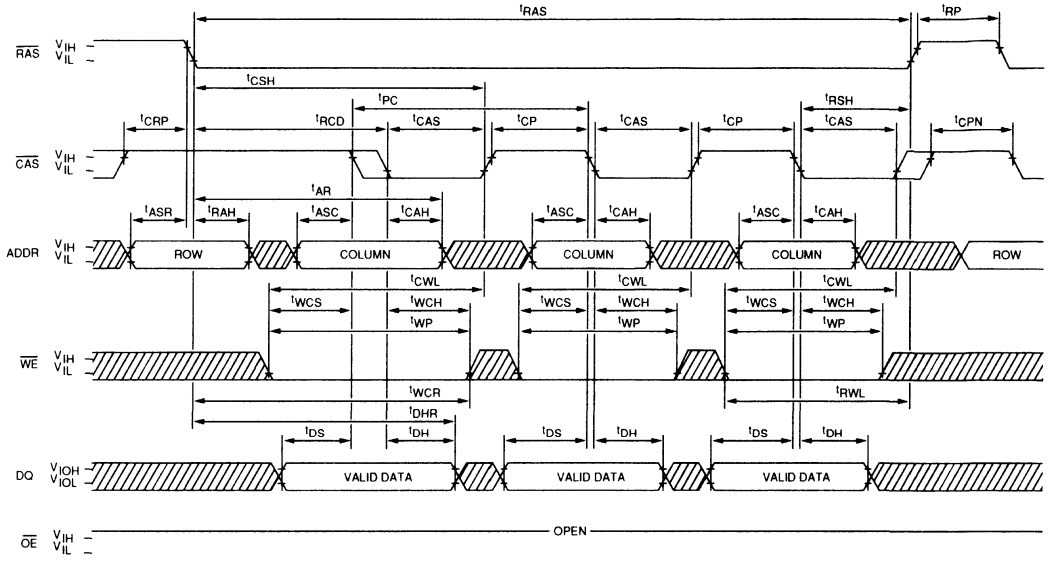
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE

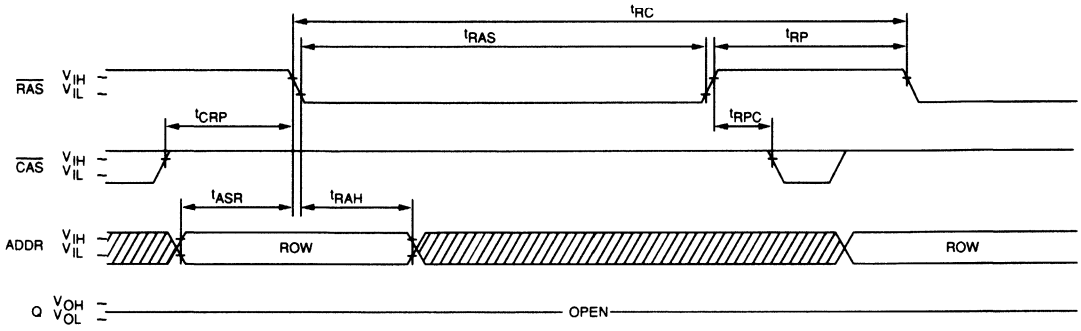


PAGE-MODE EARLY-WRITE CYCLE



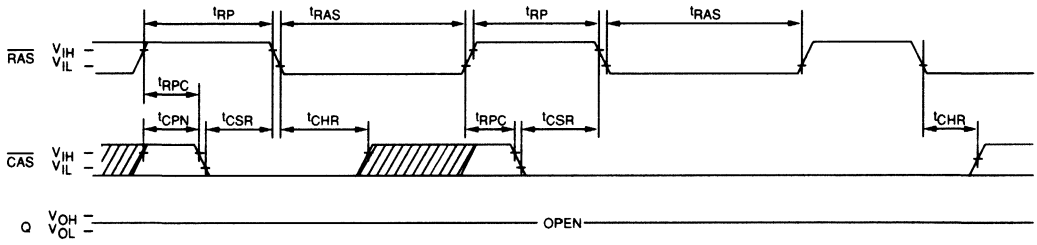
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



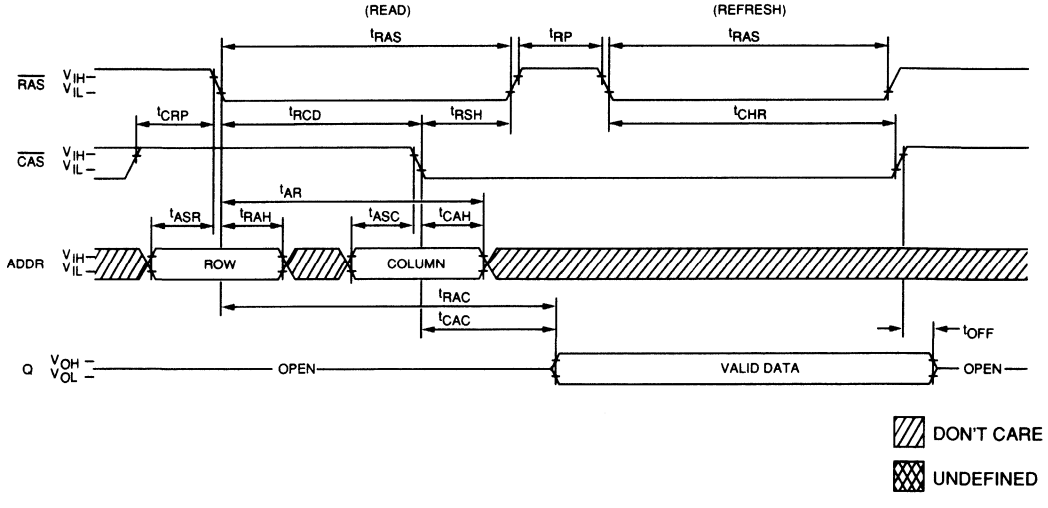
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8 and $\overline{WE}$ = DON'T CARE.)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[21]



DRAM MODULE

256K x 4 DRAM

LOW PROFILE

FEATURES

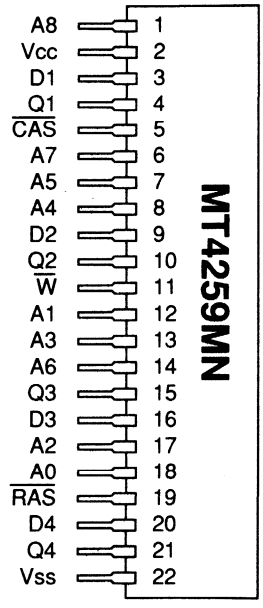
- Industry standard pin-out in a 22-pin single-in-line memory module
- Low profile
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 60mW standby; 600mW active, typical
- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
150ns access	-15
• Packages:	
Leaded 22-pin SIP	MN

PIN ASSIGNMENT (Top View)

22 PIN SIP
(MA)

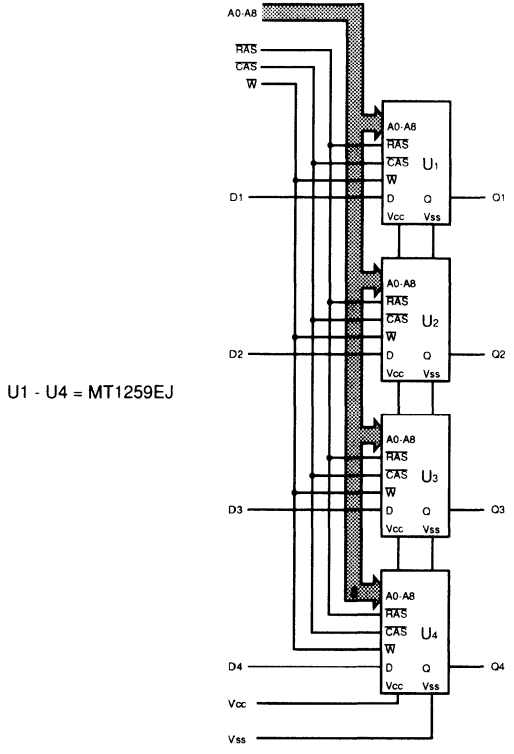


GENERAL DESCRIPTION

The MT4259MN is a randomly accessed solid-state memory containing 262,144 words organized in a x4 configuration. The 16 address bits are entered 8 bits at a time using $\overline{RAS}$ to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits. If the $\overline{WE}$ pin goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open until the next $\overline{CAS}$ cycle.

By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined page boundary. Returning $\overline{RAS}$ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



U1 - U4 = MT1259EJ

TRUTH TABLE

Function	RAS	CAS	WE	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 4 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts	I_I	-40	40	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-40	40	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	20	20	20	20	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	260	220	220	180	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	260	220	220	180	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	220	160	160	140	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	260	220	220	180	mA	2,19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		20	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		32	pF	18
Input Capacitance: D	C_{I3}		7	pF	18
Output Capacitance: Q	C_O		7	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

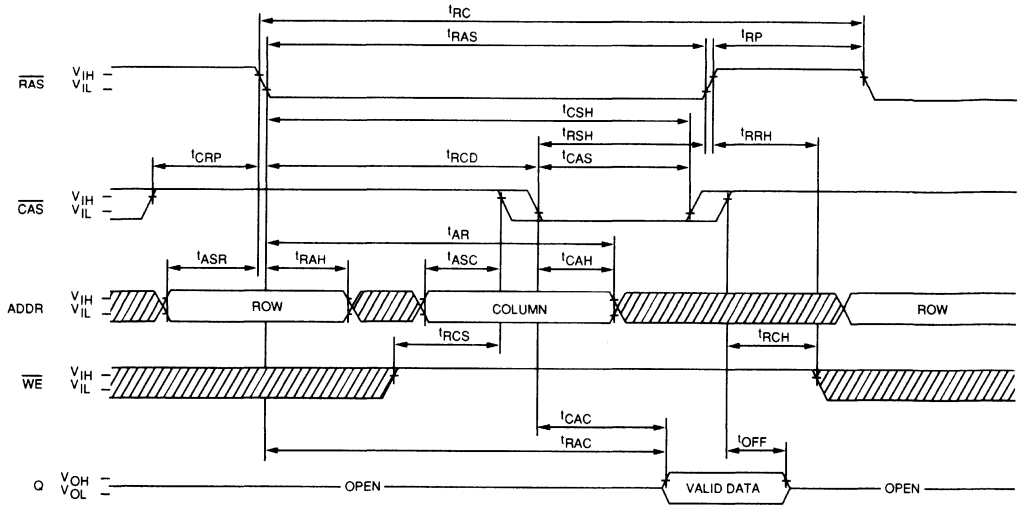
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	180		220		255		295		ns	
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	30		40		50		60		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	70		90		110		135		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	21
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	20
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$) refresh	^tCSR	10		15		20		20		ns	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		0		ns	20

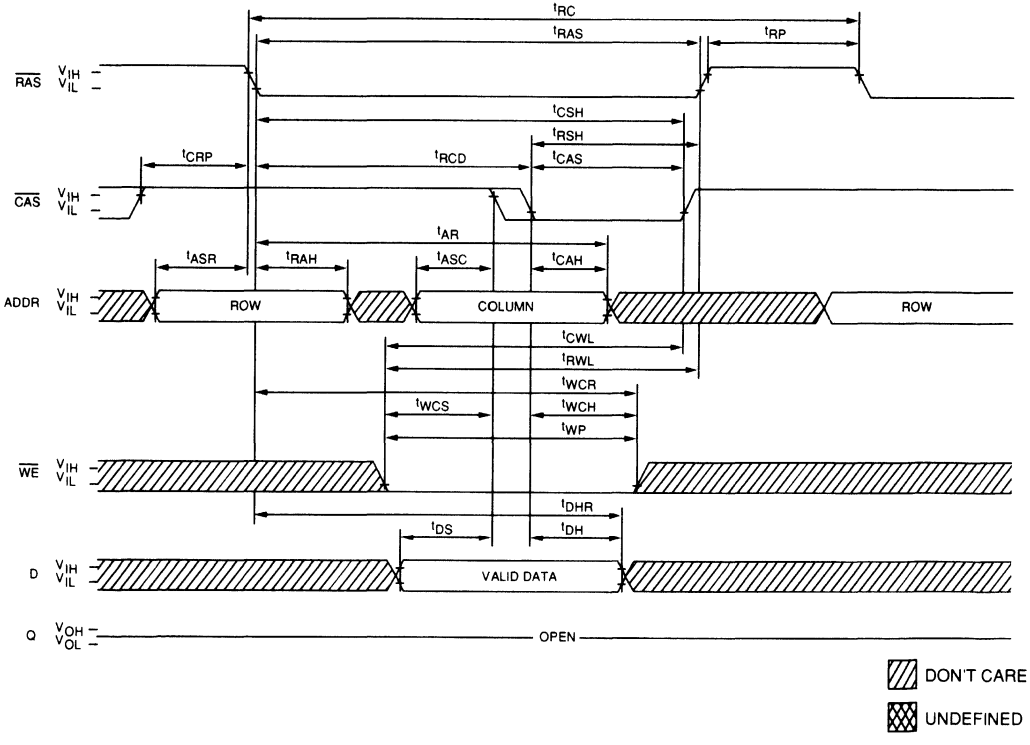
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \ge ^tCWD$ (min) and $^tRWD \ge ^tRWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. On-chip refresh and address counters are enabled.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

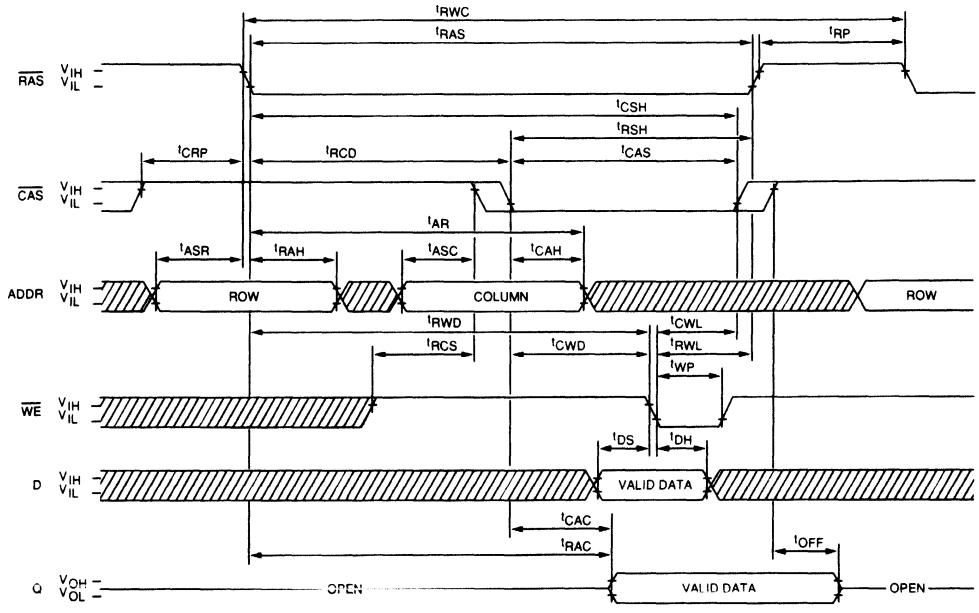
READ CYCLE



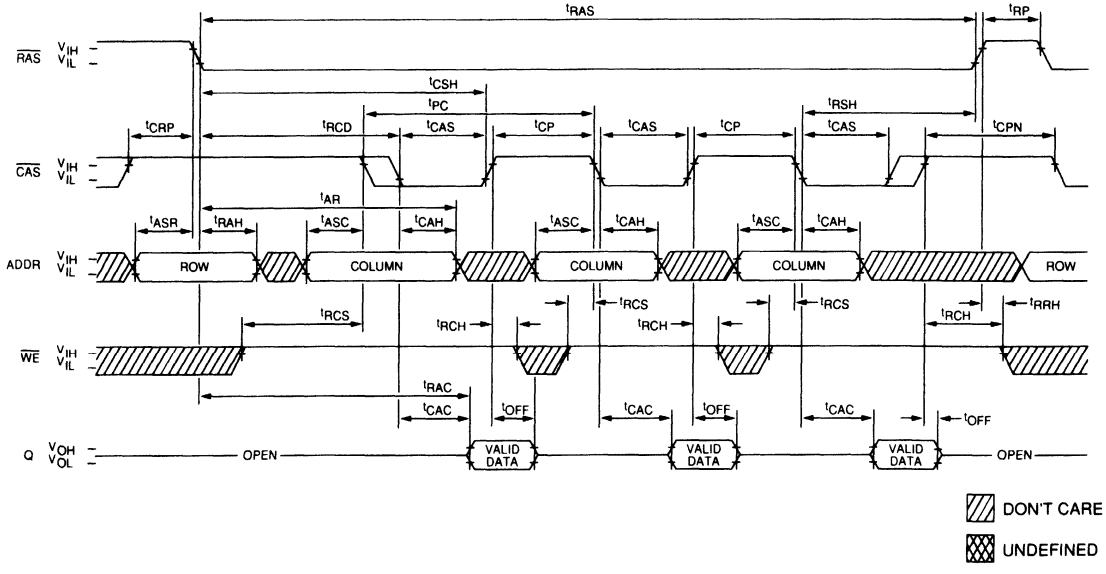
EARLY-WRITE CYCLE



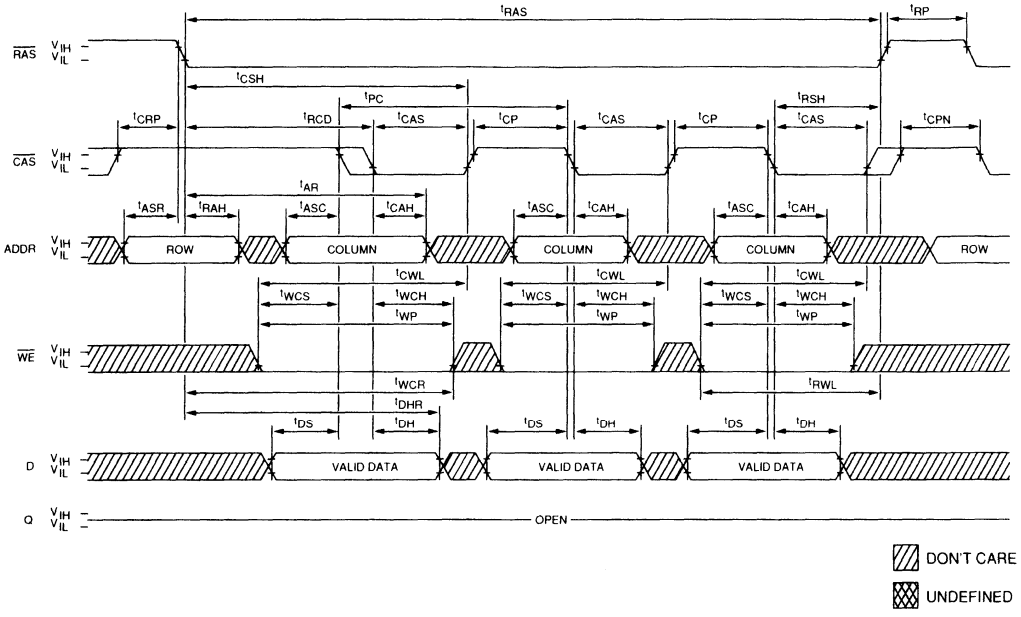
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE

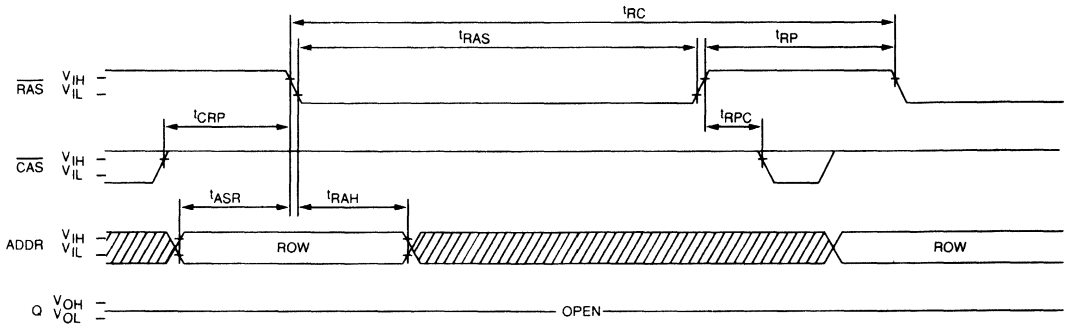


PAGE-MODE EARLY-WRITE CYCLE



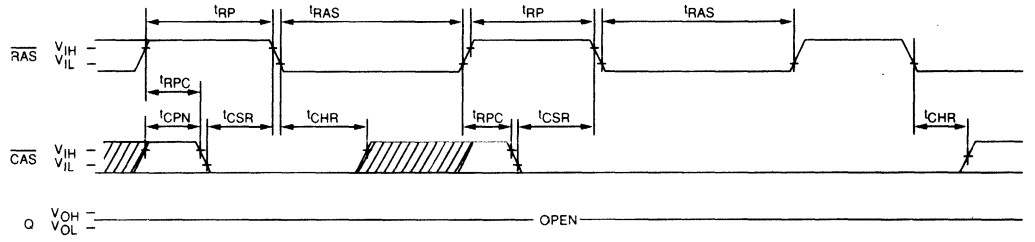
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



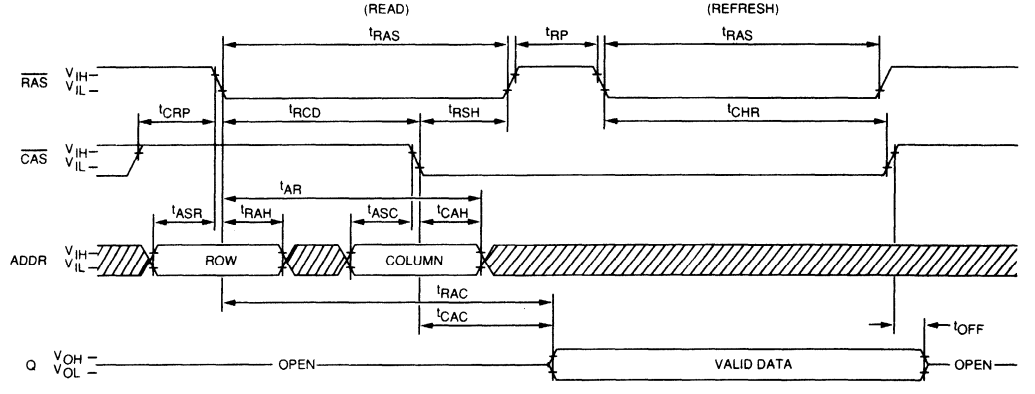
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8 and $\overline{WE}$ = DON'T CARE.)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[21]



DON'T CARE

UNDEFINED

DRAM MODULE

256K x 5 DRAM

LOW PROFILE

FEATURES

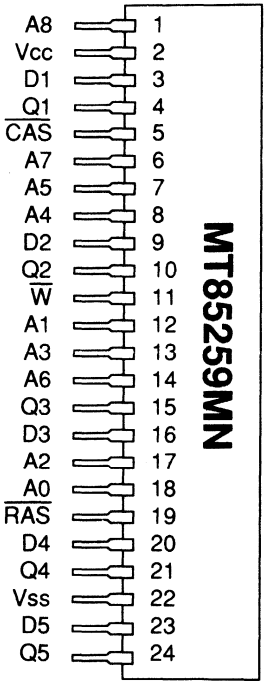
- Industry standard pin-out in a 24-pin single-in-line memory module
- Low profile (0.415 inch, typical)
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 75mW standby; 750mW active, typical
- On-board power supply decoupling capacitors (0.2µf) for low noise
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
150ns access	-15
• Packages:	
Leaded 24-pin SIP	MN

PIN ASSIGNMENT (Top View)

24 PIN SIP
(MB)

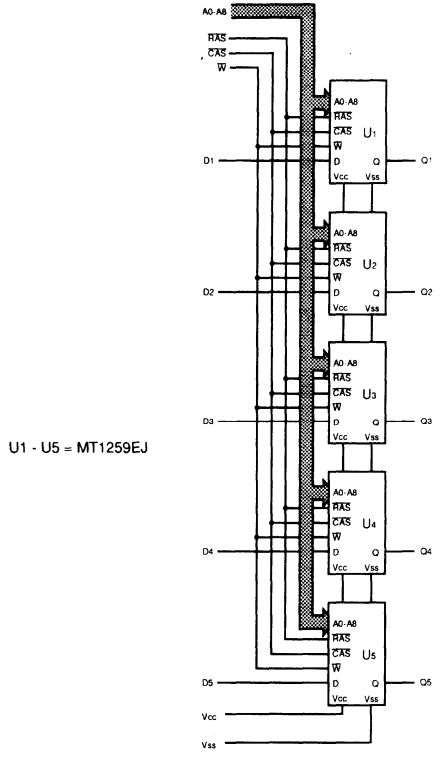


GENERAL DESCRIPTION

The MT85259MN is a randomly accessed solid-state memory containing 262,144 words organized in a x5 configuration. The 16 address bits are entered 8 bits at a time using $\overline{RAS}$ to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits. If the $\overline{WE}$ pin goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open until the next $\overline{CAS}$ cycle.

By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined page boundary. Returning $\overline{RAS}$ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



U1 - U5 = MT1259EJ

TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 5 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts	I_I	-50	50	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-50	50	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	25	25	25	25	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	325	275	275	225	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	325	275	275	225	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	275	200	200	175	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	325	275	275	225	mA	2,19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		25	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		40	pF	18
Input Capacitance: D	C_{I3}		7	pF	18
Output Capacitance: Q	C_O		7	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

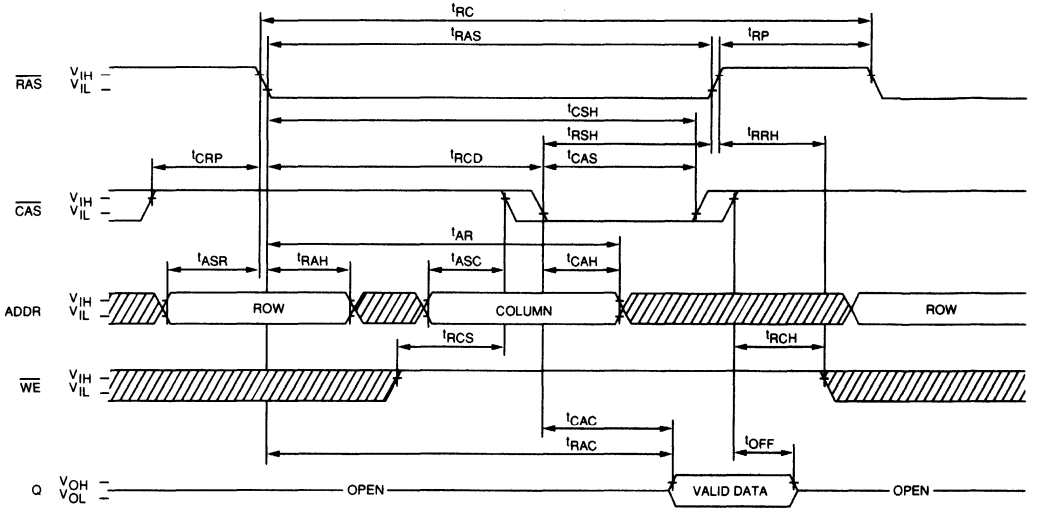
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	180		220		255		295		ns	
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	30		40		50		60		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	70		90		110		135		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	21
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	20
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$) refresh	^tCSR	10		15		20		20		ns	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		0		ns	20

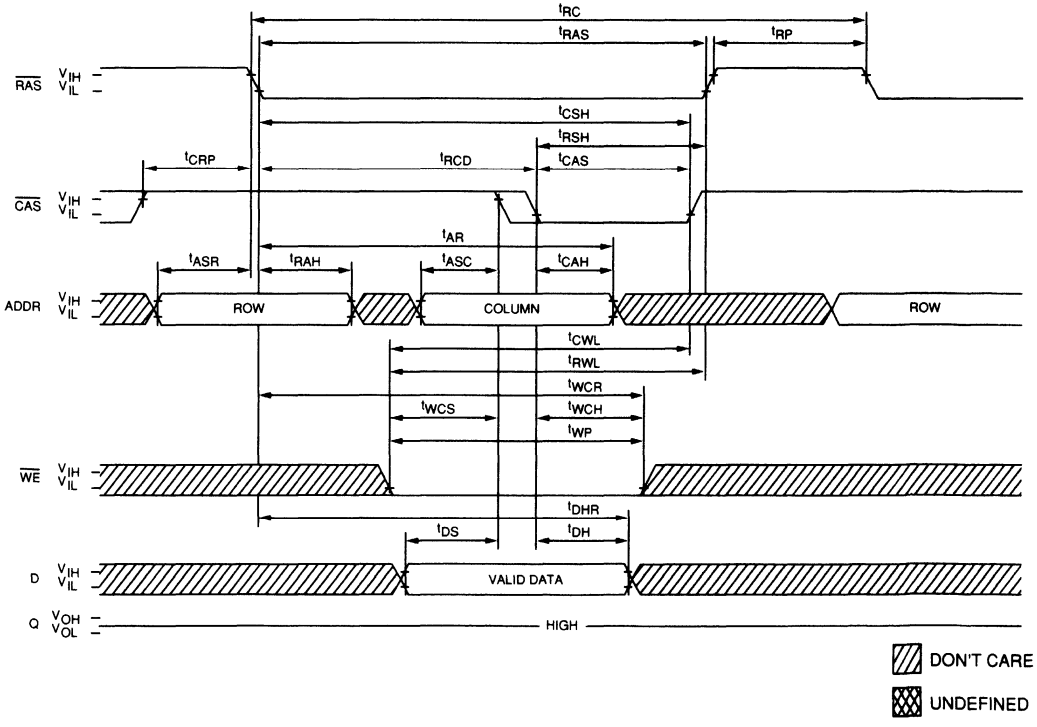
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge {}^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \ge {}^tCWD$ (min) and $^tRWD \ge {}^tRWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. On-chip refresh and address counters are enabled.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

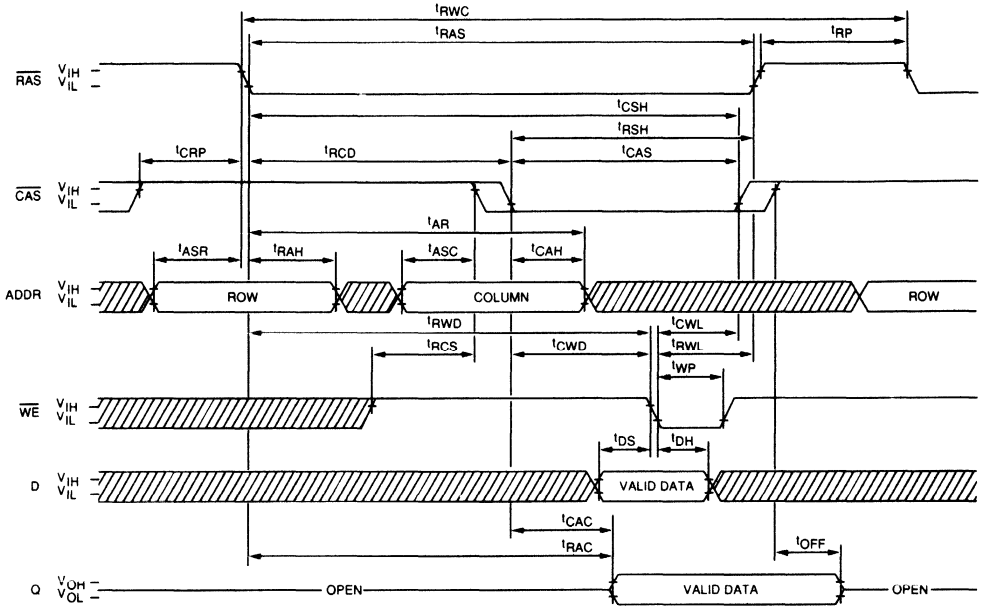
READ CYCLE



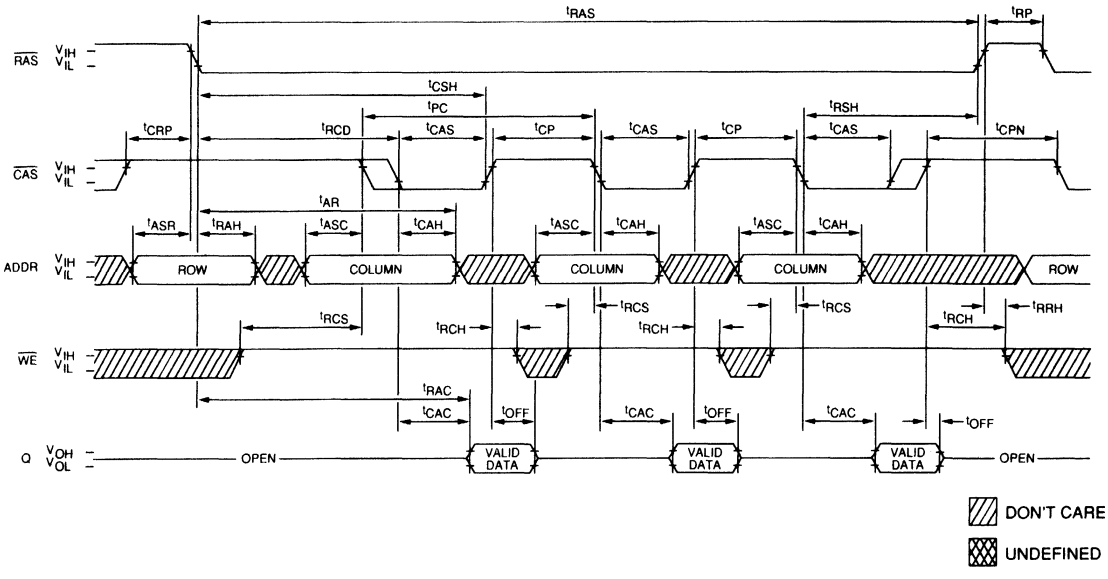
EARLY-WRITE CYCLE



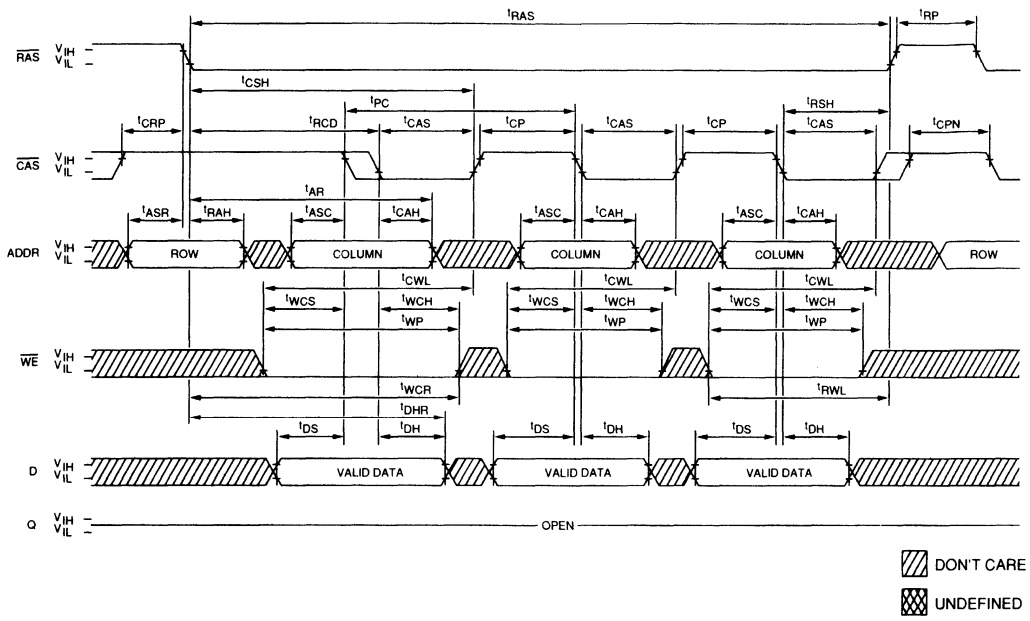
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE

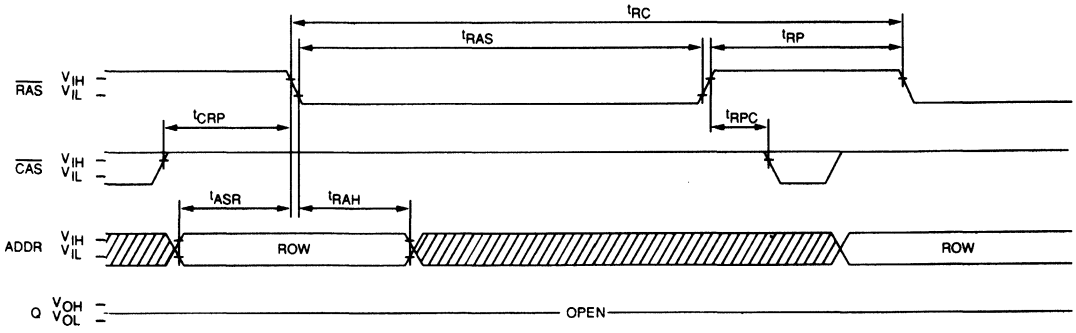


PAGE-MODE EARLY-WRITE CYCLE



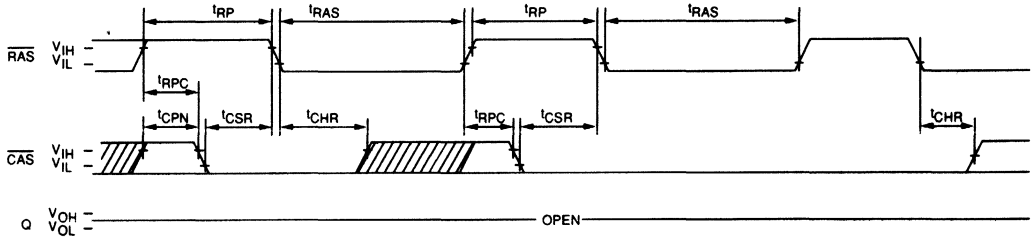
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



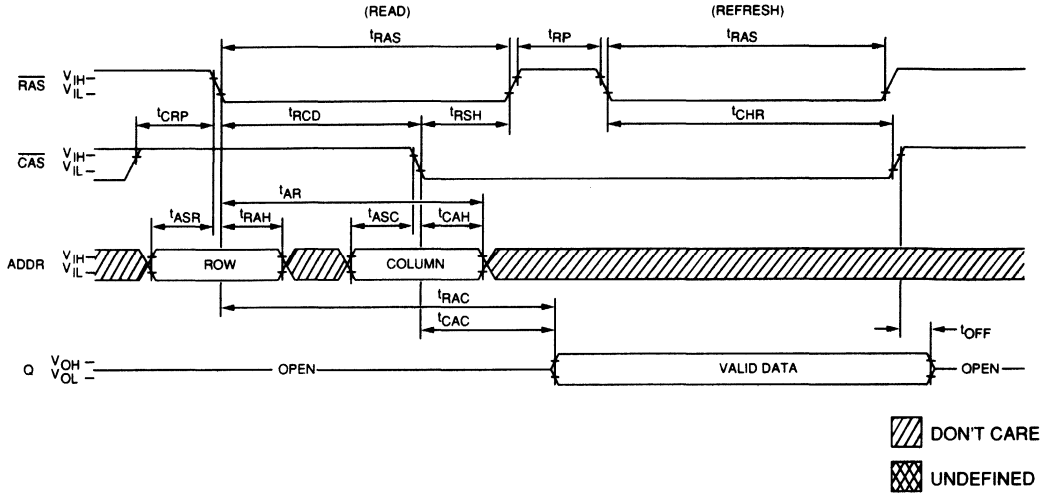
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8, $\overline{WE}$ = DON'T CARE.)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[21]



DRAM MODULE

256K x 8 DRAM

LOW PROFILE

FEATURES

- Industry standard pin-out in a 30-pin single-in-line package
- Low profile, double-side mount (0.45 in)
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 135mW standby; 1350mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

- Timing

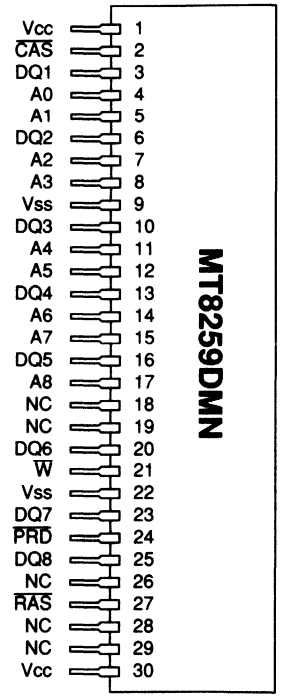
80ns access	- 8
100ns access	-10
120ns access	-12
150ns access	-15

- Packages:

Leaded 30-pin SIP (low profile)	DMN

PIN ASSIGNMENT (Top View)

30 PIN SIP
(ME)

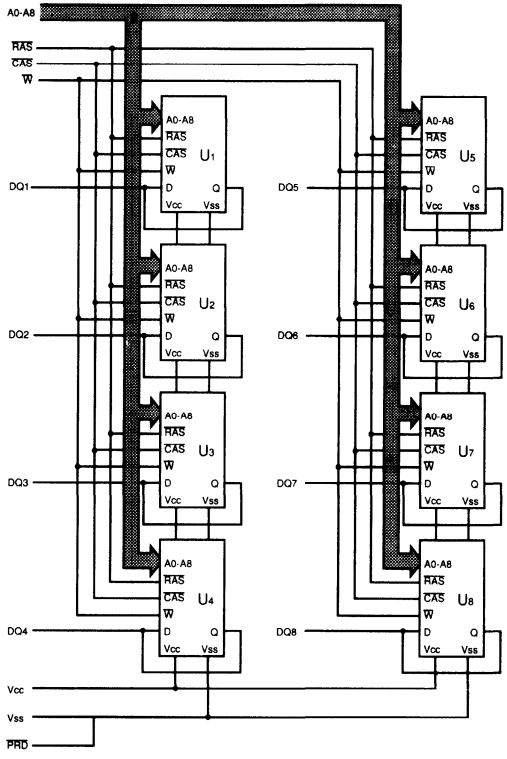


GENERAL DESCRIPTION

The MT8259 is a randomly accessed solid-state memory containing 262,144 bits organized in a x8 configuration. The 18 address words are entered 9 bits at a time using $\overline{RAS}$ to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. If the $\overline{WE}$ pin goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open until the next $\overline{CAS}$ cycle.

By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined page boundary. Returning $\overline{RAS}$ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4 ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



U1 - U8 = MT1259EJ

TRUTH TABLE

Function	RAS	CAS	WE	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 8 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts	I_I	-80	80	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-80	80	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	40	40	40	40	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	500	440	440	360	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	520	440	440	360	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	440	320	320	280	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	520	440	440	360	mA	2,19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		40	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		64	pF	18
Input/Output Capacitance: DQ	C_{IO}		12	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

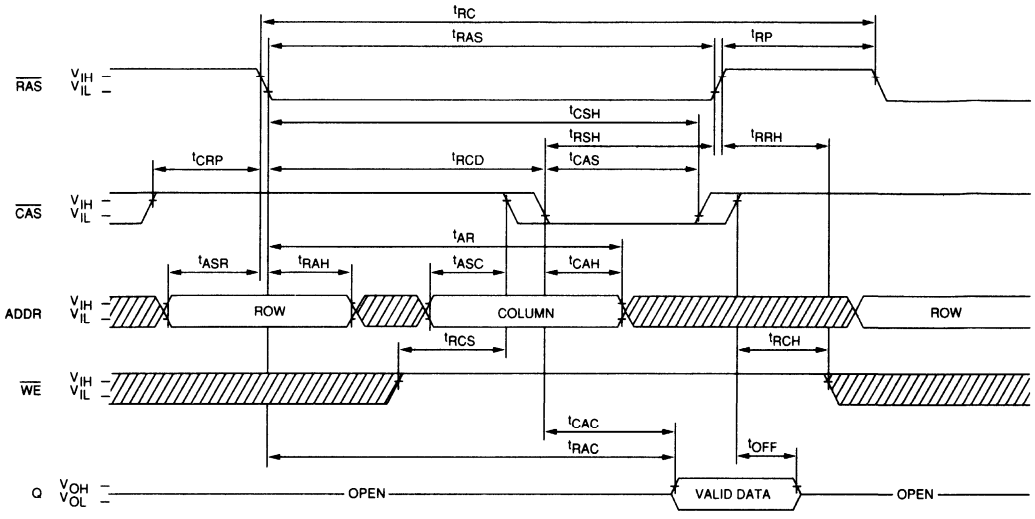
(Notes: 3, 4, 5, 10, 11, 17, 18) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	180		220		255		295		ns	
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	30		40		50		60		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	70		90		110		135		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	21
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	20
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$) refresh	^tCSR	10		15		20		20		ns	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		0		ns	20

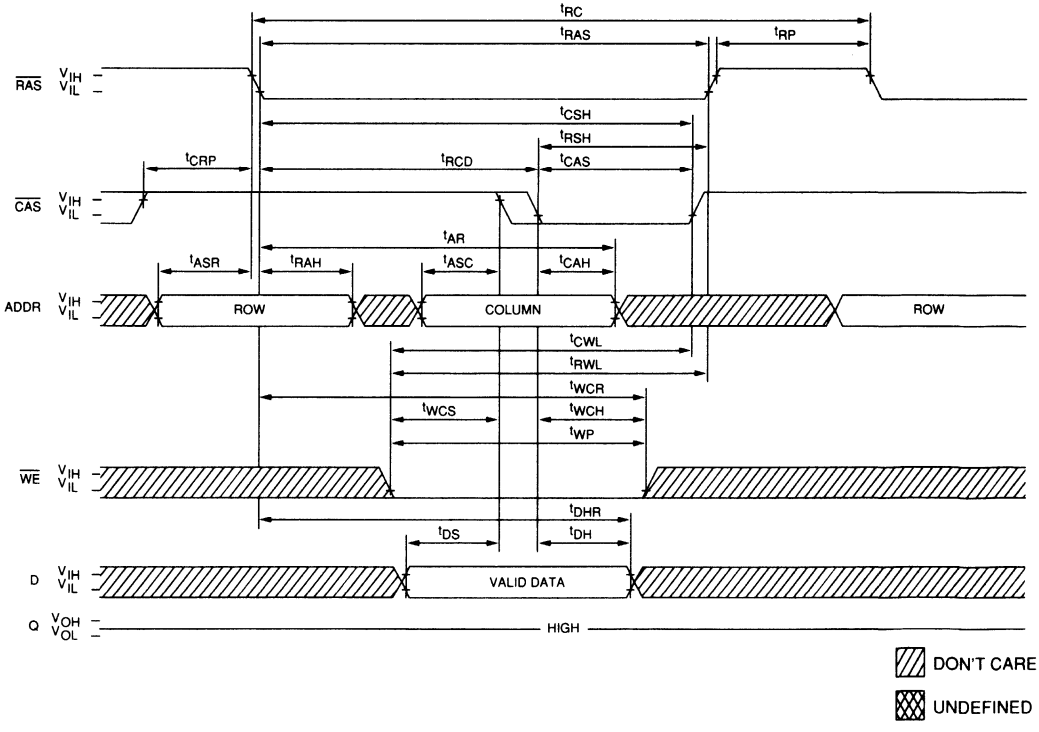
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \ge ^tCWD$ (min) and $^tRWD \ge ^tRWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. On-chip refresh and address counters are enabled.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

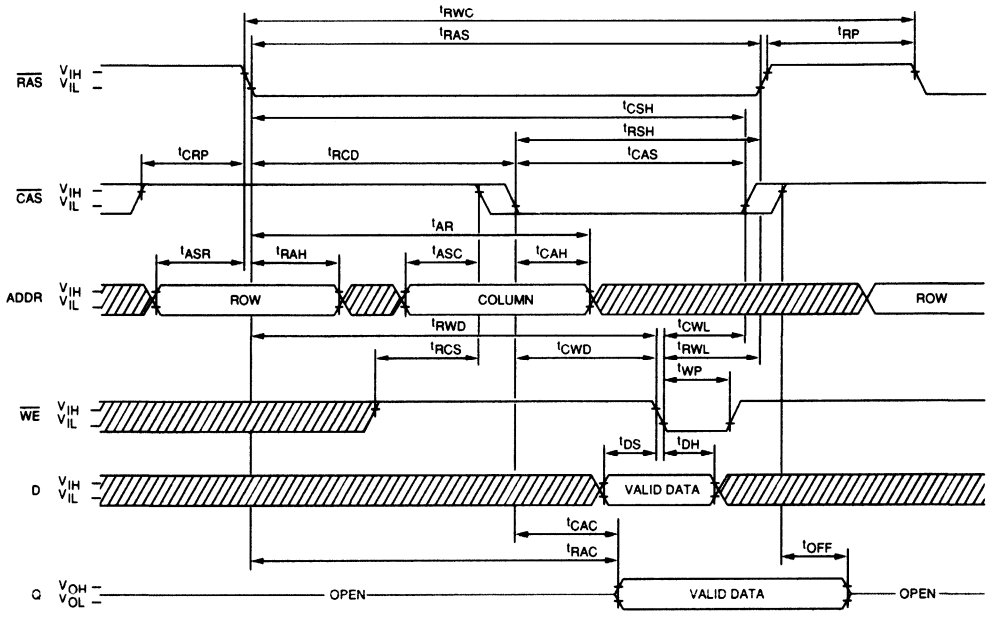
READ CYCLE



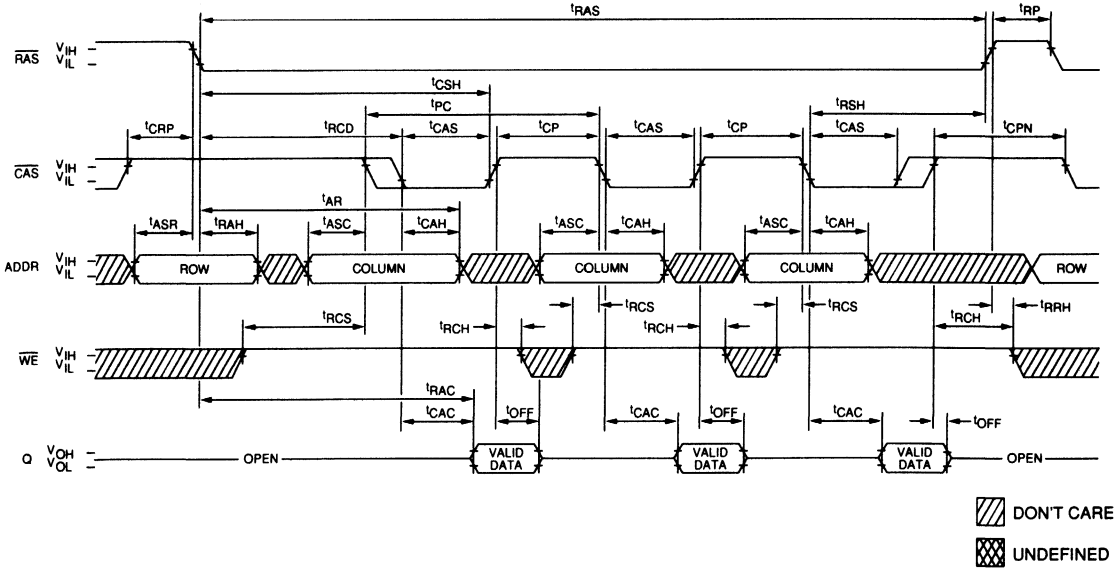
EARLY-WRITE CYCLE



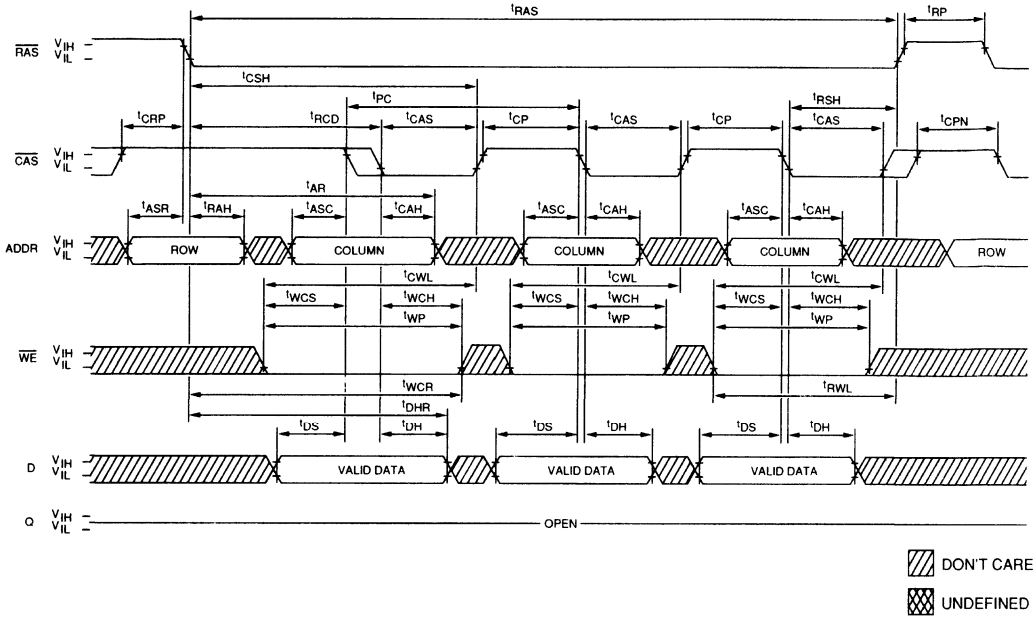
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE

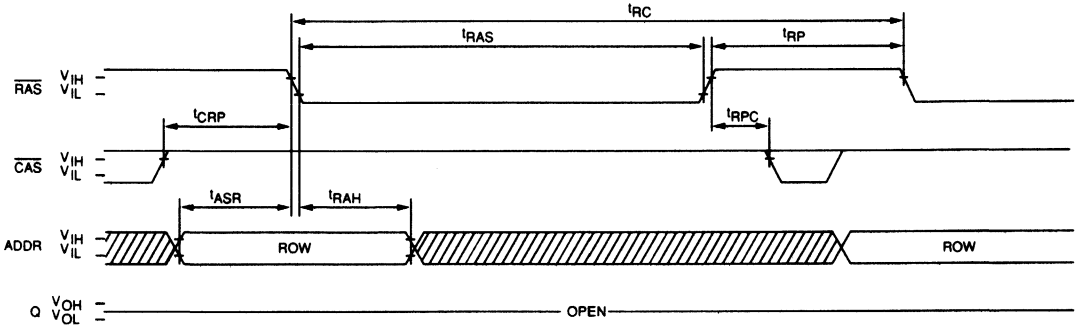


PAGE-MODE EARLY-WRITE CYCLE



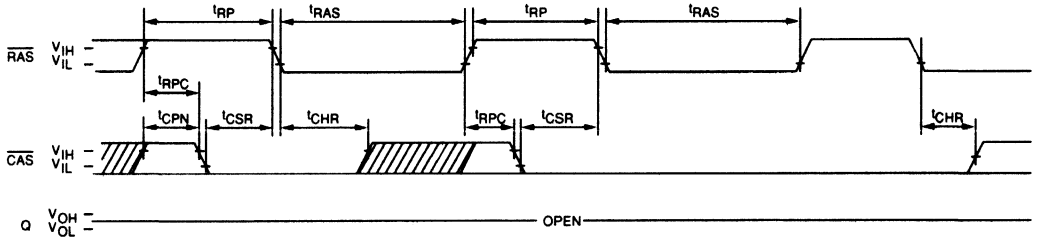
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



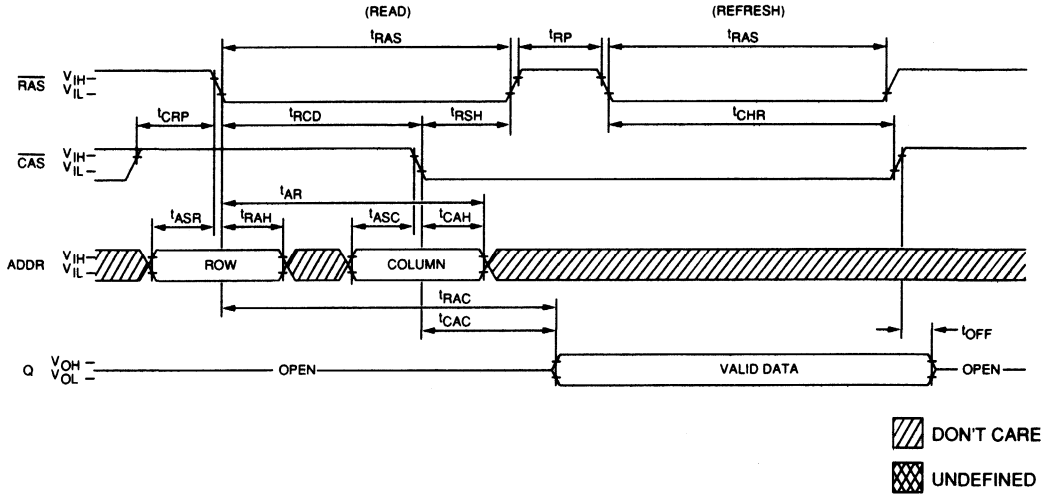
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8, $\overline{WE}$ = DON'T CARE.)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[21]



DRAM MODULE

256K x 8 DRAM

REFRESH: 512 CYCLE/8MS

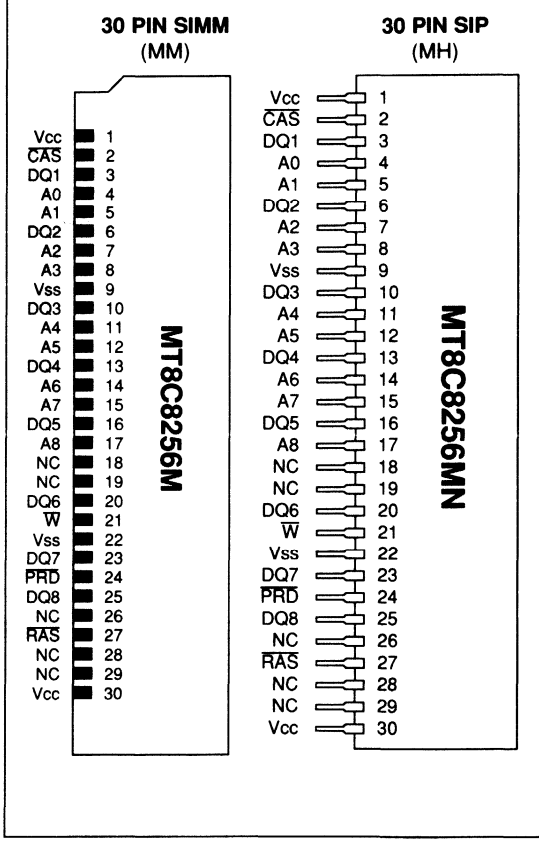
FEATURES

- Industry standard pin-out in a 30-pin single-in-line memory module
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 120mW standby; 1200mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional Fast Page Mode access cycle
- 512 cycle refresh distributed across 8ms

OPTIONS MARKING

• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages:	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	MN

PIN ASSIGNMENT (Top View)



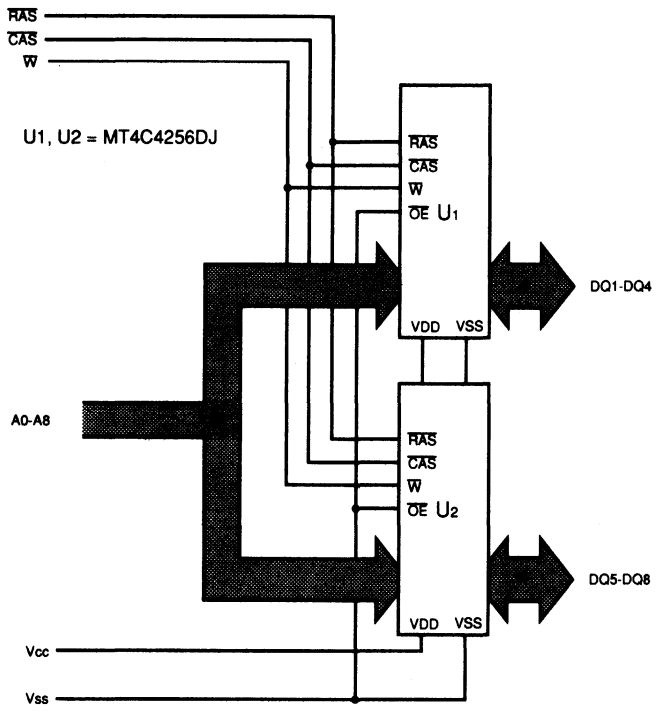
GENERAL DESCRIPTION

The MT8C8256 is a randomly accessed solid-state memory containing 262,144 words organized in a x8 configuration. The 18 address bits are entered 9 bits at a time using $\overline{RAS}$ to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. If the $\overline{WE}$ pin goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open until the next $\overline{CAS}$ cycle.

By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined page boundary. Returning $\overline{RAS}$ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time.

Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (refresh) cycle so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8 ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Function	RAS	CAS	WE	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 8 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts	I_I	-20	20	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-20	20	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	6	4	4	4	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	140	120	100	80	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	100	80	60	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	140	120	100	80	mA	3, 4
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	140	120	100	80	mA	3, 4

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		10	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		14	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	160		190		220		ns	
READ-WRITE cycle time	^tRWC	215		220		295		ns	
FAST PAGE MODE READ or WRITE cycle time	^tPC	45		55		70		ns	
FAST PAGE MODE READ-WRITE cycle time	^tPRWC	100		115		140		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		30	ns	15
Output Enable	^tOE		20		25		30	ns	
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		55		65	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		25		35		ns	
$\overline{RAS}$ precharge time	^tRP	70		80		90		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	35	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	15		15		20		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	25	75	25	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	12		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	17	40	20	50	20	60	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		85		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

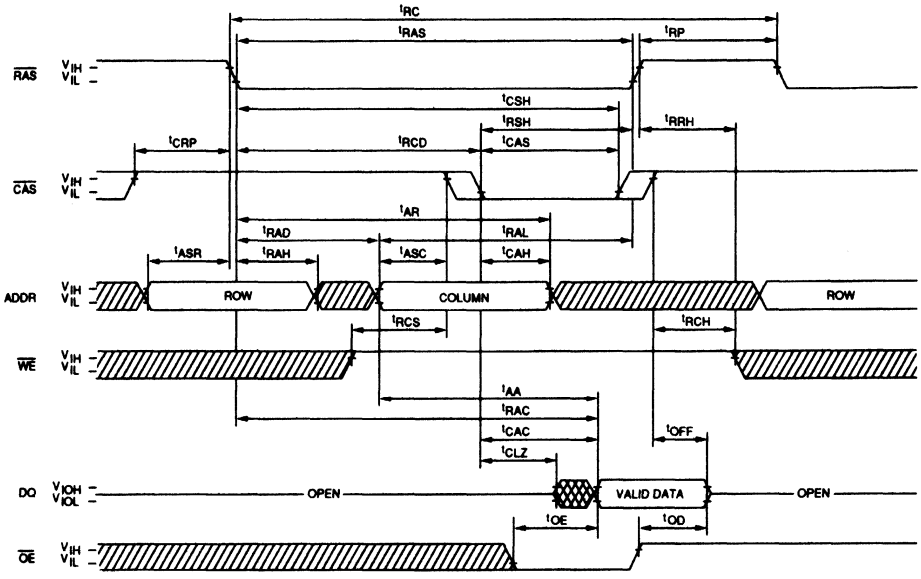
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	^tOFF	0	20	0	20	0	35	ns	20
Output Disable	^tOD		20		20		35	ns	
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		85		ns	
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		25		30		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	20		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	110		130		160		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	70		80		100		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	55		65		75		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5

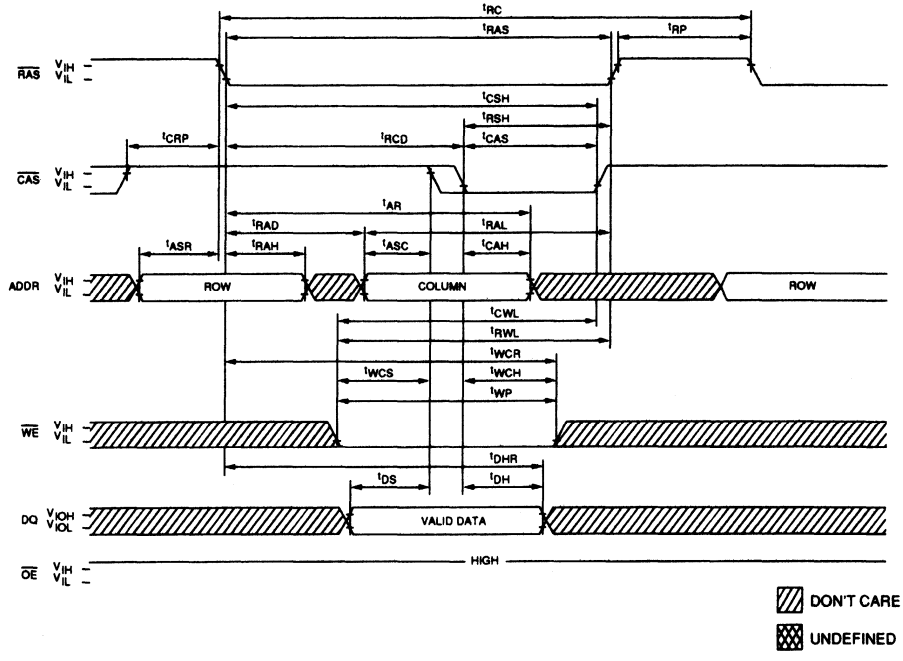
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \ge {}^tRWD$ (min), $^tAWD \ge {}^tAWD$ (min) and $^tCWD \ge {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW a READ-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
25. All other inputs at Vcc -0.2V.

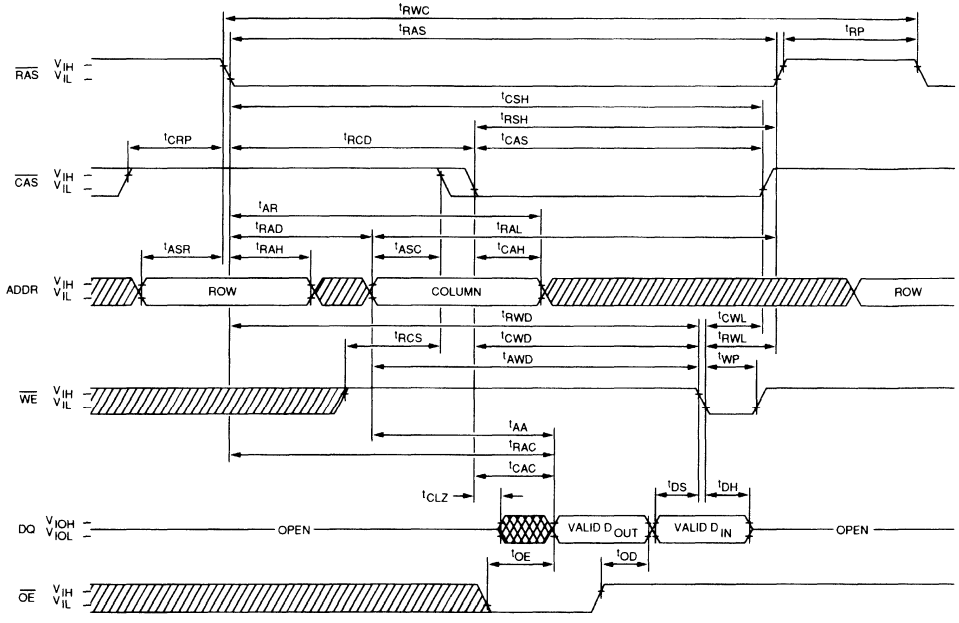
READ CYCLE



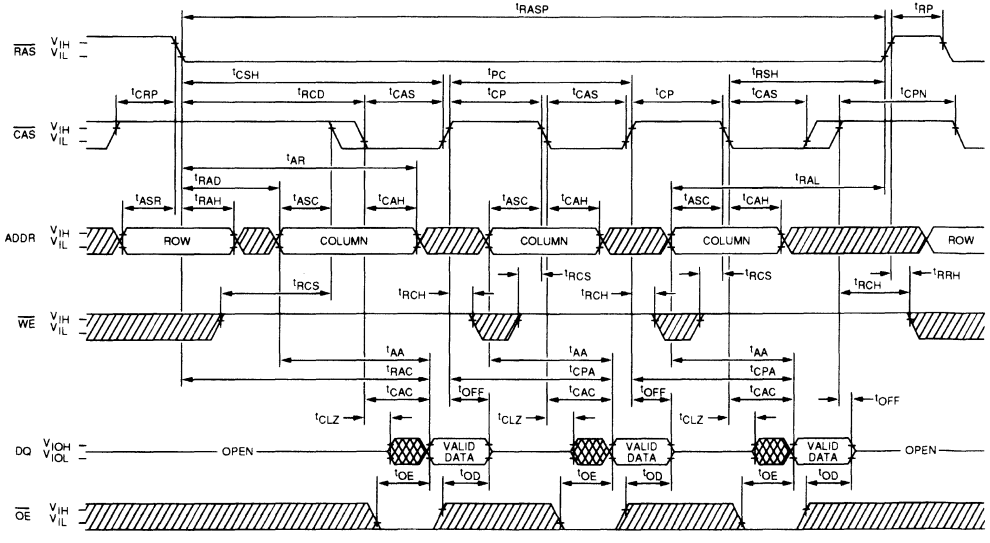
EARLY-WRITE CYCLE



READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



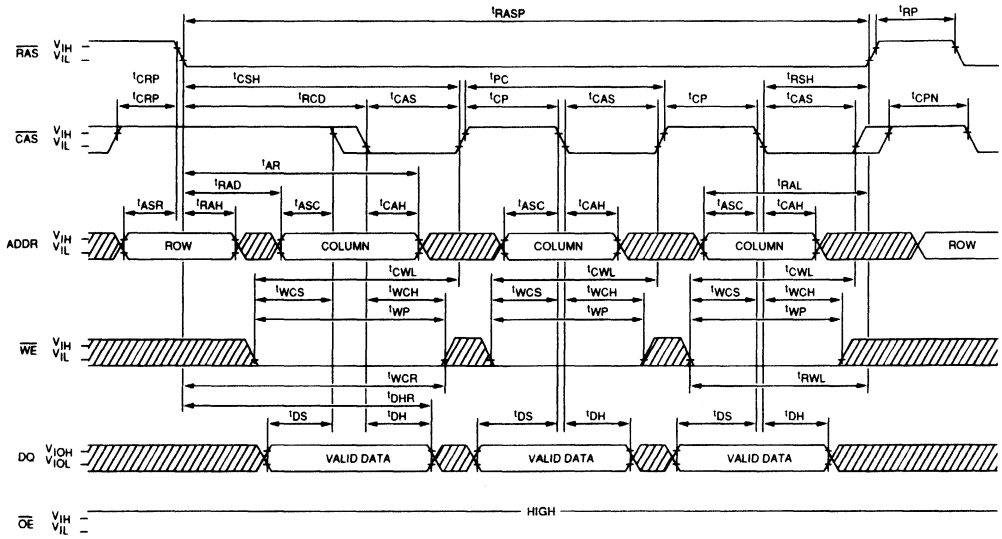
PAGE-MODE READ CYCLE



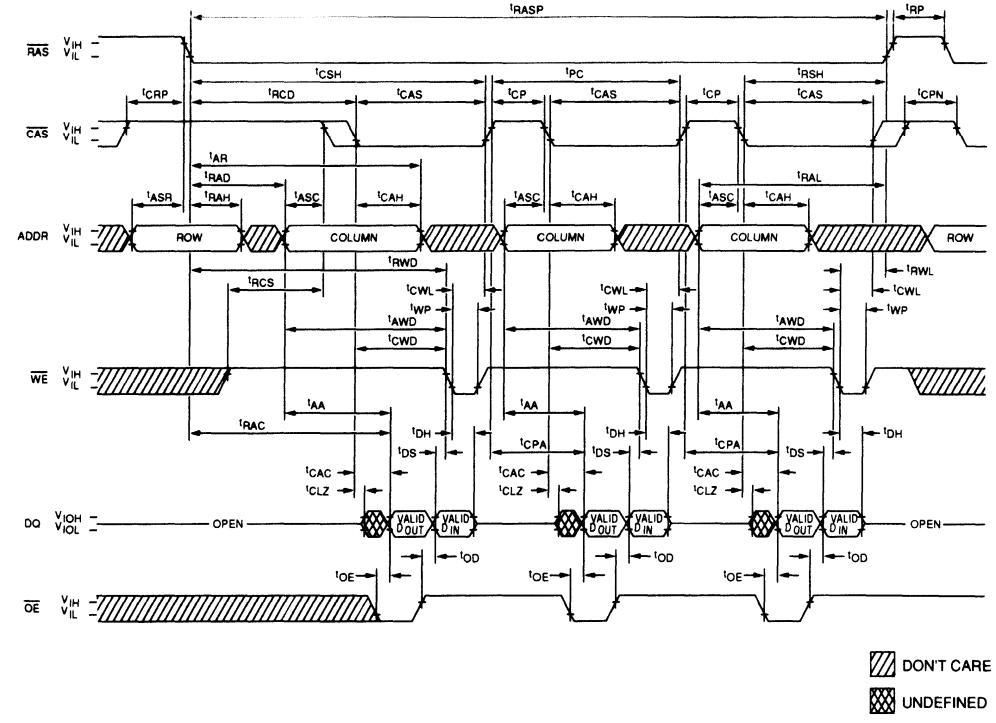
DON'T CARE

UNDEFINED

PAGE-MODE EARLY-WRITE CYCLE

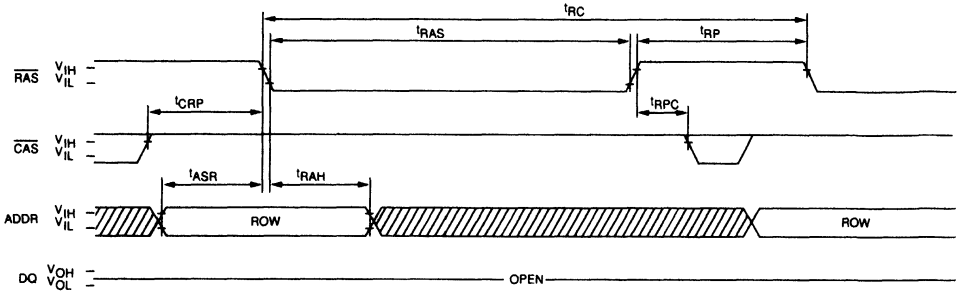


PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



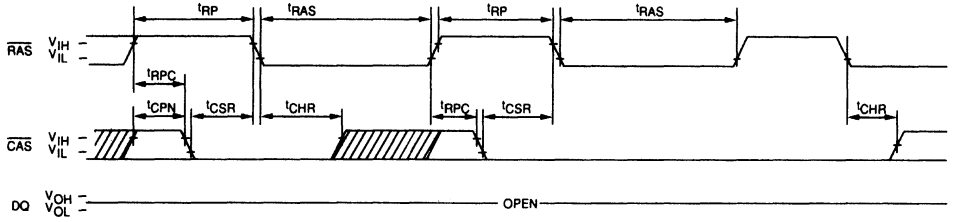
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; $\overline{WE}$ = DON'T CARE.)



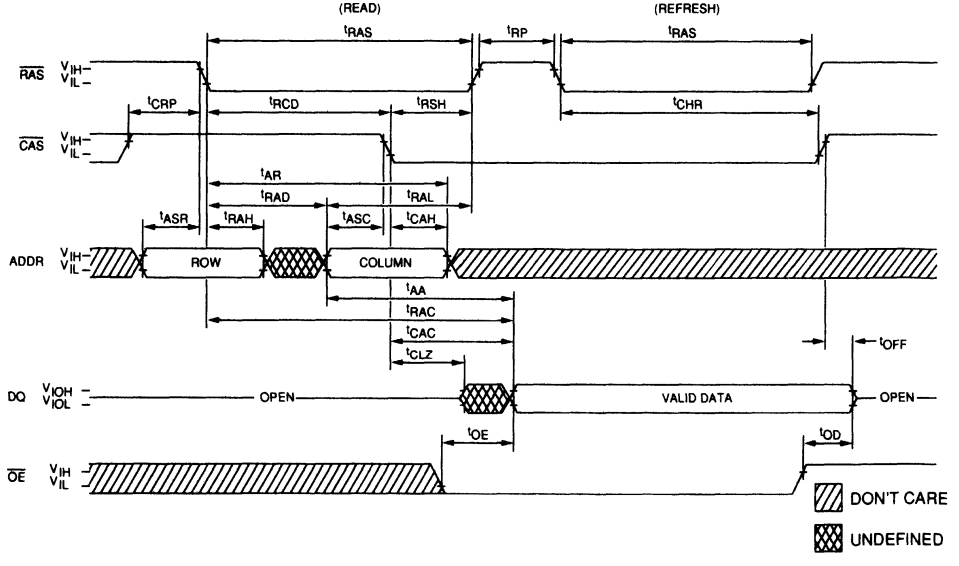
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH, $\overline{OE}$=LOW)[24]



DRAM MODULE

256K x 8 DRAM

FEATURES

- Industry standard pin-out in a 30-pin single-in-line memory module
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 120mW standby; 1200mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

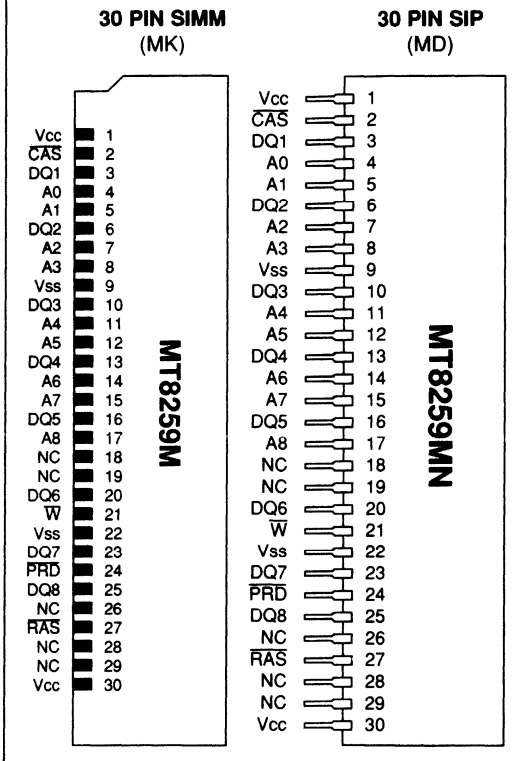
- Timing

80ns access	- 8
100ns access	-10
120ns access	-12
150ns access	-15

- Packages:

Leadless 30-pin SIMM	M
Leaded 30-pin SIP	MN

PIN ASSIGNMENT (Top View)

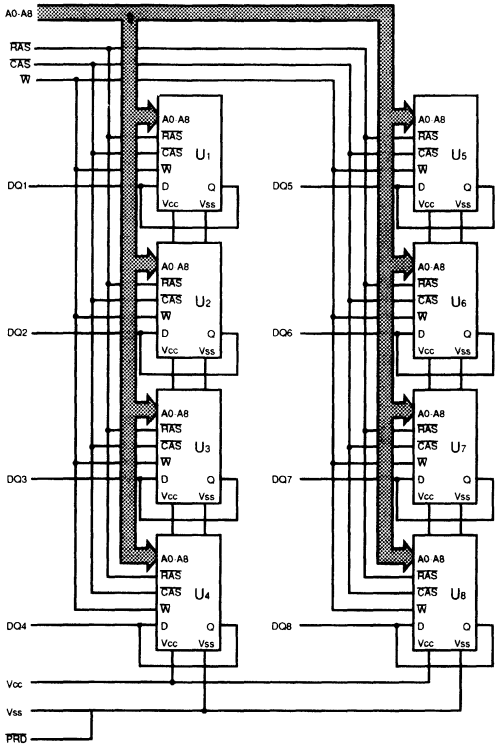


GENERAL DESCRIPTION

The MT8259 is a randomly accessed solid-state memory containing 262,144 words organized in a x8 configuration. The 18 address bits are entered 9 bits at a time using $\overline{RAS}$ to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. If the $\overline{WE}$ pin goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open until the next $\overline{CAS}$ cycle.

By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined page boundary. Returning $\overline{RAS}$ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



U1 - U8 = MT1259EJ

TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 8 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts	I_I	-80	80	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-80	80	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	40	40	40	40	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	520	440	440	360	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	520	440	440	360	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	440	320	320	280	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	520	440	440	360	mA	2,19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		40	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		64	pF	18
Input/Output Capacitance: DQ	C_{IO}		12	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

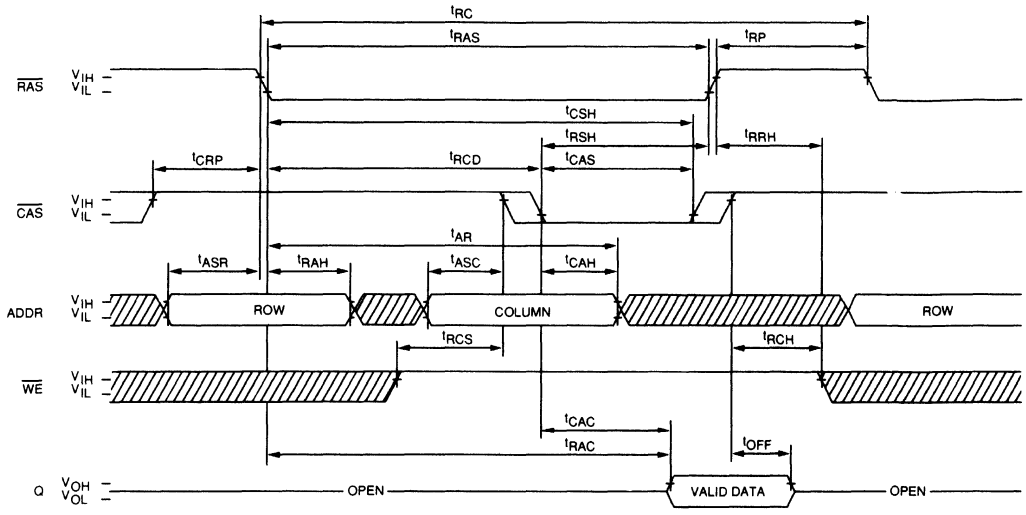
(Notes: 3, 4, 5, 10, 11, 17, 18) ($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	180		220		255		295		ns	
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	30		40		50		60		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	70		90		110		135		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	21
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	20
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$) refresh	^tCSR	10		15		20		20		ns	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		0		ns	20

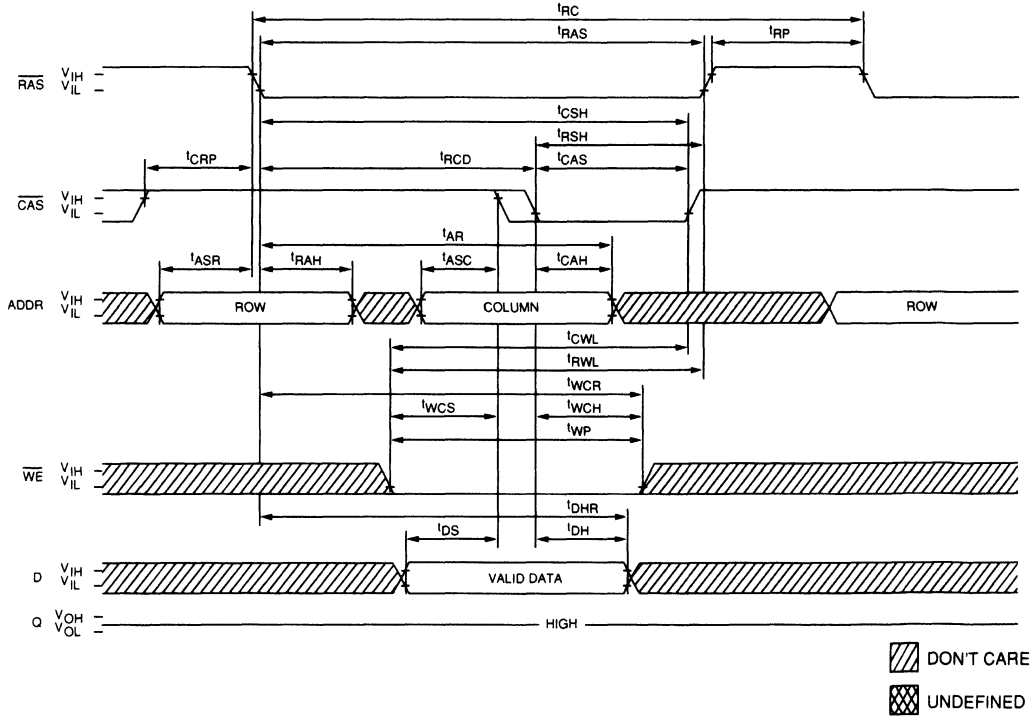
NOTES

1. All voltages referenced to Vss.
2. ICC is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq ^tRCD$ (max).
10. If $\overline{CAS}$ = VIH, data output is high impedance.
11. If $\overline{CAS}$ = VIL, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \geq ^tCWD$ (min) and $^tRWD \geq ^tRWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to VIH) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and VCC = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. On-chip refresh and address counters are enabled.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

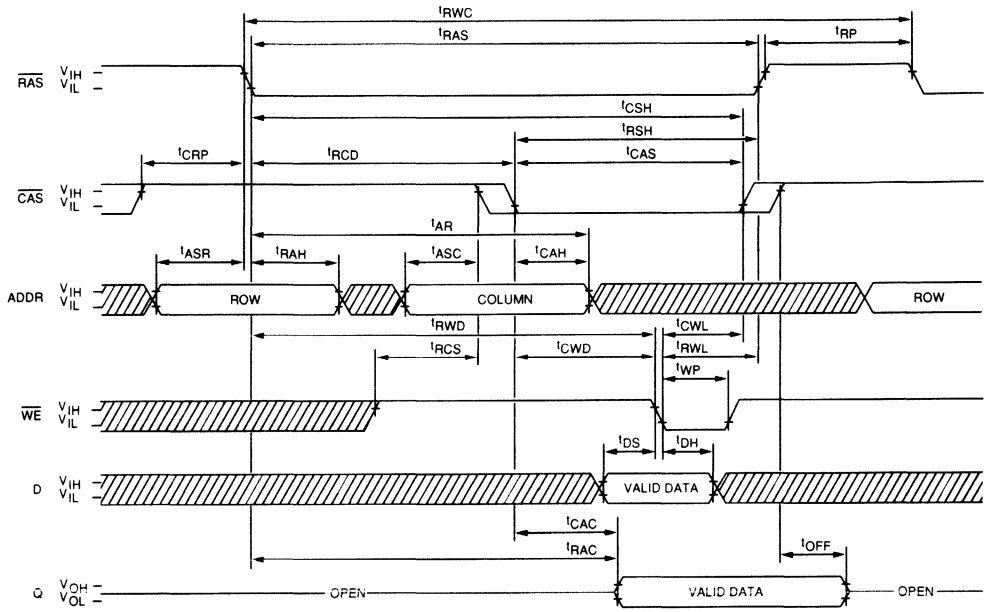
READ CYCLE



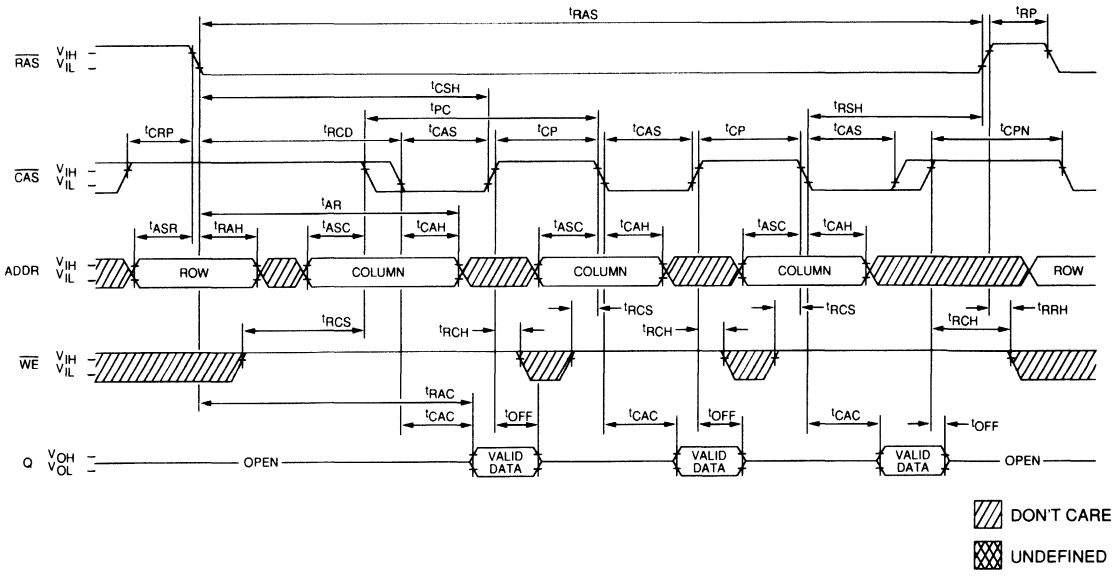
EARLY-WRITE CYCLE



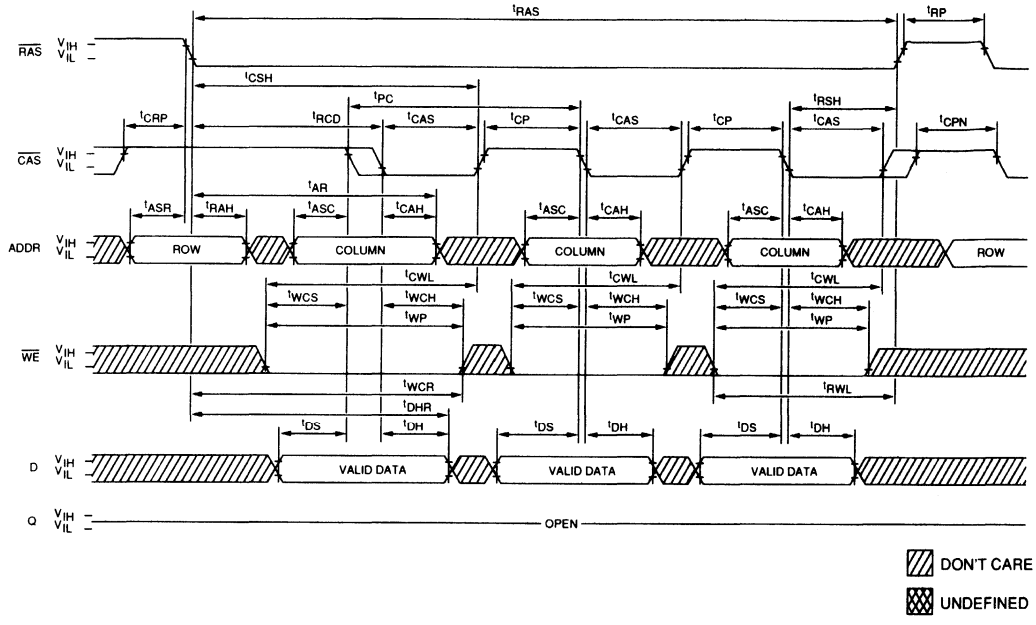
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE

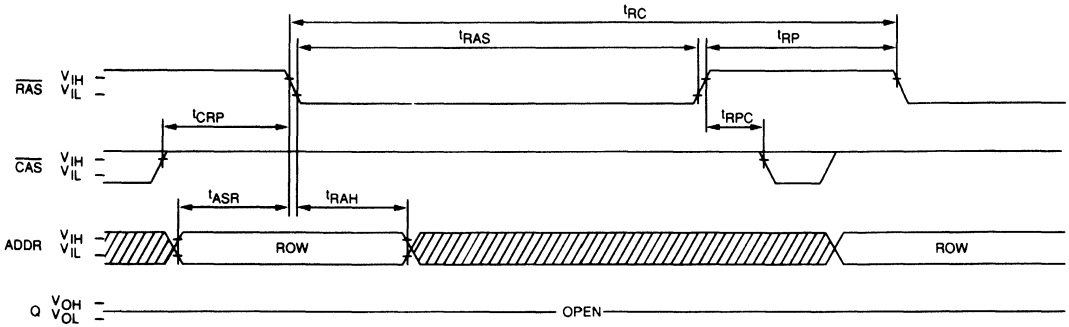


PAGE-MODE EARLY-WRITE CYCLE



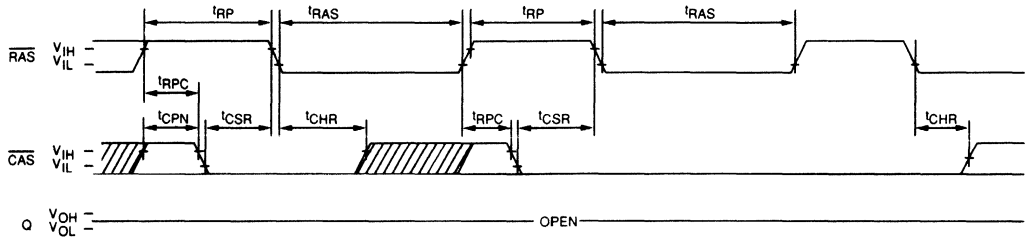
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



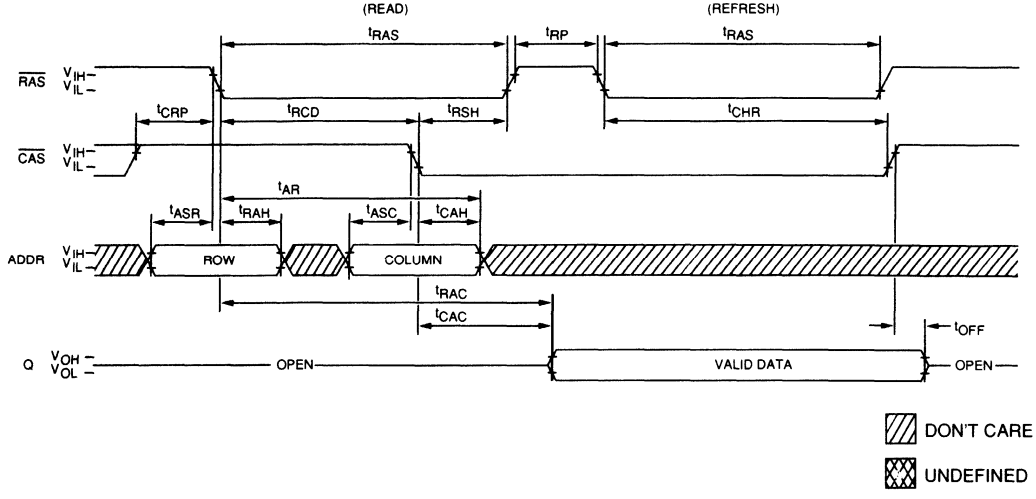
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8, $\overline{WE}$ = DON'T CARE.)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[21]



DRAM MODULE

256K x 9 DRAM

LOW PROFILE

FEATURES

- Industry standard pin-out in a 30-pin single-in-line package (SIP)
- Low profile, double-side mount (0.45 in)
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible.
- Low power, 135mW standby; 1350mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

- Timing

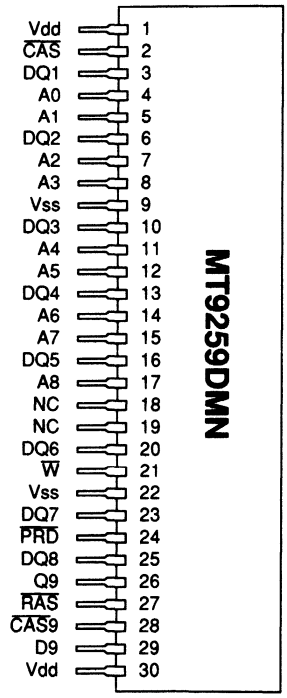
80ns access	- 8
100ns access	-10
120ns access	-12
150ns access	-15

- Packages:

(low profile) Leaded 30-pin SIP	DMN

PIN ASSIGNMENT (Top View)

30 PIN SIP
(ME)

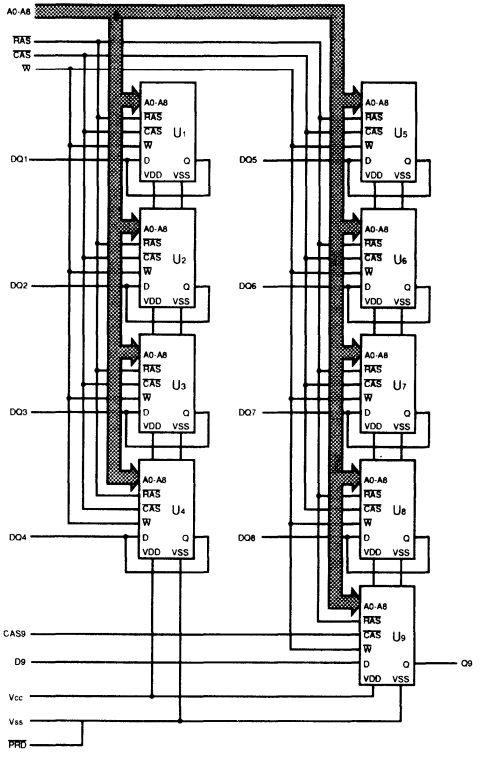


GENERAL DESCRIPTION

The MT9259 is a randomly accessed solid-state memory containing 262,144 words organized in a x9 configuration. The 18 address bits are entered 9 bits at a time using $\overline{RAS}$ to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. If the $\overline{WE}$ pin goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open until the next $\overline{CAS}$ cycle.

By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined page boundary. Returning $\overline{RAS}$ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



U1 - U9 = MT1259EJ

TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 9 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts	I_I	-90	90	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-90	90	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	45	45	45	45	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	585	495	495	405	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	585	495	495	405	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	495	360	360	315	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	585	495	495	405	mA	2,19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		45	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		72	pF	18
Input/Output Capacitance: DQ	C_{IO}		12	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

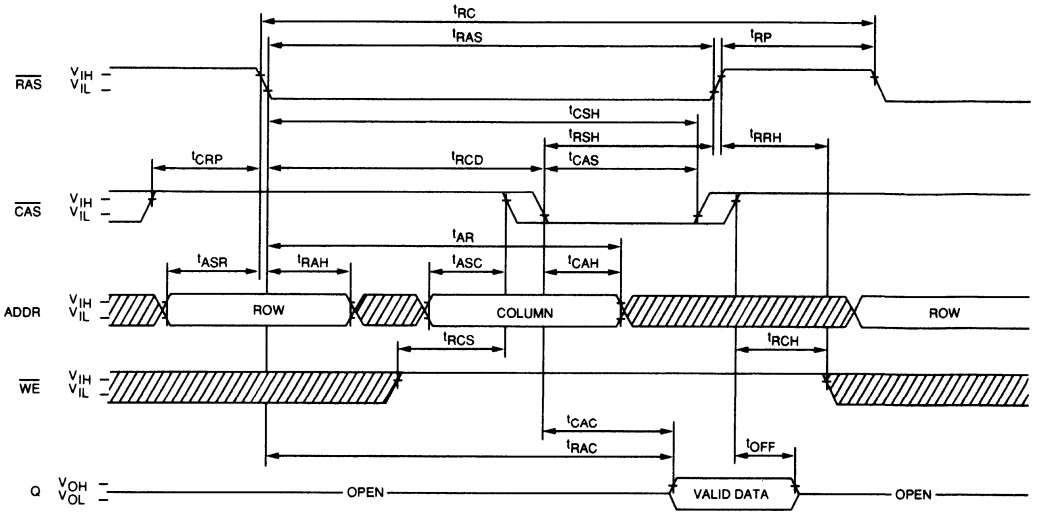
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	180		220		255		295		ns	
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	30		40		50		60		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	70		90		110		135		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	21
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	20
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$) refresh	^tCSR	10		15		20		20		ns	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		0		ns	20

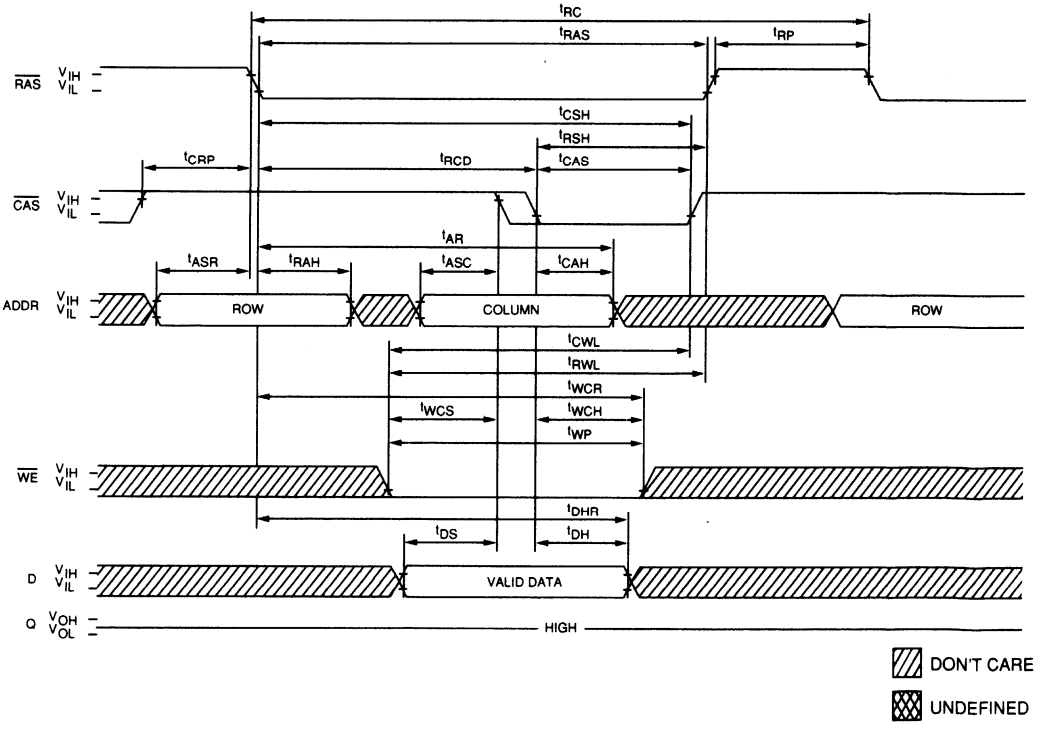
NOTES

1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq ^tRCD$ (max).
10. If $\overline{CAS}$ = VIH, data output is high impedance.
11. If $\overline{CAS}$ = VIL, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \geq ^tCWD$ (min) and $^tRWD \geq ^tRWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to VIH) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and Vcc = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. On-chip refresh and address counters are enabled.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

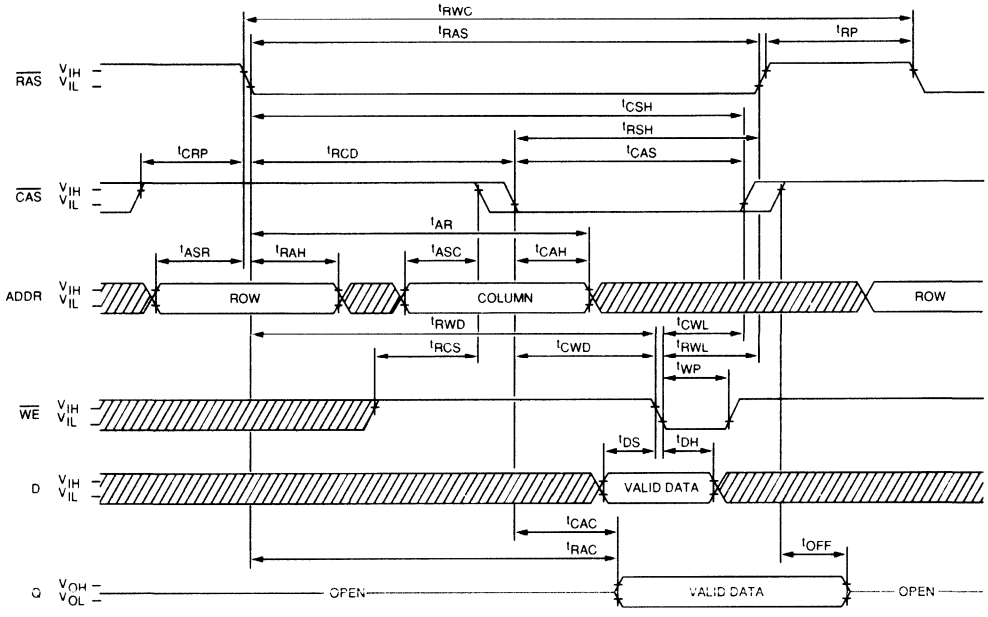
READ CYCLE



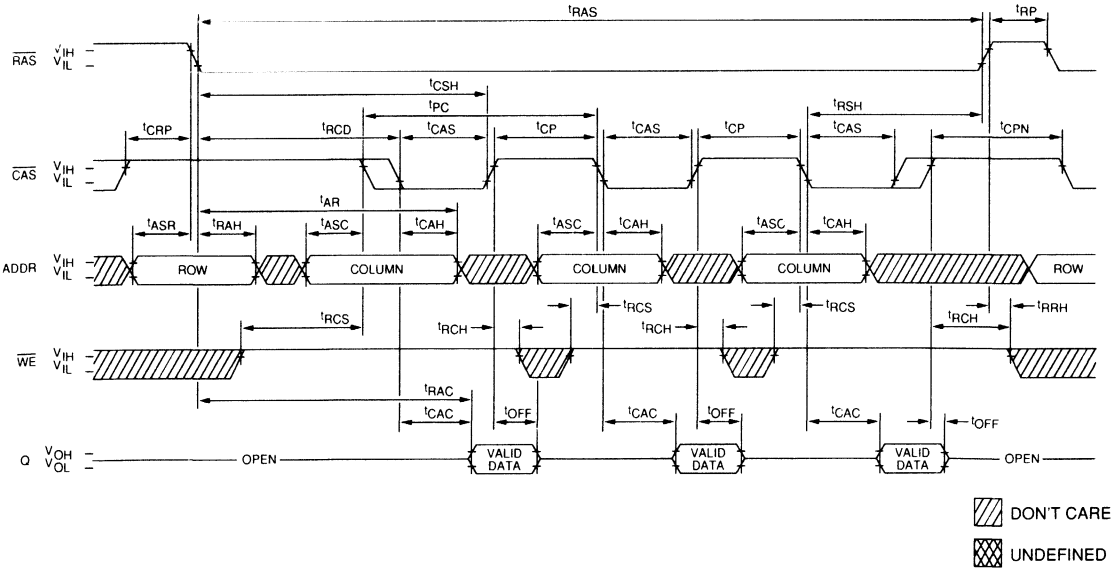
EARLY-WRITE CYCLE



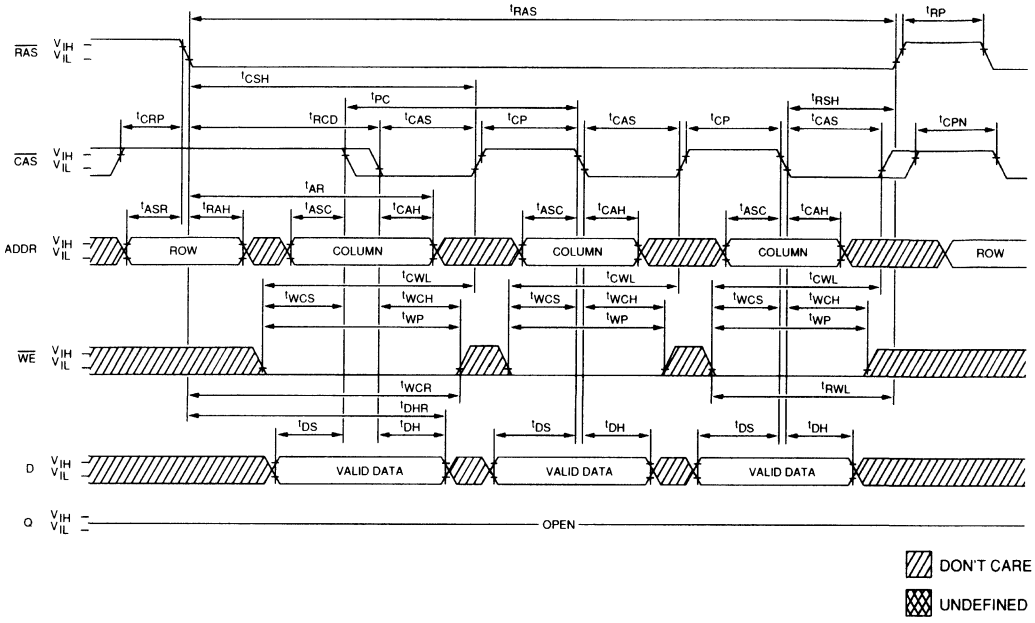
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE

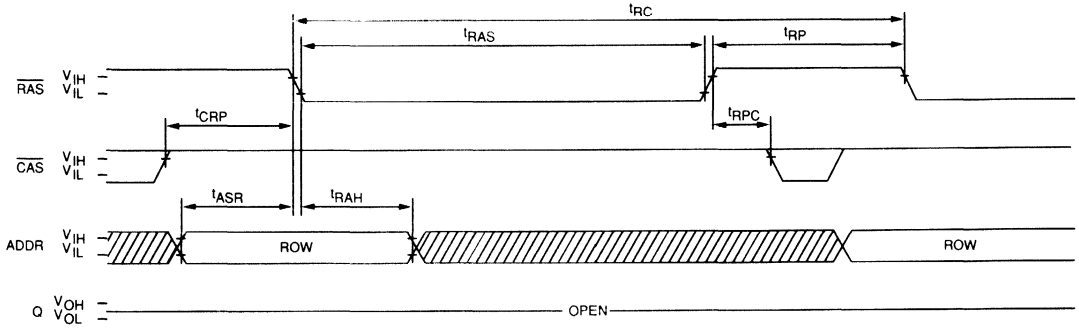


PAGE-MODE EARLY-WRITE CYCLE



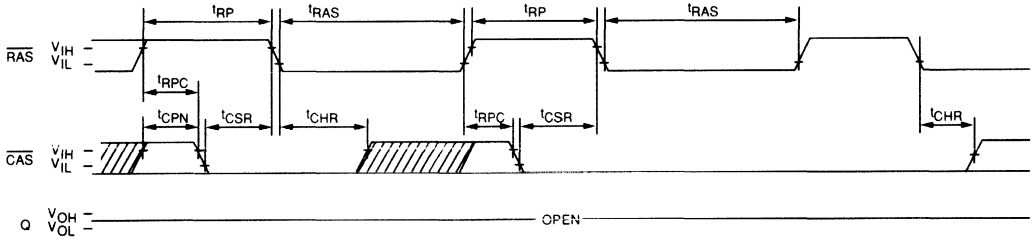
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



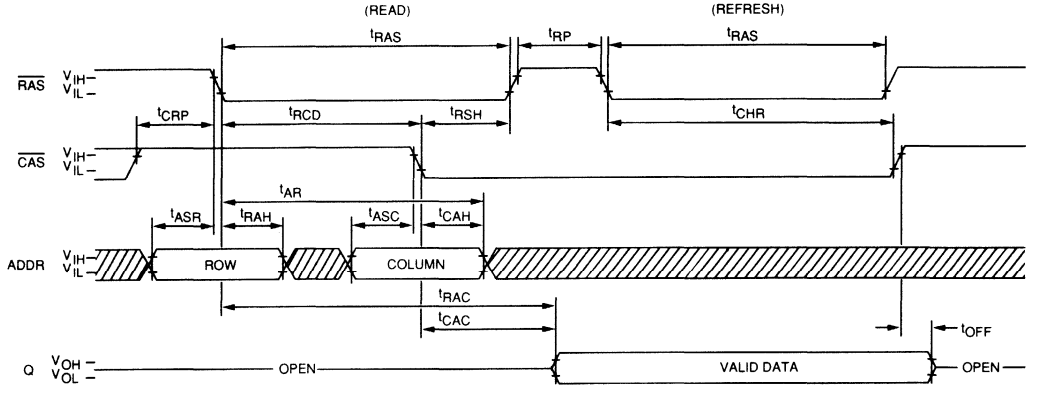
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8, $\overline{WE}$ = DON'T CARE.)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[21]



DON'T CARE

UNDEFINED

DRAM MODULE

256K x 9 DRAM

REFRESH: 512 CYCLE/8MS

FEATURES

- Industry standard pin-out in a 30-pin single-in-line memory module
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 135mW standby; 1350mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- Optional Page Mode access cycle
- 512 cycle refresh distributed across 8ms

OPTIONS MARKING

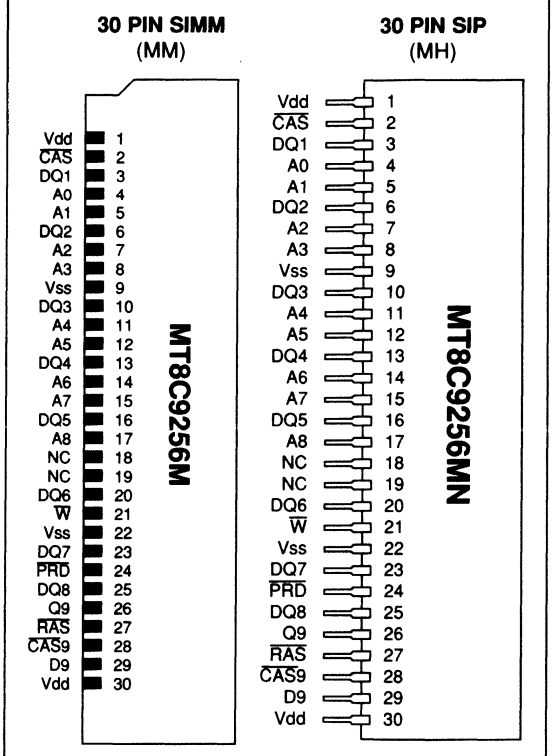
- Timing

80ns access	- 8
100ns access	-10
120ns access	-12

- Packages:

Leadless 30-pin SIMM	M
Leaded 30-pin SIP	MN

PIN ASSIGNMENT (Top View)



GENERAL DESCRIPTION

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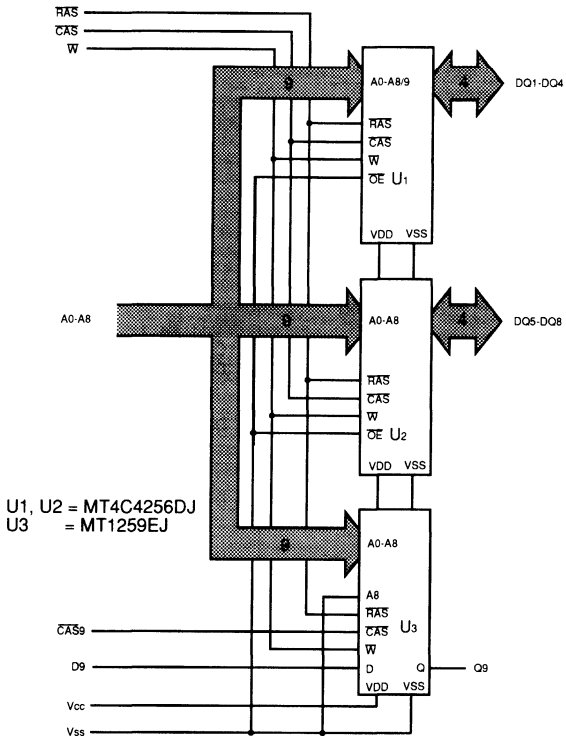
By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined page boundary. Returning $\overline{RAS}$ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (refresh) cycle so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



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				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 9 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts	I_I	-30	30	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-30	30	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	11	9	9	9	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	205	175	155	125	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	165	135	115	85	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	195	160	140	115	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	205	175	155	125	mA	2,19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		15	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		27	pF	18
Input Capacitance: D	C_{I3}		7	pF	18
Input/Output Capacitance: DQ	C_{IO}		12	pF	18
Output Capacitance: DQ	C_O		7	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

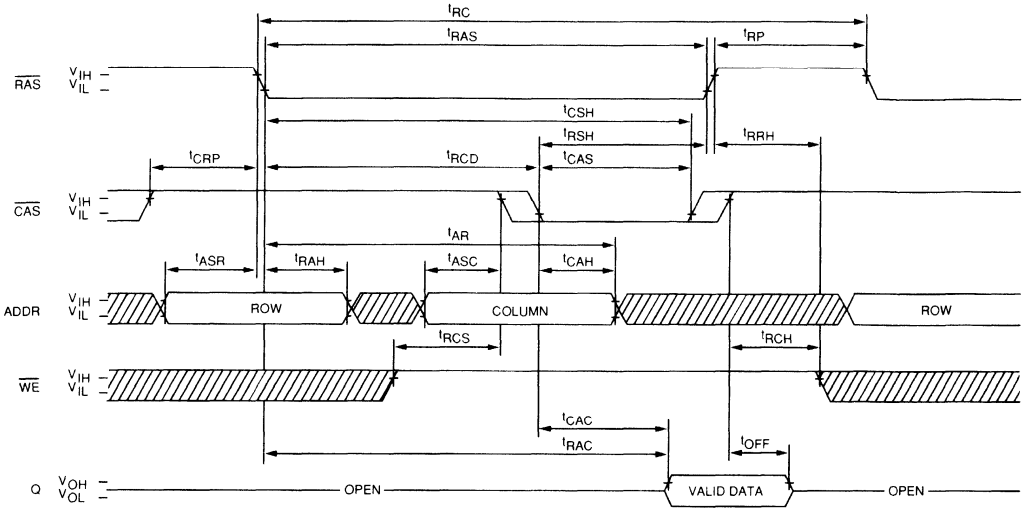
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	180		220		255		295		ns	
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	30		40		50		60		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	70		90		110		135		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	21
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	20
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$) refresh	^tCSR	10		15		20		20		ns	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		0		ns	20

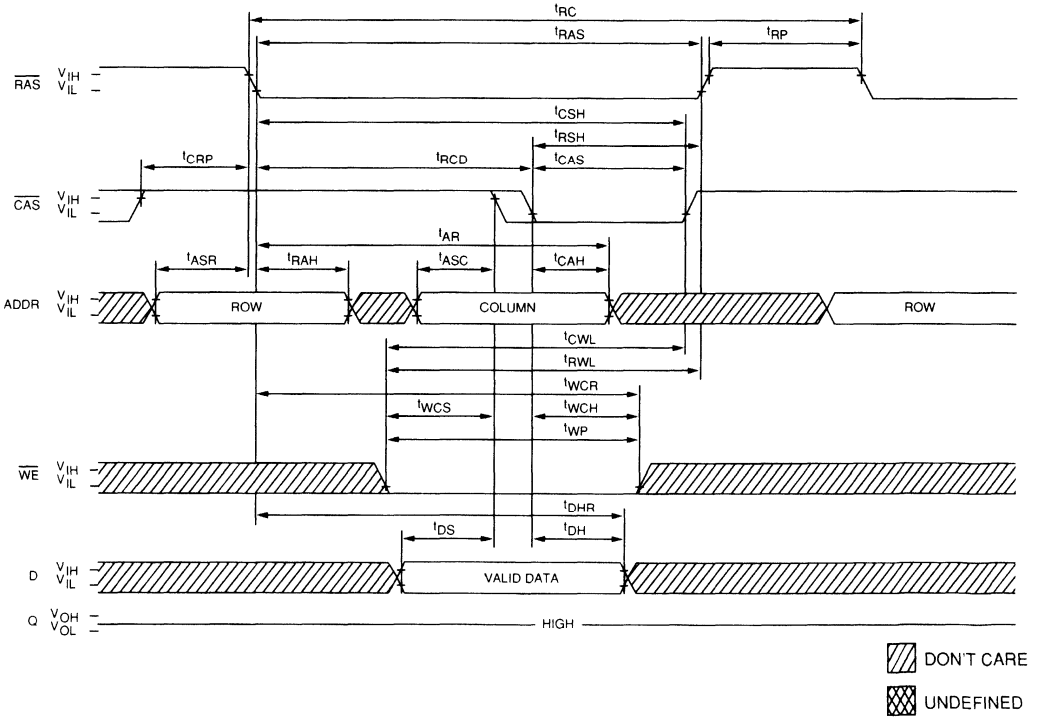
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge {}^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \ge {}^tCWD$ (min) and $^tRWD \ge {}^tRWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. On-chip refresh and address counters are enabled.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

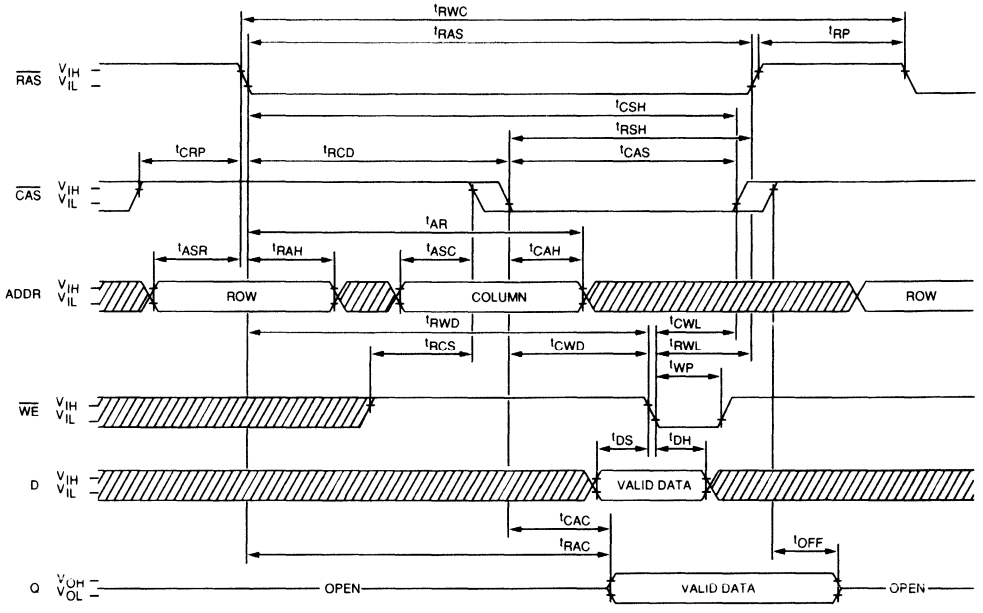
READ CYCLE



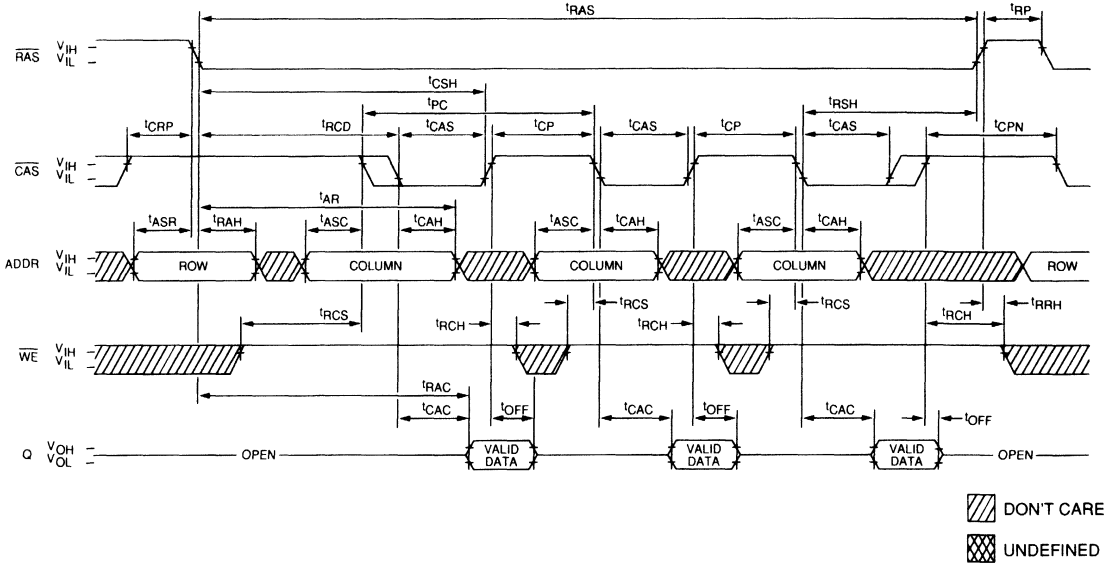
EARLY-WRITE CYCLE



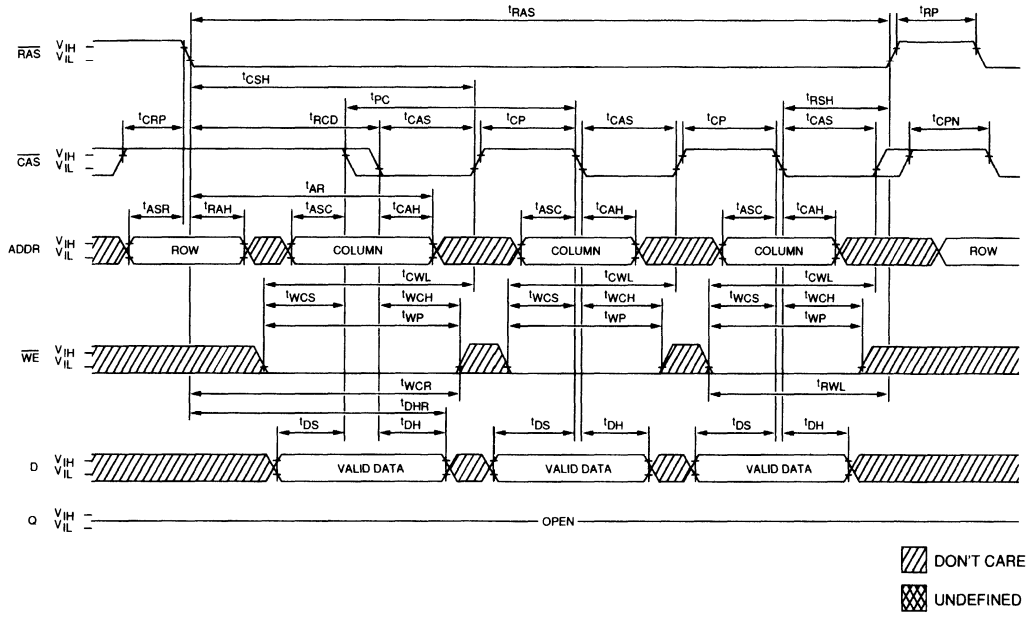
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE

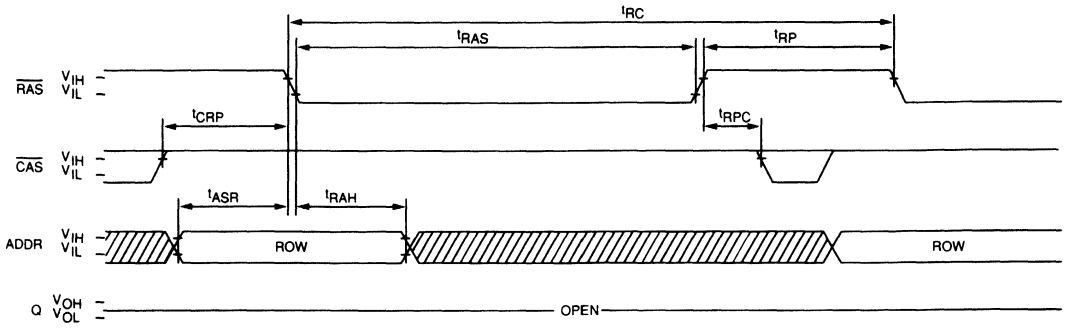


PAGE-MODE EARLY-WRITE CYCLE



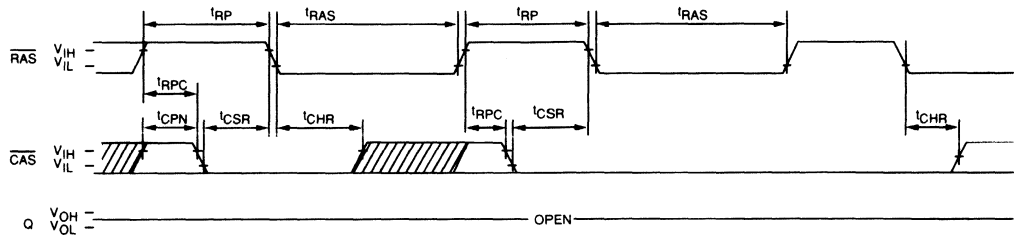
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



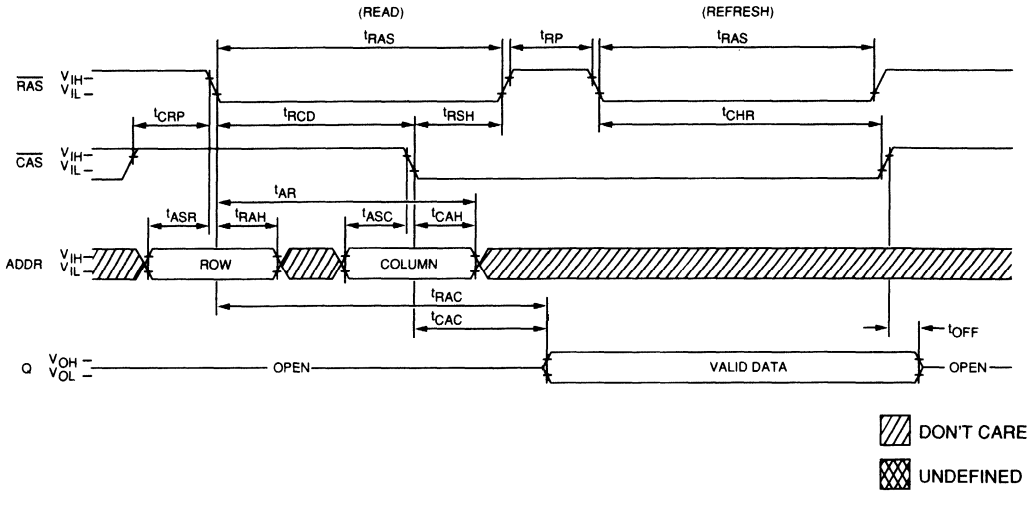
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8, $\overline{WE}$ = DON'T CARE.)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[21]



DRAM MODULE

256K x 9 DRAM

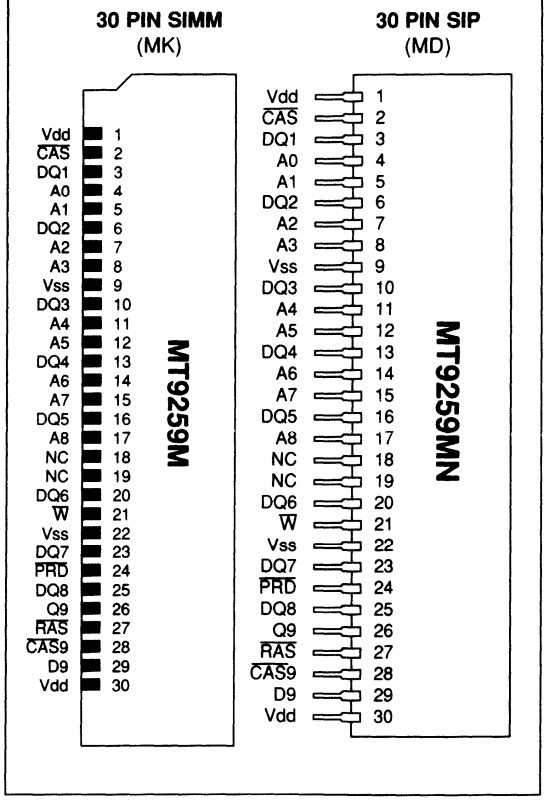
FEATURES

- Industry standard pin-out in a 30-pin single-in-line memory module
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Low power, 135mW standby; 1350mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256 cycle refresh distributed across 4ms
- Optional Page Mode access cycle

OPTIONS MARKING

• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
150ns access	-15
• Packages:	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	MN

PIN ASSIGNMENT (Top View)

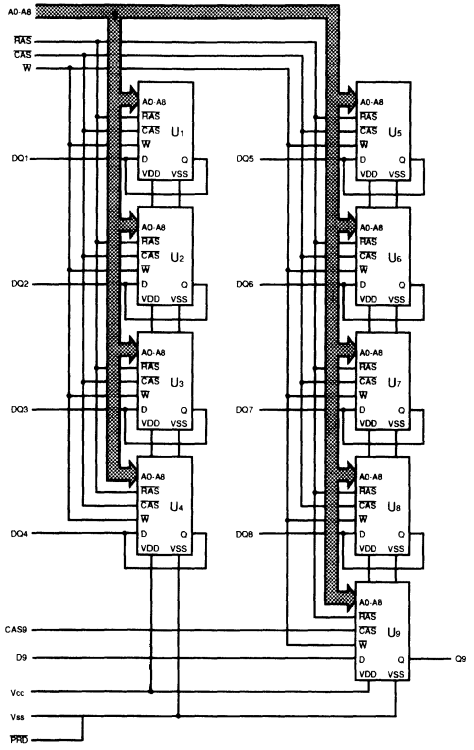


GENERAL DESCRIPTION

The MT9259 is a randomly accessed solid-state memory containing 262,144 words organized in a x9 configuration. The 18 address bits are entered 9 bits at a time using $\overline{RAS}$ to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. If the $\overline{WE}$ pin goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open until the next $\overline{CAS}$ cycle.

By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled to execute several faster READ or WRITE cycles within the $\overline{RAS}$ address defined page boundary. Returning $\overline{RAS}$ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM



U1 - U9 = MT1259EJ

TRUTH TABLE

Function	RAS	CAS	WE	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 9 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts	I_I	-90	90	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OZ}	-90	90	µA	
OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-8	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	45	45	45	45	mA	
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC2}	585	495	495	405	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC3}	585	495	495	405	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = $t_{RC(MIN)}$)	I_{CC4}	495	360	360	315	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = cycling, t_{RC} = $t_{RC(MIN)}$)	I_{CC5}	585	495	495	405	mA	2,19

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		45	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		72	pF	18
Input Capacitance: D	C_{I3}		7	pF	18
Input/Output Capacitance: DQ	C_{IO}		12	pF	18
Output Capacitance: DQ	C_O		7	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

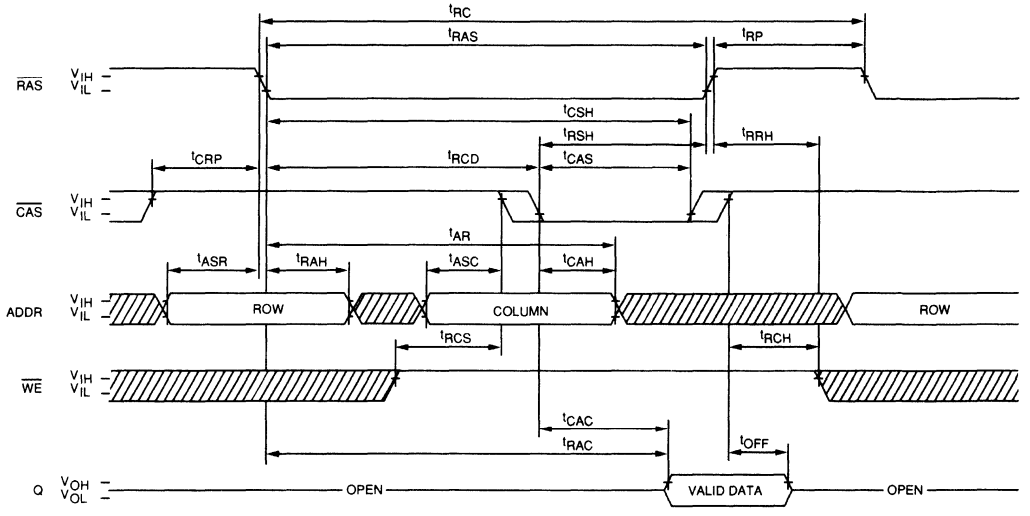
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	180		220		255		295		ns	
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	30		40		50		60		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	70		90		110		135		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	21
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	20
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$) refresh	^tCSR	10		15		20		20		ns	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		0		ns	20

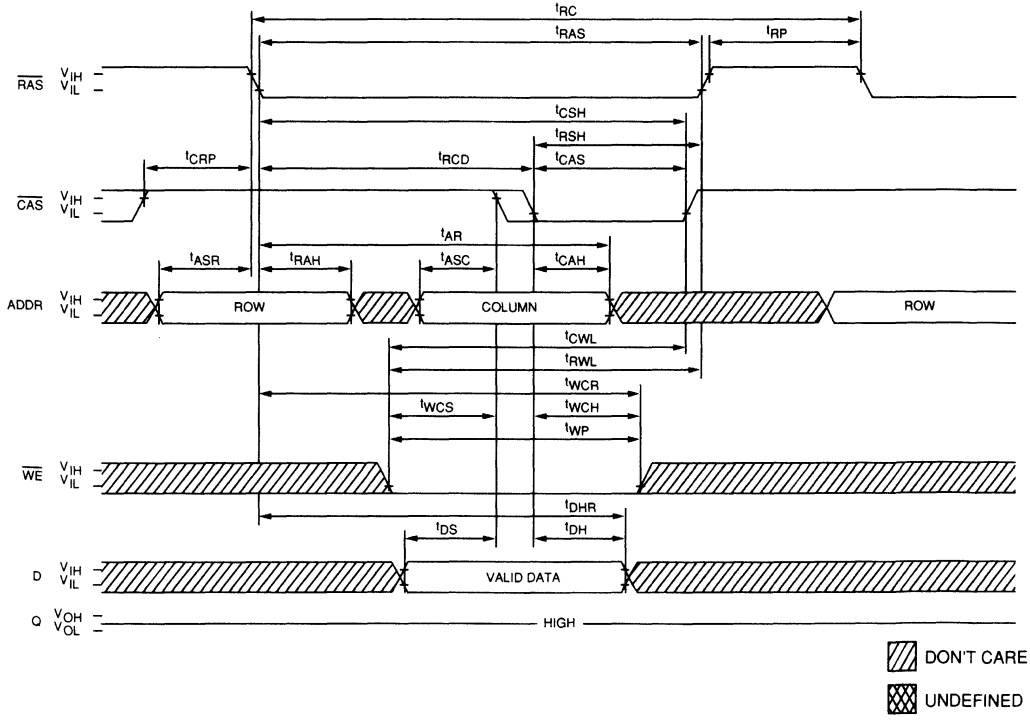
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \ge ^tCWD$ (min) and $^tRWD \ge ^tRWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. On-chip refresh and address counters are enabled.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

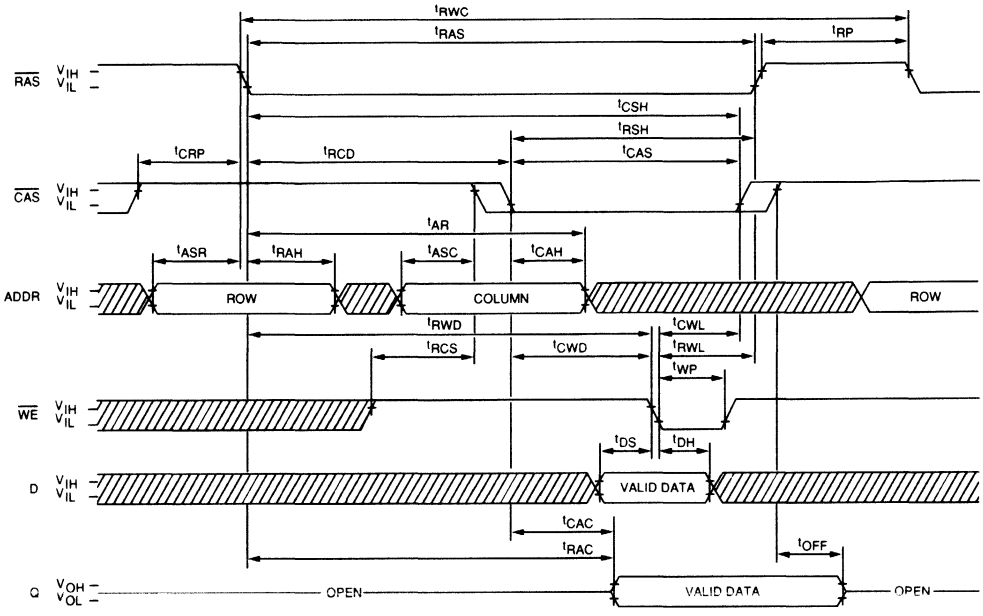
READ CYCLE



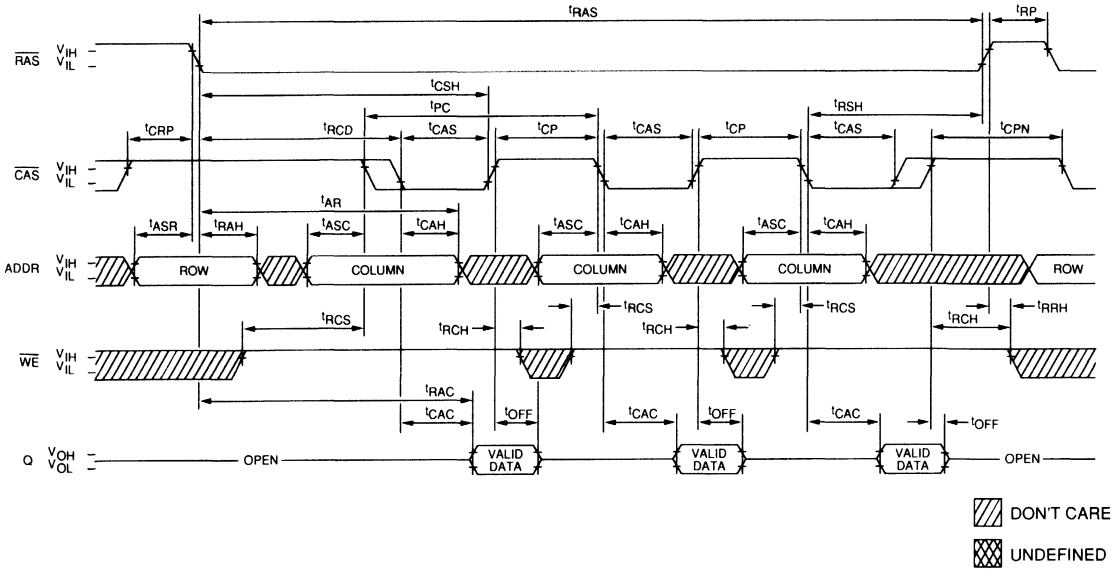
EARLY-WRITE CYCLE



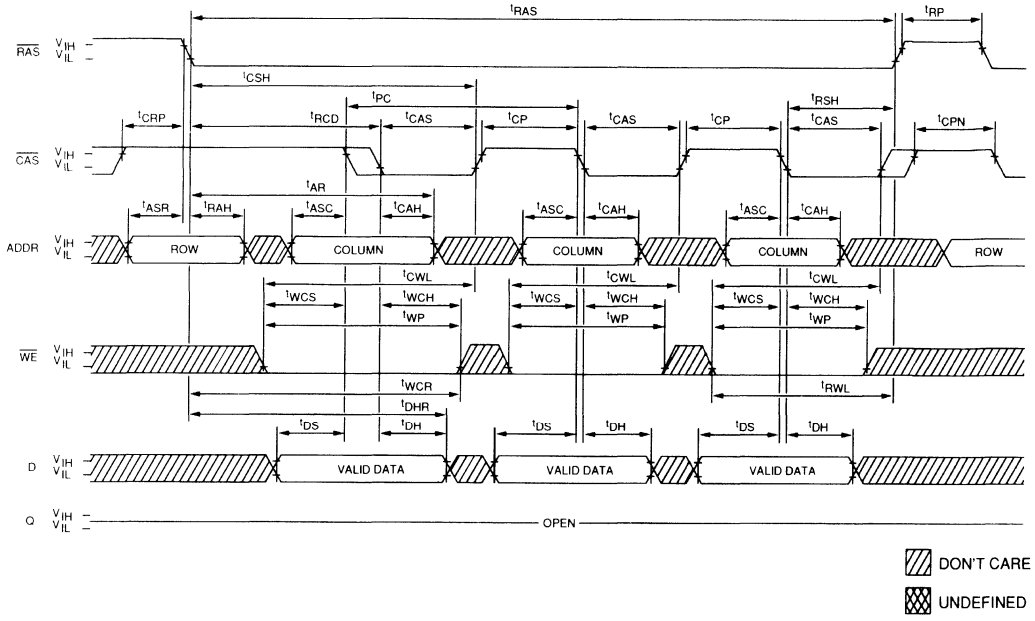
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE

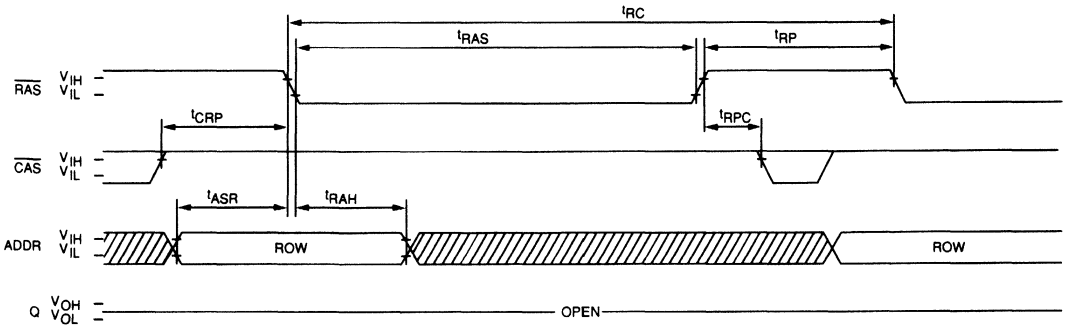


PAGE-MODE EARLY-WRITE CYCLE



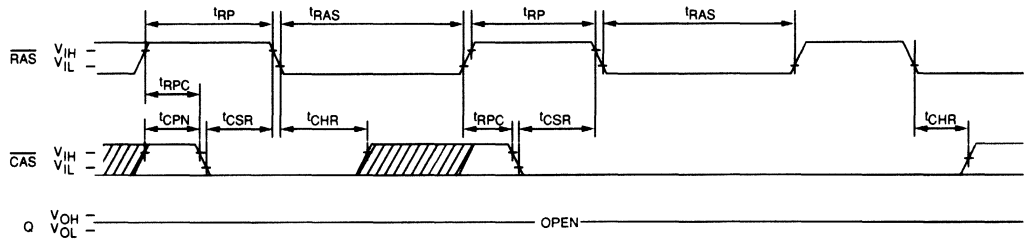
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



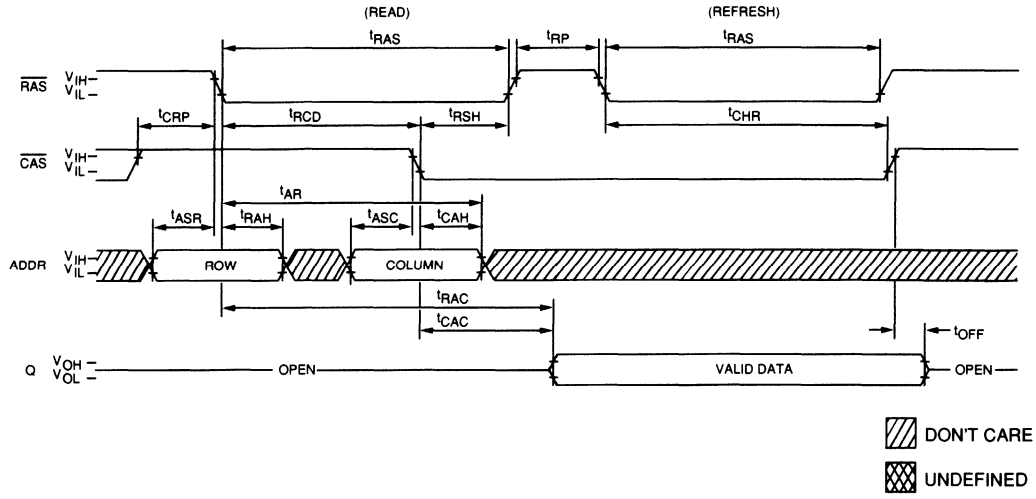
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8, $\overline{WE}$ = DON'T CARE.)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[21]



DRAM MODULE

256K x 36 DRAM

FEATURES

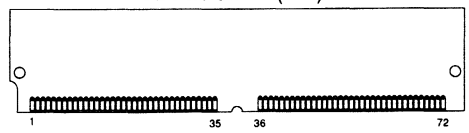
- Industry standard pin-out in a 72-pin single-in-line package
- High performance CMOS silicon gate process.
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 100mW standby; 2000mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512 cycle refresh distributed across 8ms
- Optional Page Mode

OPTIONS MARKING

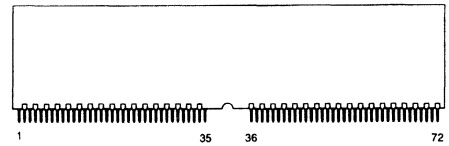
- Timing
  - 80ns access - 8
  - 100ns access -10
  - 120ns access -12
- Lead dress
  - Tin/Lead None
  - Gold (SIMM only) G
- Packages:
  - Leadless 72-pin SIMM M
  - Leaded 72-pin ZIP ZN

PIN ASSIGNMENT (Top View)

72 PIN SIMM (MN)



72 PIN ZIP (MP)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	Vss	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	Vcc
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	NC	50	DQ27	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	PRD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	Vss

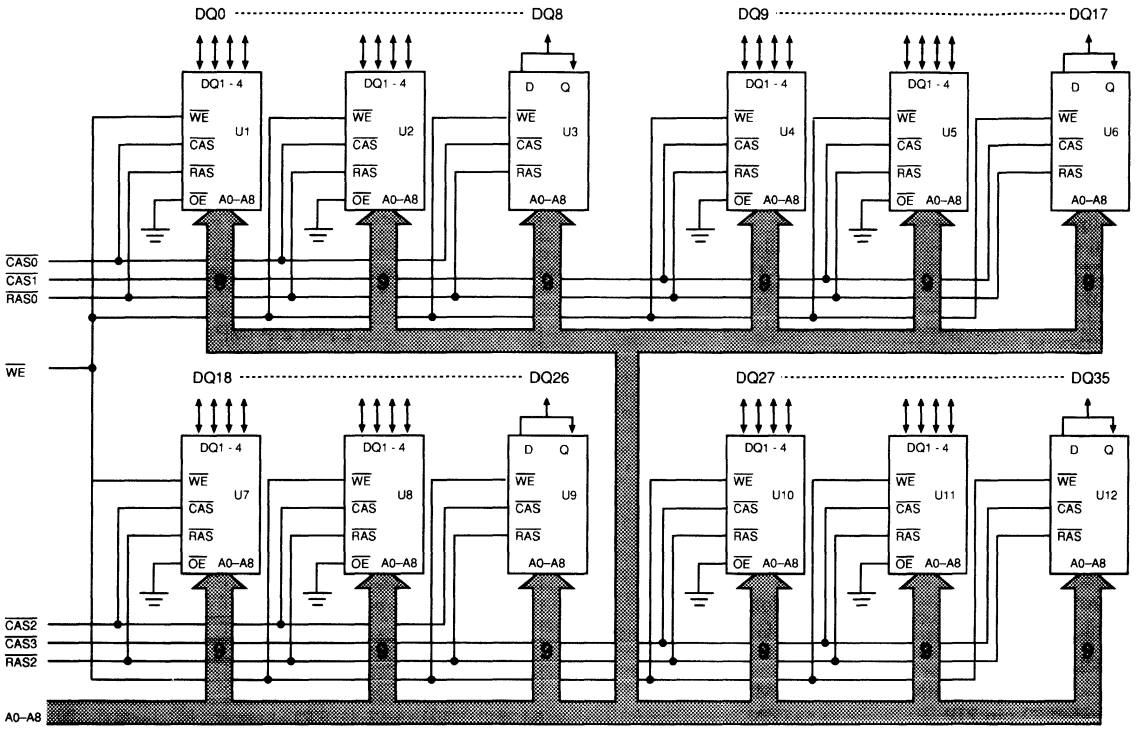
GENERAL DESCRIPTION

The MT8C36256 is a randomly accessed solid-state memory containing 262,144 words organized in a x36 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM



U1, U2, U4, U5, U7, U8, U10, U11 = MT4C4256DJ
U3, U6, U9, U12 = MT1259EJ

TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

PRESENCE DETECT

SYMBOL	-8	-10	-12
PRD1	GND	GND	GND
PRD2	NC	NC	NC
PRD3	GND	GND	NC
PRD4	NC	GND	NC

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 12 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts) (For each package input)	I_I	-120	120	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) (For each package input)	I_{OZ}	-120	120	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		720	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		720	mA	2
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		36	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		14	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		840	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		840	mA	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		60	pF	18
Input Capacitance: $\overline{WE}$	C_{I2}		84	pF	18
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		42	pF	18
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		21	pF	18
Input/Output Capacitance: DQ0 - DQ35	C_{IO}		17	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

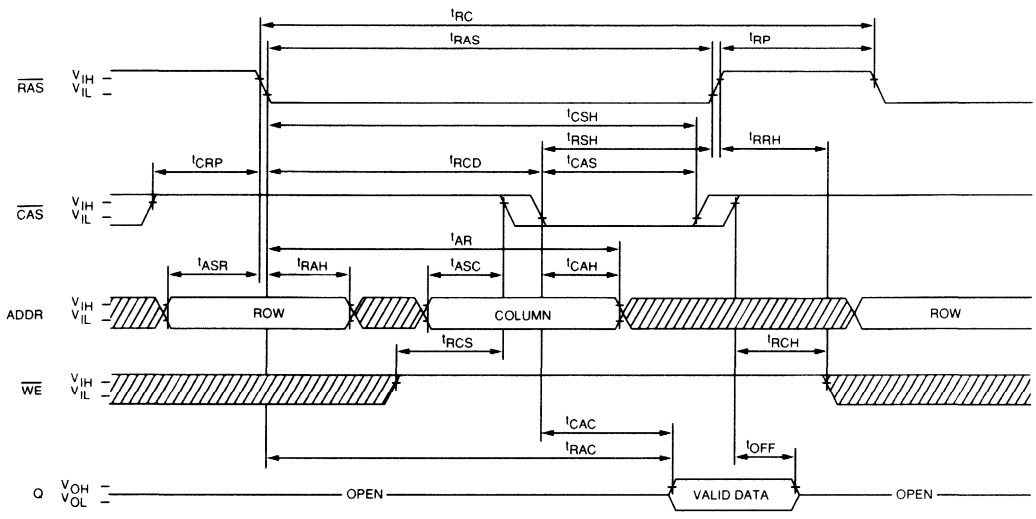
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	180		220		255		295		ns	
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	30		40		50		60		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	70		90		110		135		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	21
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	20
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$) refresh	^tCSR	10		15		20		20		ns	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		0		ns	20

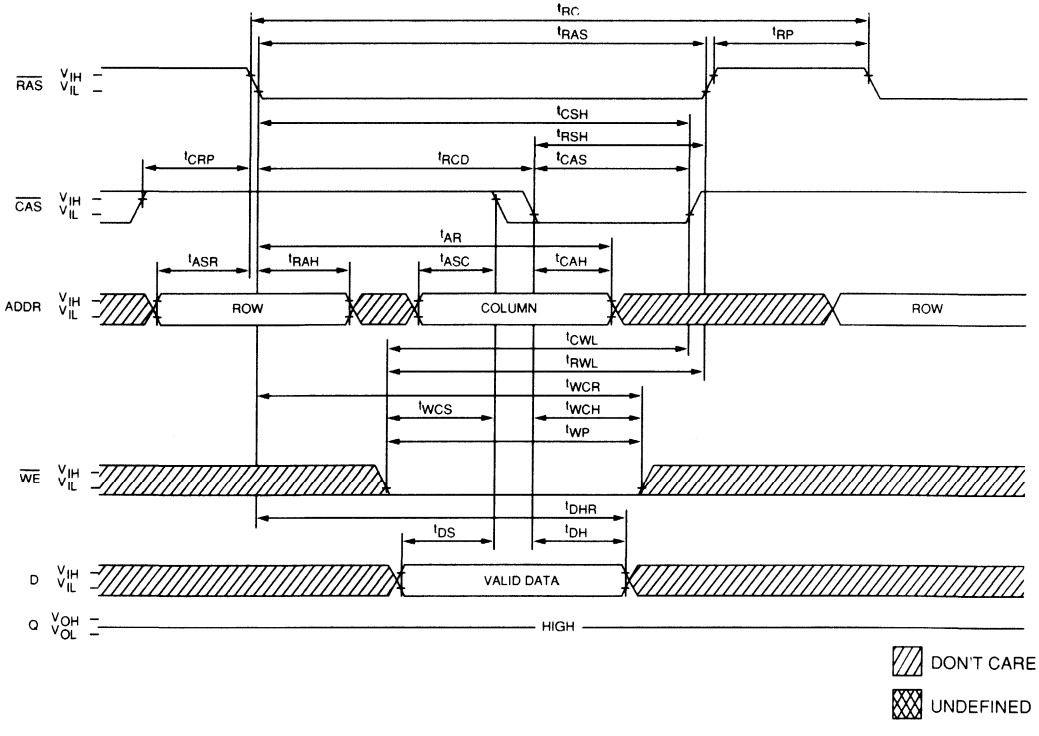
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq ^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \geq ^tCWD$ (min) and $^tRWD \geq ^tRWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. On-chip refresh and address counters are enabled.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

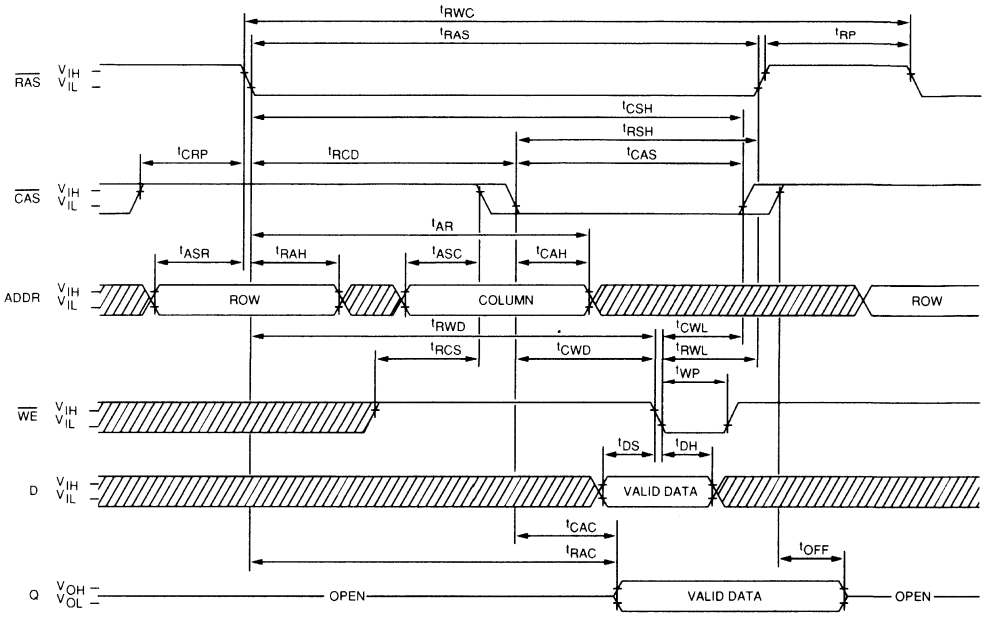
READ CYCLE



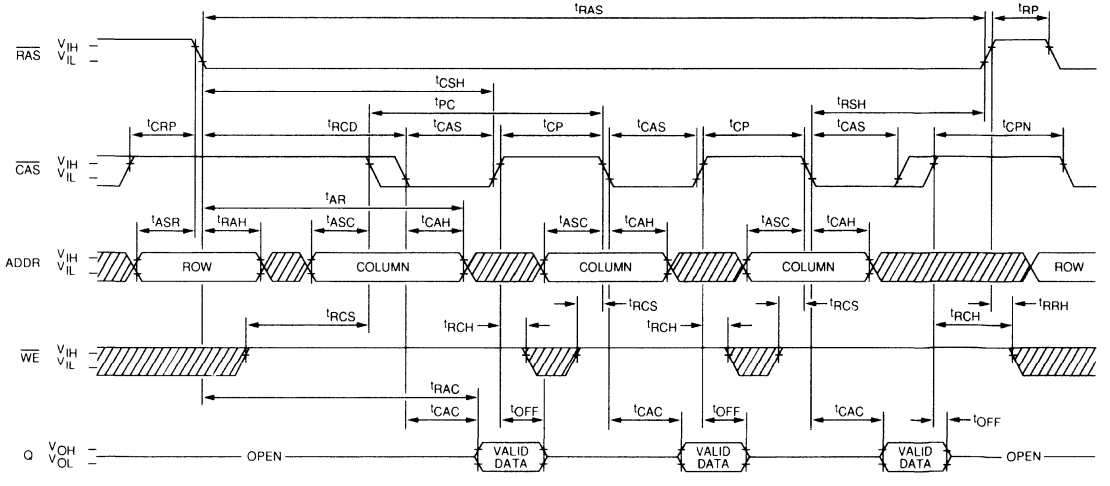
EARLY-WRITE CYCLE



READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



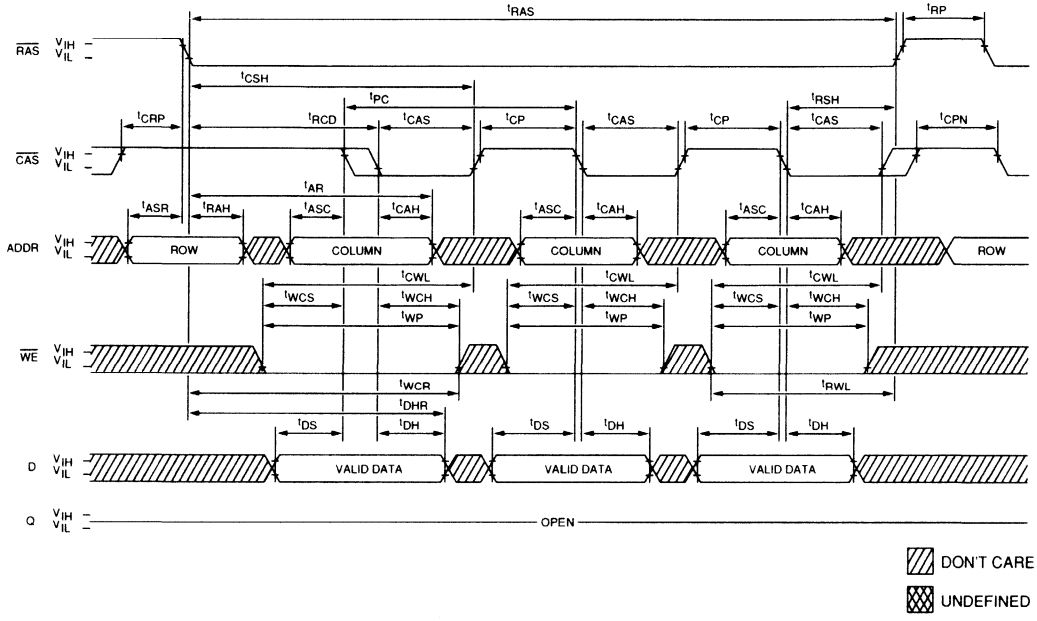
PAGE-MODE READ CYCLE



DON'T CARE

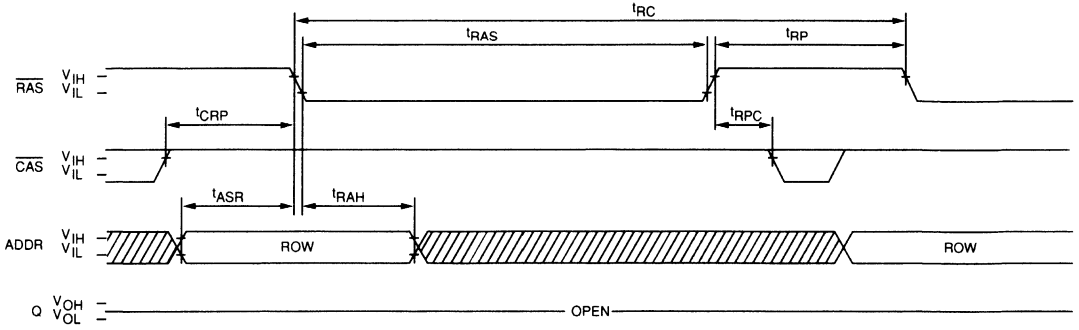
UNDEFINED

PAGE-MODE EARLY-WRITE CYCLE



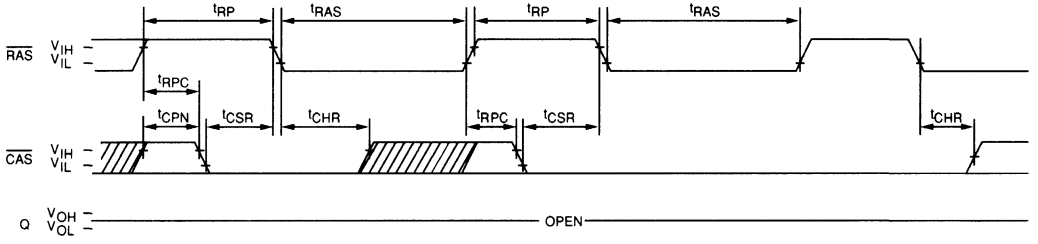
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



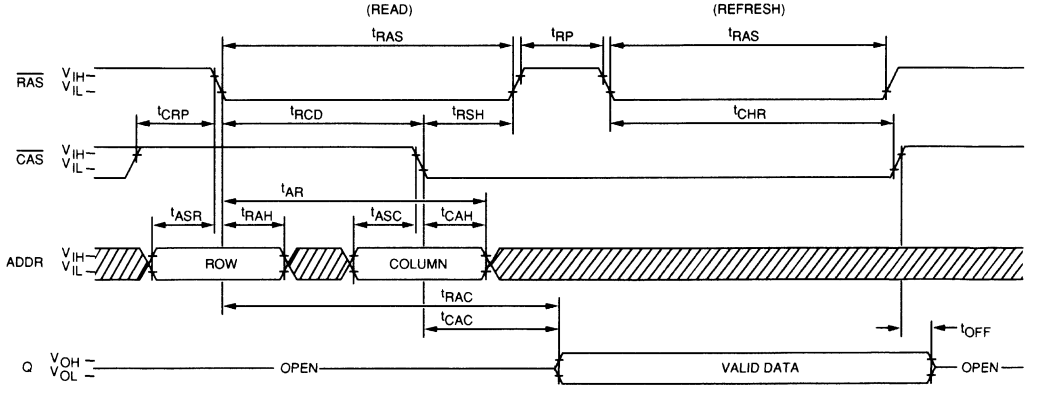
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8 and $\overline{WE}$ = DON'T CARE.)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[21]



DON'T CARE

UNDEFINED

DRAM MODULE

512K x 36 DRAM

FEATURES

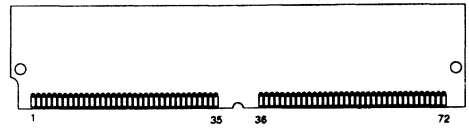
- Industry standard pin-out in a 72-pin single-in-line package
- High performance CMOS silicon gate process.
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 100mW standby; 2000mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512 cycle refresh distributed across 8ms
- Optional Page Mode

OPTIONS MARKING

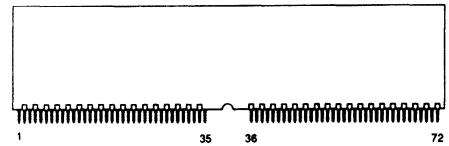
• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Lead dress	
Tin/Lead	None
Gold (SIMM only)	G
• Packages:	
Leadless 72-pin SIMM	DM
Leaded 72-pin ZIP	DZN

PIN ASSIGNMENT (Top View)

72 PIN SIMM (MO)



72 PIN ZIP (MQ)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	Vss	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	Vcc
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	$\overline{RAS1}$	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	NC	50	DQ27	68	PRD2
15	A3	33	$\overline{RAS3}$	51	DQ10	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	PRD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	Vss

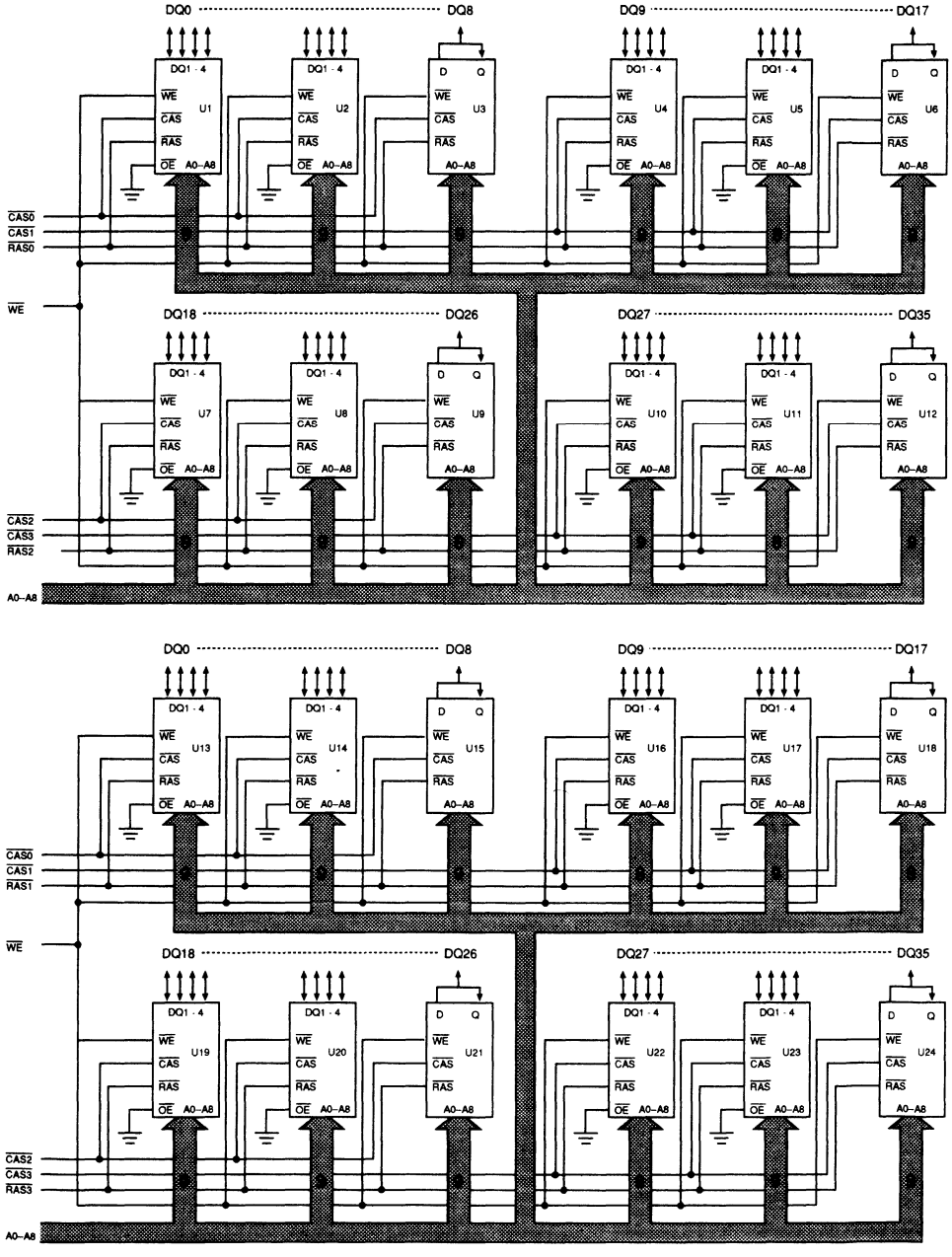
GENERAL DESCRIPTION

The MT8C36256 is a randomly accessed solid-state memory containing 524,288 words organized in a x36 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM



U1, U2, U4, U5, U7, U8, U10, U11, U13, U14, U16, U17, U19, U20, U22, U23 = MT4C4256DJ
U3, U6, U9, U12, U15, U18, U21, U24 = MT1259EJ

TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

PRESENCE DETECT

SYMBOL	-8	-10	-12
PRD1	NC	NC	NC
PRD2	GND	GND	GND
PRD3	GND	GND	NC
PRD4	NC	GND	NC

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 12 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	$V_{CC}+1$	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT (any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts) (For each package input)	I_I	-240	240	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, $0V \le V_{OUT} \le V_{CC}$) (For each package input)	I_{OZ}	-240	240	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: $t_{RC} = t_{RC(MIN)}$)	I_{CC1}		1.2	A	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ = Cycling: $t_{PC} = t_{PC(MIN)}$)	I_{CC2}		1.2	A	2
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		72	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{CC}$ -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		28	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS} = V_{IH}$)	I_{CC5}		1.6	A	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		1.6	A	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		60	pF	18
Input Capacitance: $\overline{WE}$	C_{I2}		84	pF	18
Input Capacitance: $\overline{RAS}0$, $\overline{RAS}2$	C_{I3}		42	pF	18
Input Capacitance: $\overline{CAS}0$, $\overline{CAS}1$, $\overline{CAS}2$, $\overline{CAS}3$	C_{I4}		21	pF	18
Input/Output Capacitance: DQ0 - DQ35	C_{IO}		17	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

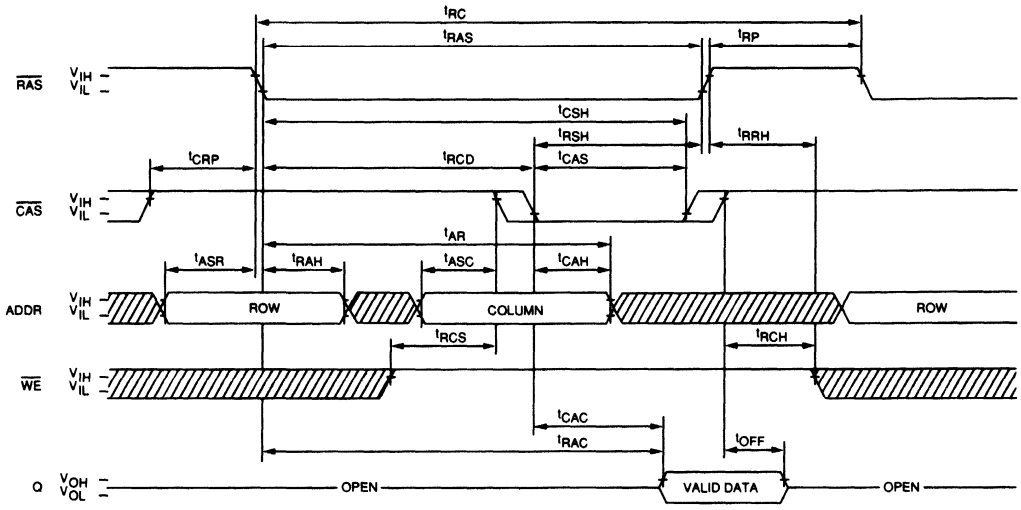
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	180		220		255		295		ns	
PAGE-MODE cycle time	^tPC	75		90		100		120		ns	6, 7
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		40		50		60		75	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	40		50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	60		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	40	10,000	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	20		25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	25		30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ set-up time	^tCRP	10		15		20		20		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	15		15		15		15		ns	
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	^tAR	50		70		80		100		ns	
READ command set-up time	^tRCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	^tRCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	^tRRH	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	25	0	30	0	30	0	35	ns	12
$\overline{WE}$ command set-up time	^tWCS	0		0		0		0		ns	16
WRITE command hold time	^tWCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	^tWCR	35		85		100		120		ns	
WRITE command pulse width	^tWP	15		35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	35		35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	35		35		40		45		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	15
Data-in hold time	^tDH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	^tDHR	35		85		100		120		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	30		40		50		60		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	70		90		110		135		ns	16
Transition time (rise or fall)	^tT	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^tREF		4		4		4		4	ms	21
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	^tCHR	15		20		25		30		ns	20
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$) refresh	^tCSR	10		15		20		20		ns	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		0		ns	20

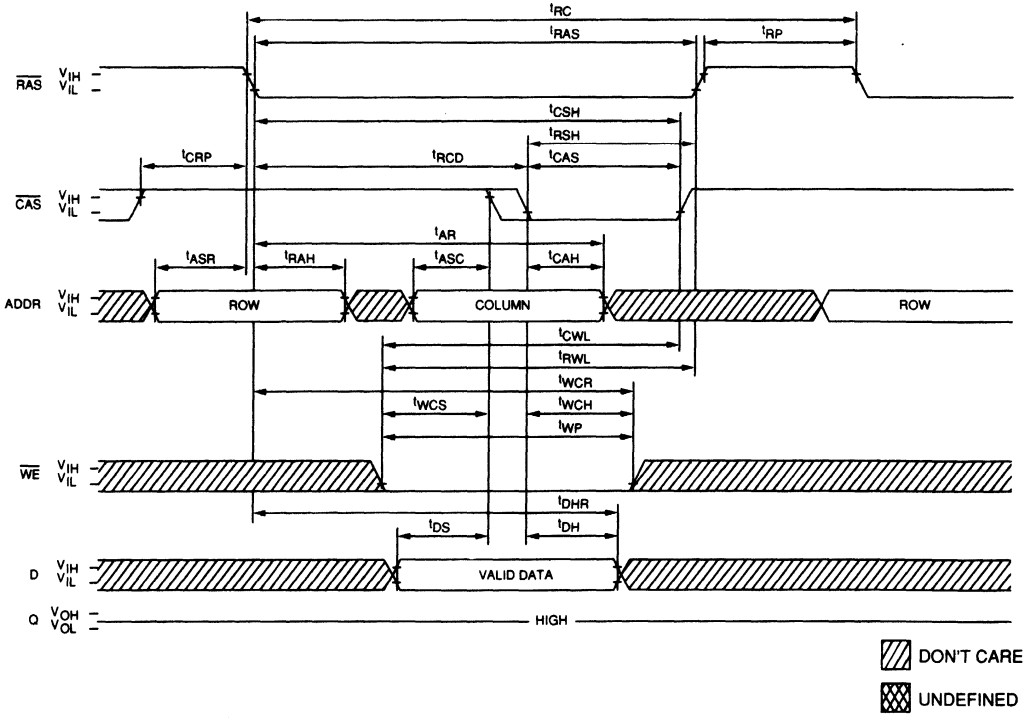
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq ^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \geq ^tCWD$ (min) and $^tRWD \geq ^tRWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. On-chip refresh and address counters are enabled.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

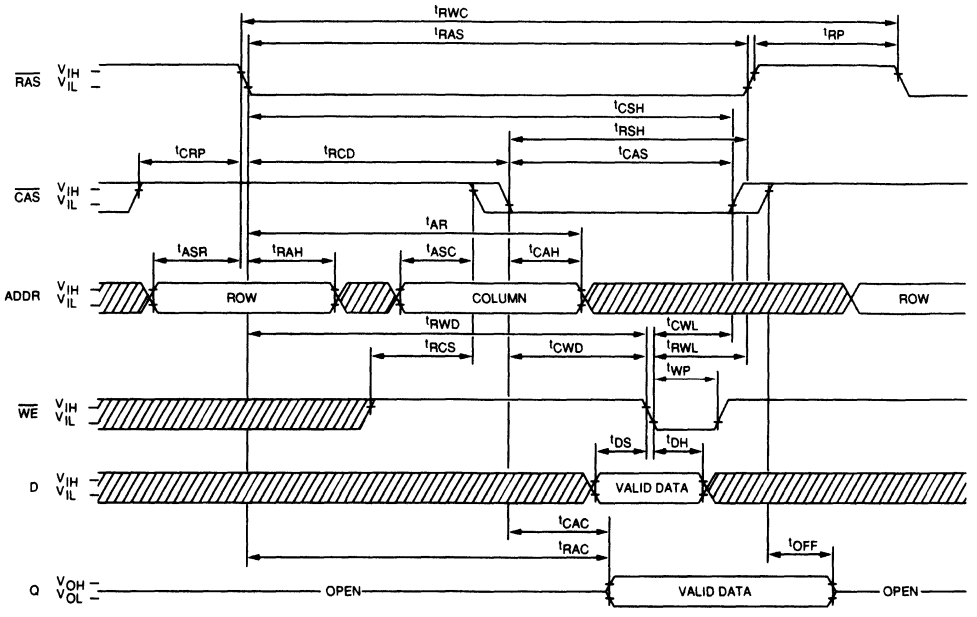
READ CYCLE



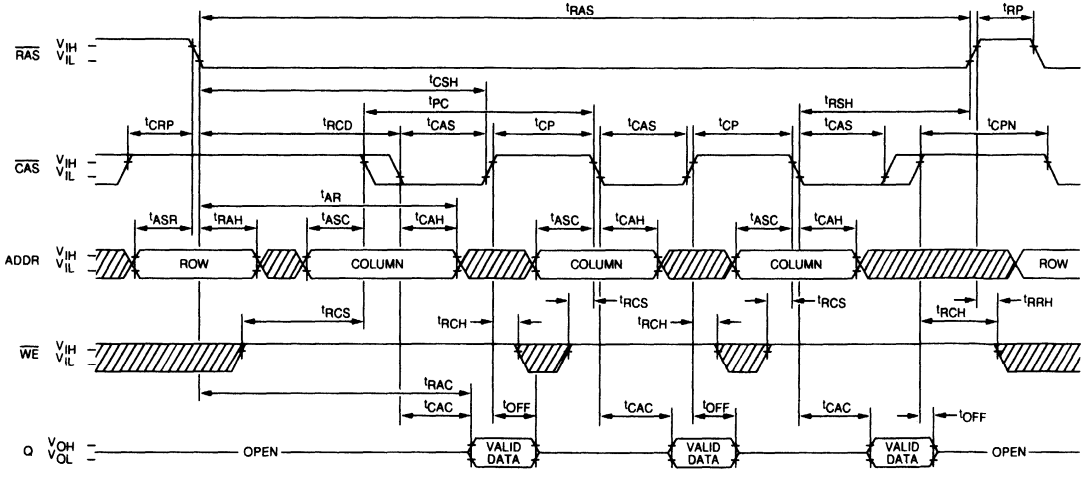
EARLY-WRITE CYCLE



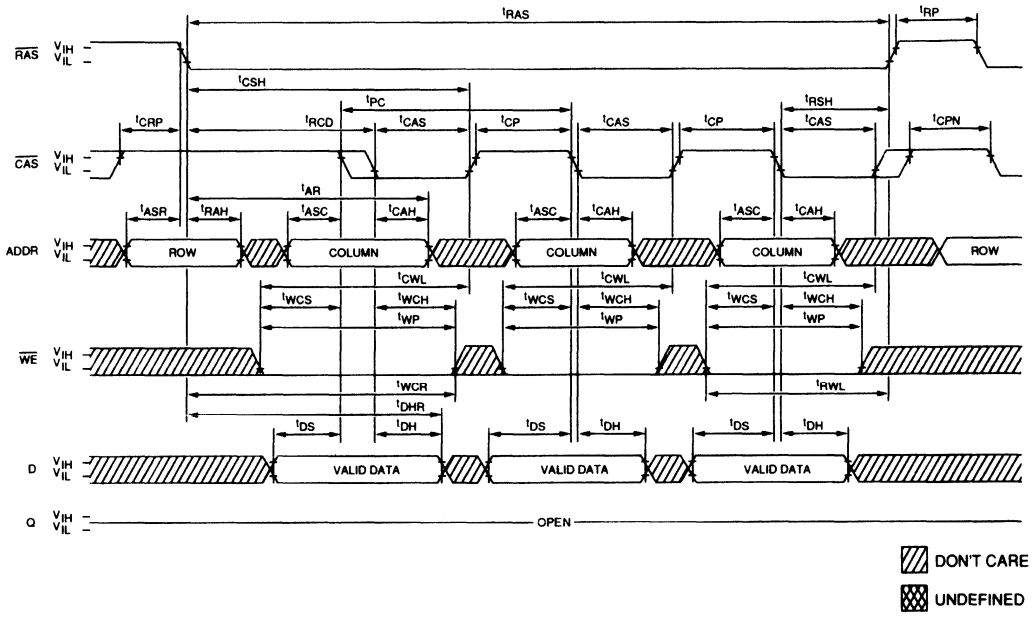
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE

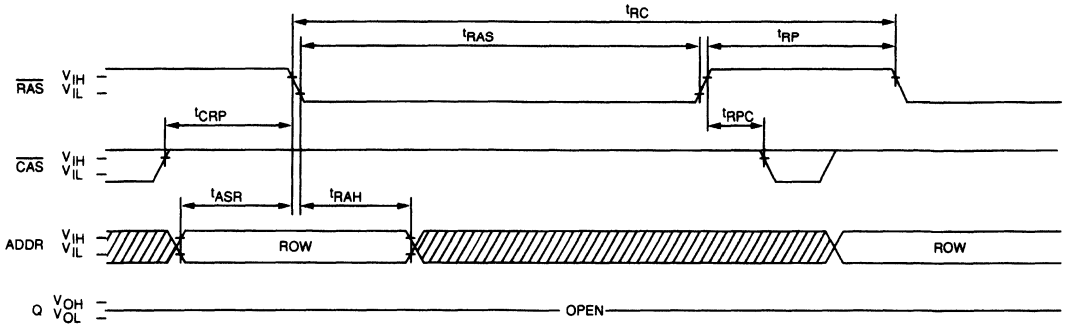


PAGE-MODE EARLY-WRITE CYCLE



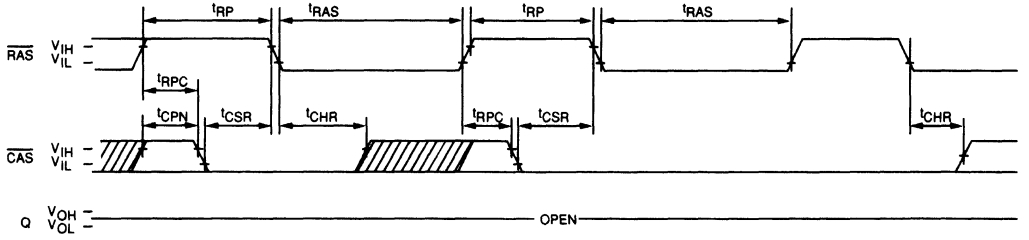
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{WE}$ = DON'T CARE.)



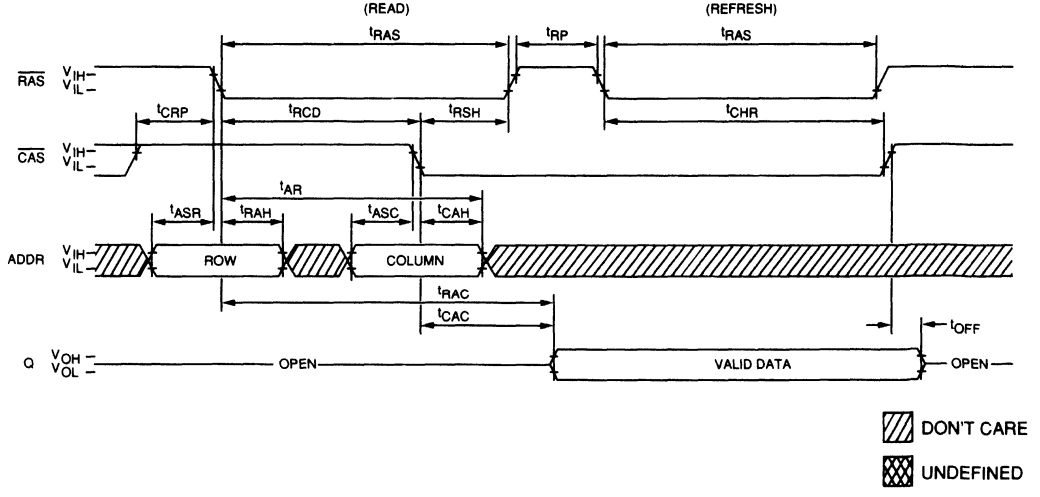
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_8 and $\overline{WE}$ = DON'T CARE.)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[21]



DRAM MODULE

1MEG x 8 DRAM

FAST PAGE MODE

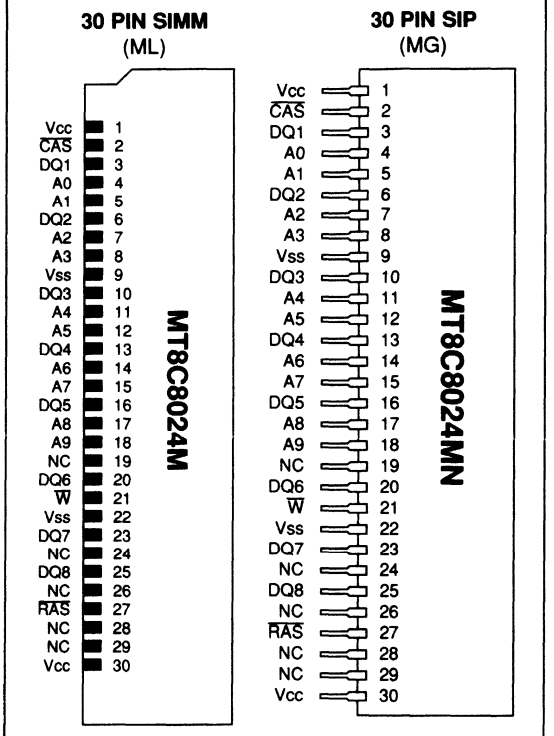
FEATURES

- Industry standard pin-out in a 30-pin single-in-line package
- High performance CMOS silicon gate process
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 40mW standby; 1400mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512 cycle refresh distributed across 8ms
- Optional Fast Page Mode

OPTIONS

	MARKING
• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages:	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	MN

PIN ASSIGNMENT (Top View)



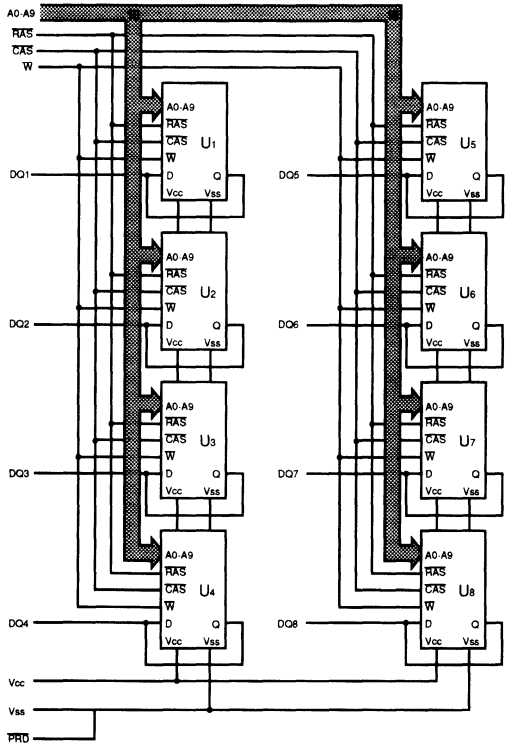
GENERAL DESCRIPTION

The MT8C8024 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x8 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM



U1 - U8 = MT4C1024DJ

TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 8 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-80	80	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-80	80	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		400	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		400	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		16	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or Vss + 0.2V)	I_{CC4}		8	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		280	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		280	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		40	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		56	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	160		190		220		ns	
READ-WRITE cycle time	^tRWC	185		220		255		ns	
FAST PAGE-MODE READ or WRITE cycle time	^tPC	45		55		70		ns	
FAST PAGE-MODE READ-WRITE cycle time	^tPRWC	70		85		105		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		30	ns	15
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		55		65	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		25		30		ns	
$\overline{RAS}$ precharge time	^tRP	70		80		90		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	15		15		20		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	25	75	25	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	12		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	17	40	20	50	20	60	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		85		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	35	ns	20
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

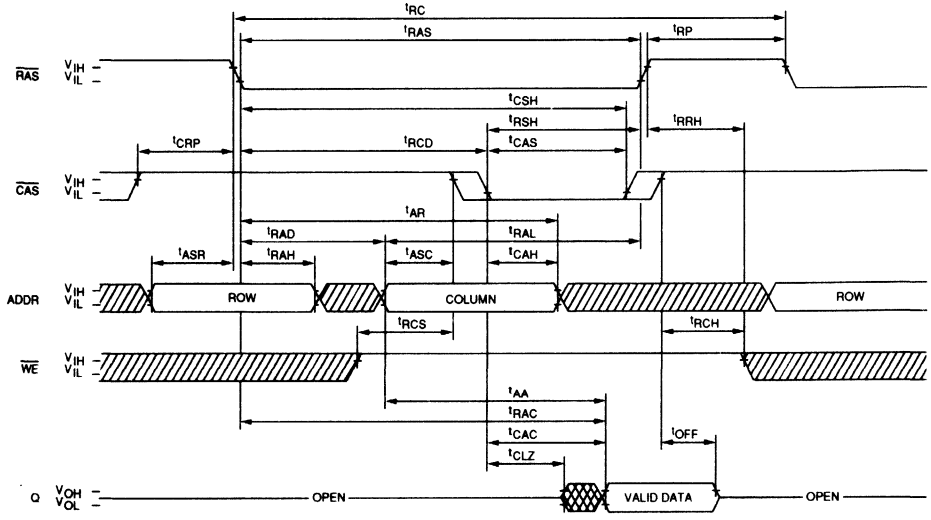
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		85		ns	
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	20		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		100		120		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		25		30		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5

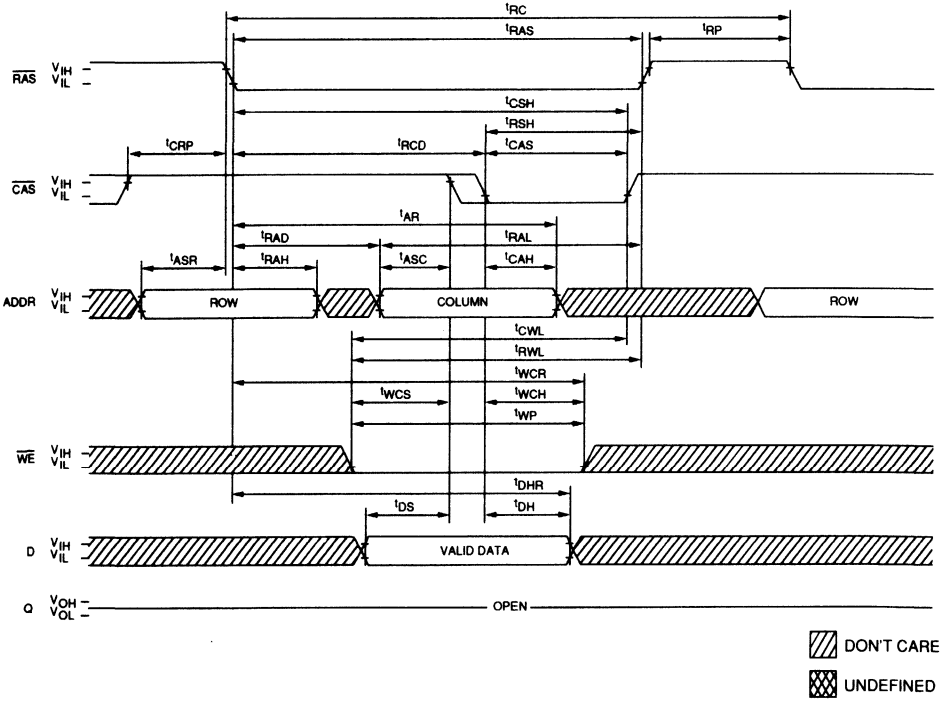
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \geq {}^tRWD$ (min), $^tAWD \geq {}^tAWD$ (min) and $^tCWD \geq {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.
24. All other inputs equal Vcc -0.2V.

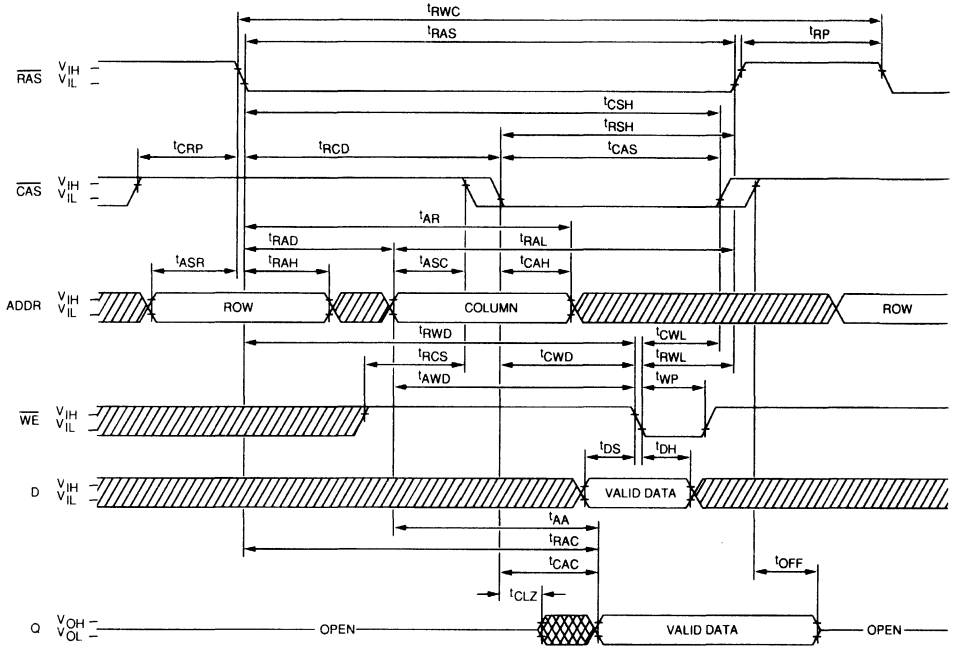
READ CYCLE



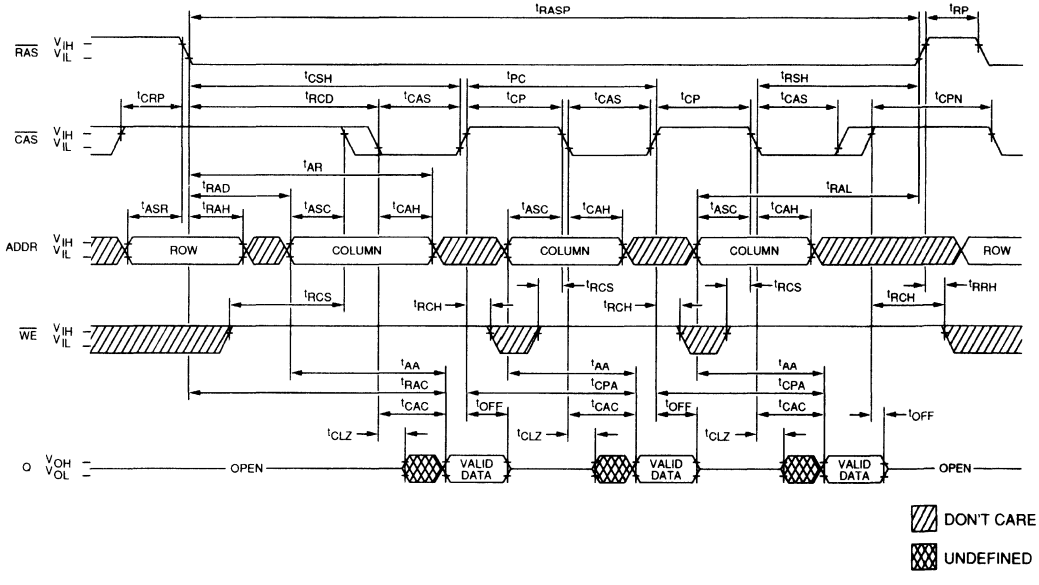
EARLY-WRITE CYCLE



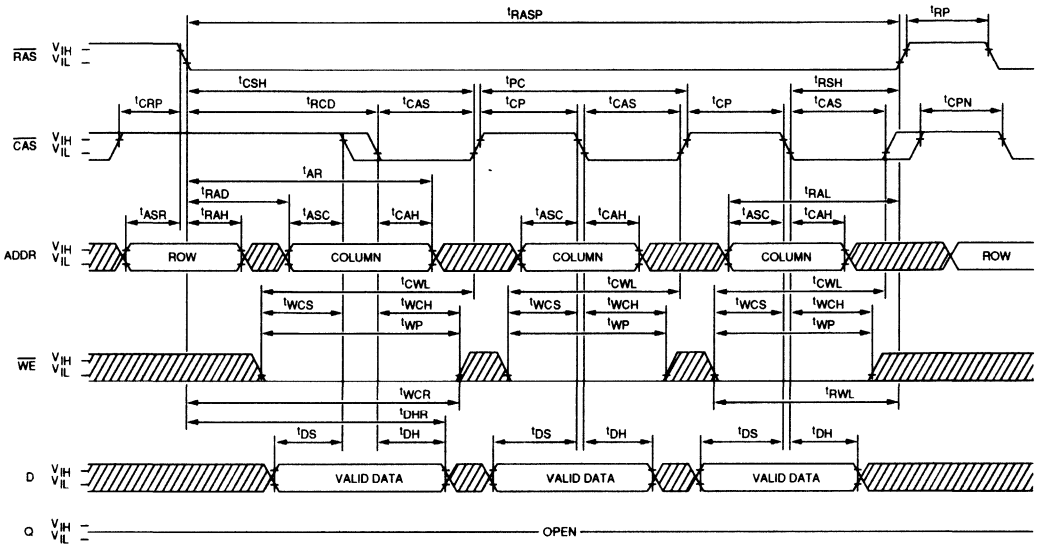
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



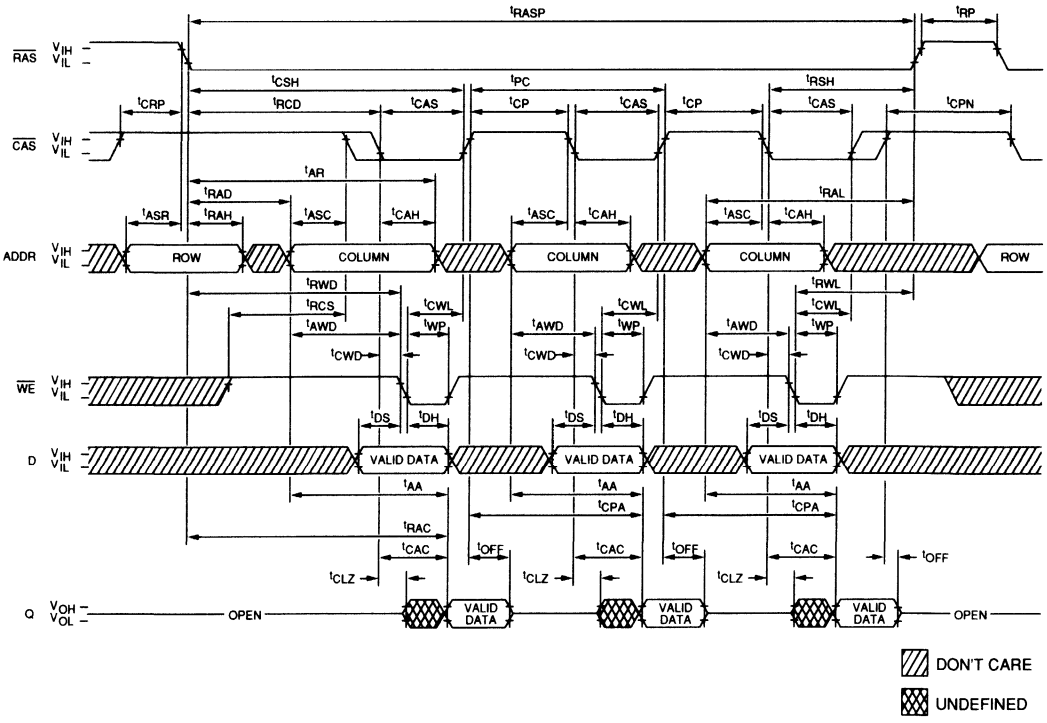
PAGE-MODE READ CYCLE



PAGE-MODE EARLY-WRITE CYCLE

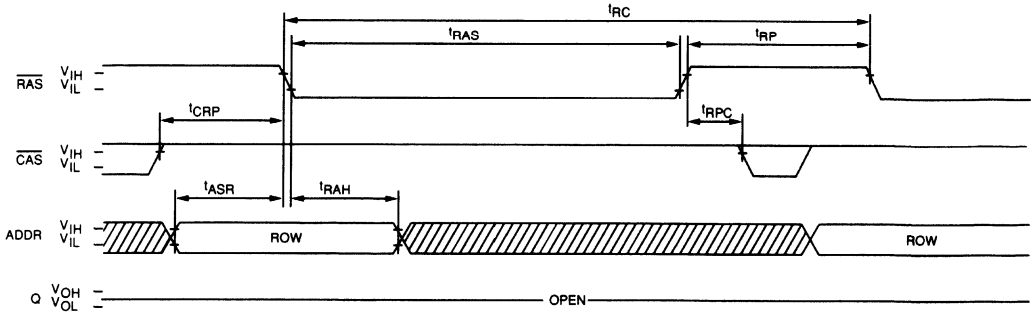


PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



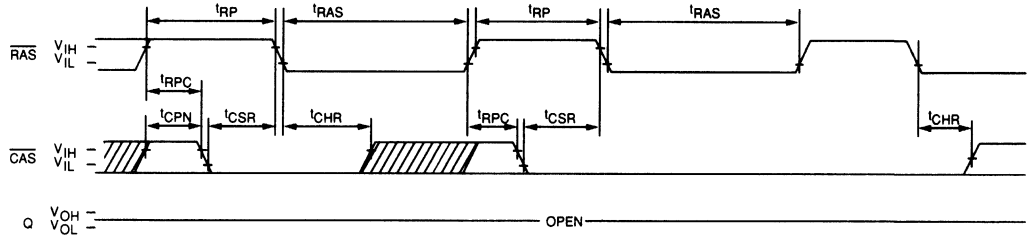
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



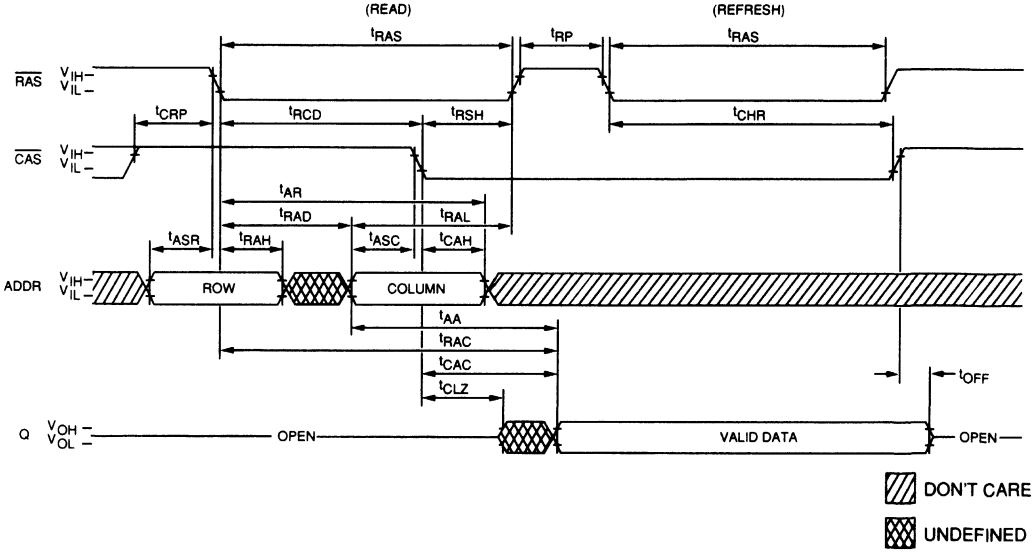
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[23]



DRAM MODULE

1MEG x 8 DRAM

LOW PROFILE

FEATURES

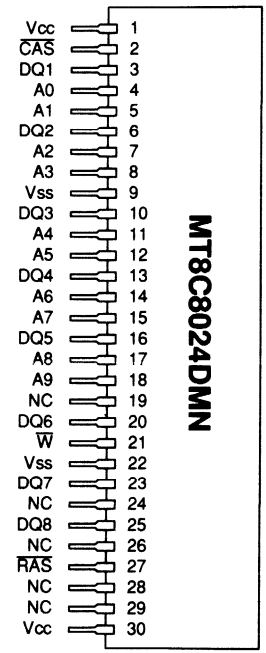
- Industry standard pin-out in a 30-pin single-in-line package
- High performance CMOS silicon gate process
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 40mW standby; 1400mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512 cycle refresh distributed across 8ms
- Optional Fast Page Mode

OPTIONS MARKING

• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages:	
Leaded 30-pin SIP	DMN

PIN ASSIGNMENT (Top View)

30 PIN SIP
(MI)



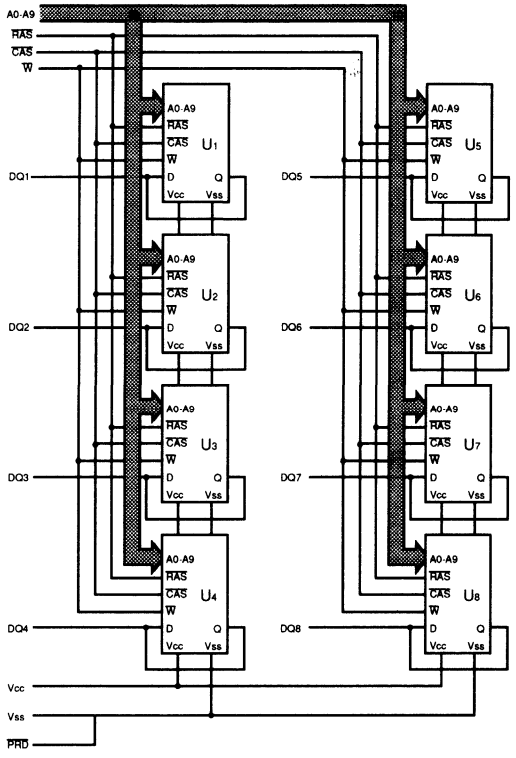
GENERAL DESCRIPTION

The MT8C8024 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x8 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM



U1 - U8 = MT4C1024DJ

TRUTH TABLE

Function	RAS	CAS	WE	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 8 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-80	80	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-80	80	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		400	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		400	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		16	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		8	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		280	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		280	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		40	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		56	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	160		190		220		ns	
READ-WRITE cycle time	^tRWC	185		220		255		ns	
FAST PAGE-MODE READ or WRITE cycle time	^tPC	45		55		70		ns	
FAST PAGE-MODE READ-WRITE cycle time	^tPRWC	70		85		105		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		30	ns	15
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		55		65	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		25		30		ns	
$\overline{RAS}$ precharge time	^tRP	70		80		90		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	15		15		20		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	25	75	25	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	12		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	17	40	20	50	20	60	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		85		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	35	ns	20
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

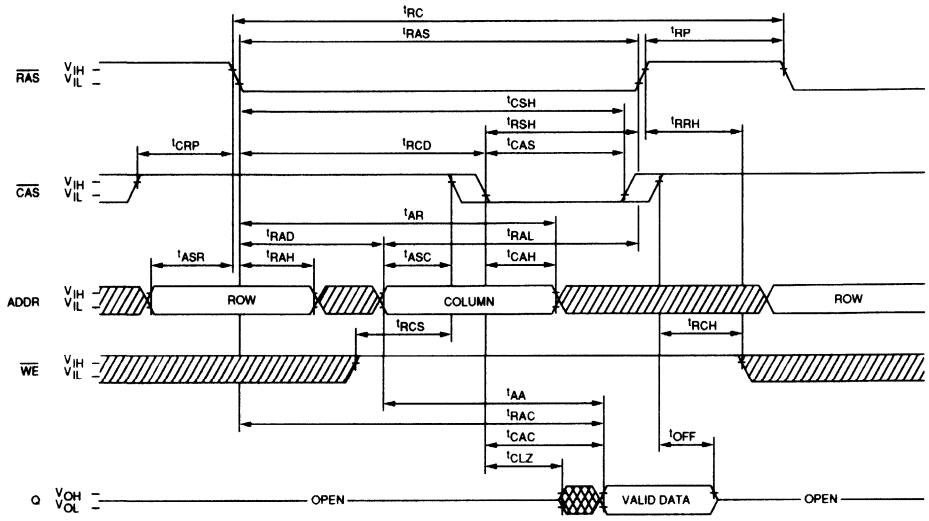
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		85		ns	
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	20		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		100		120		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		25		30		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5

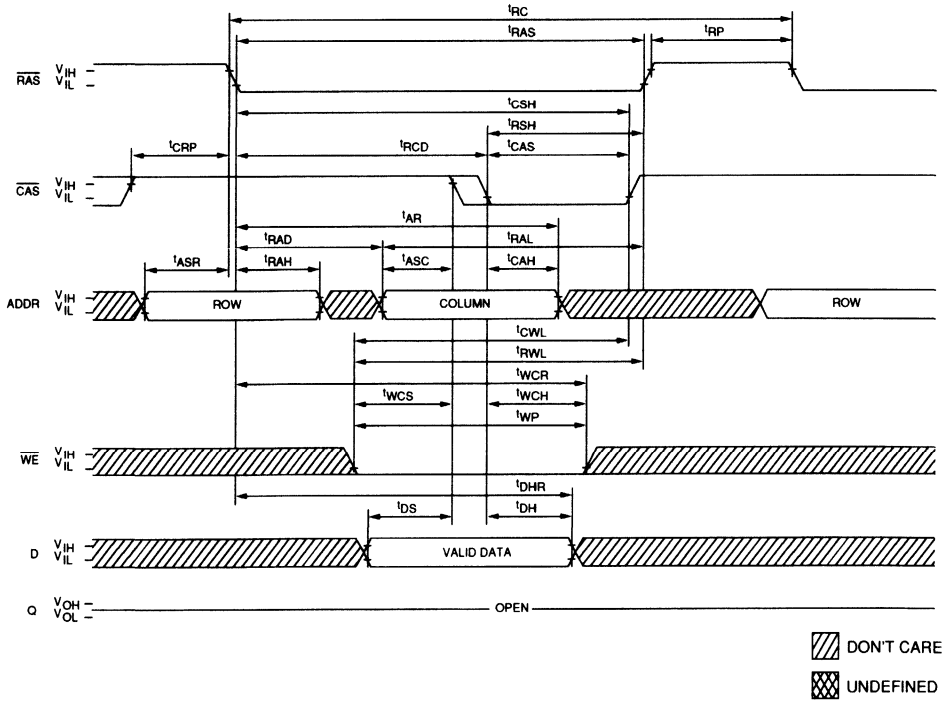
NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and Vcc = 5V.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. VIH min and VIL max are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If $\overline{CAS}$ = VIH, data output is high impedance.
12. If $\overline{CAS}$ = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \ge {}^tRWD$ (min), $^tAWD \ge {}^tAWD$ (min) and $^tCWD \ge {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to VIH) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.
24. All other inputs equal Vcc -0.2V.

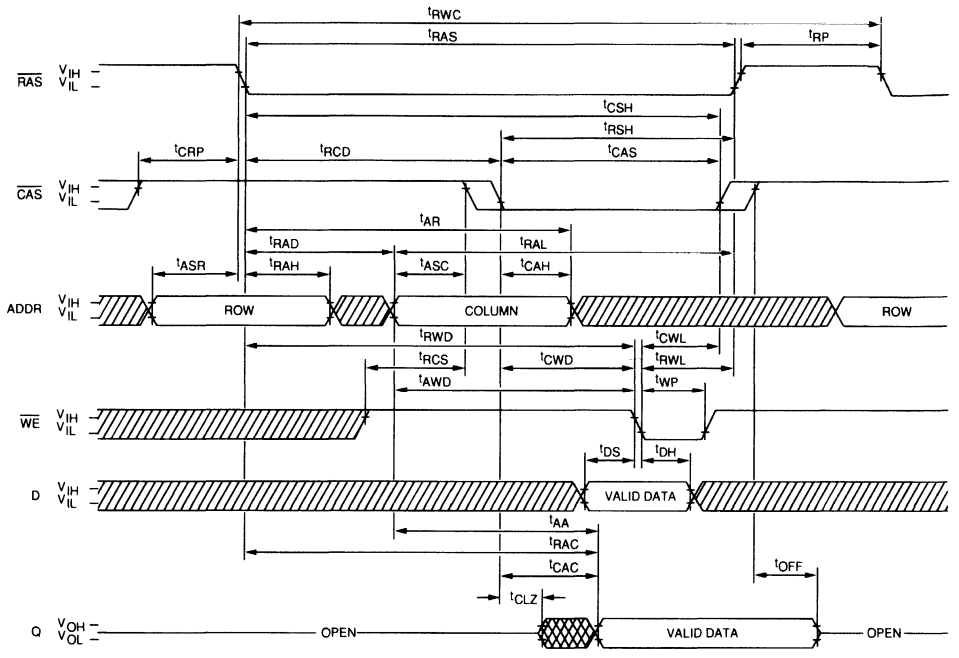
READ CYCLE



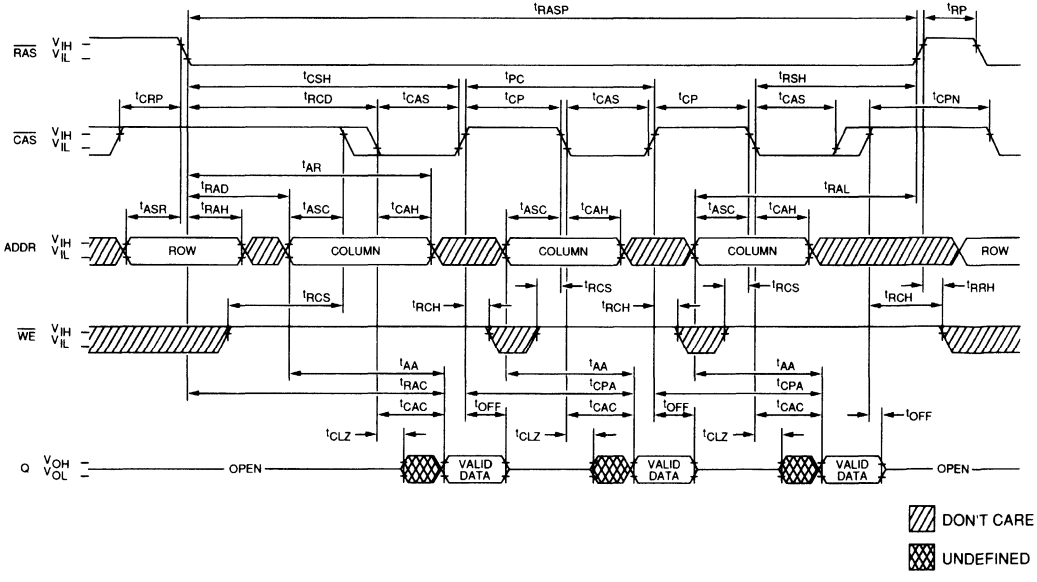
EARLY-WRITE CYCLE



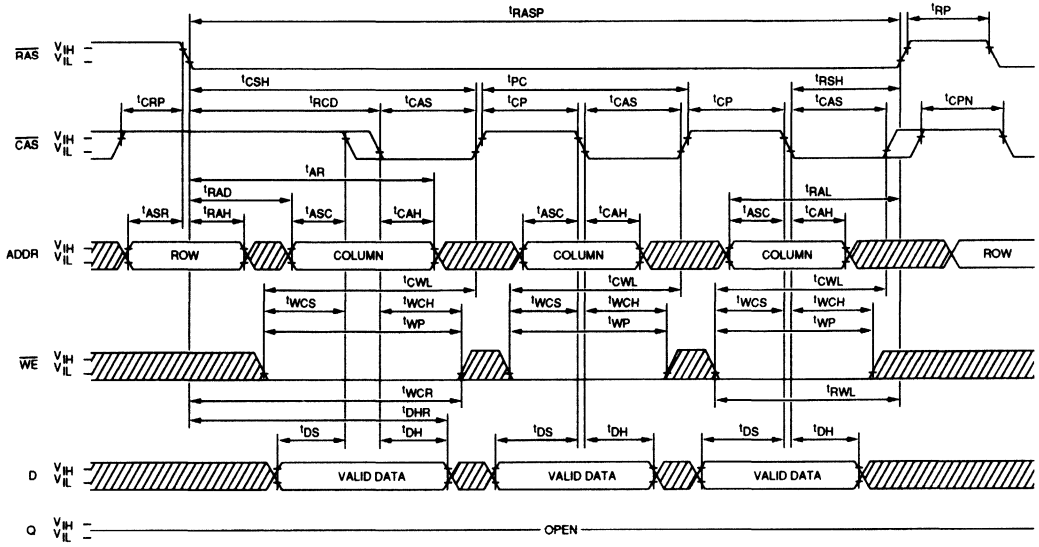
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



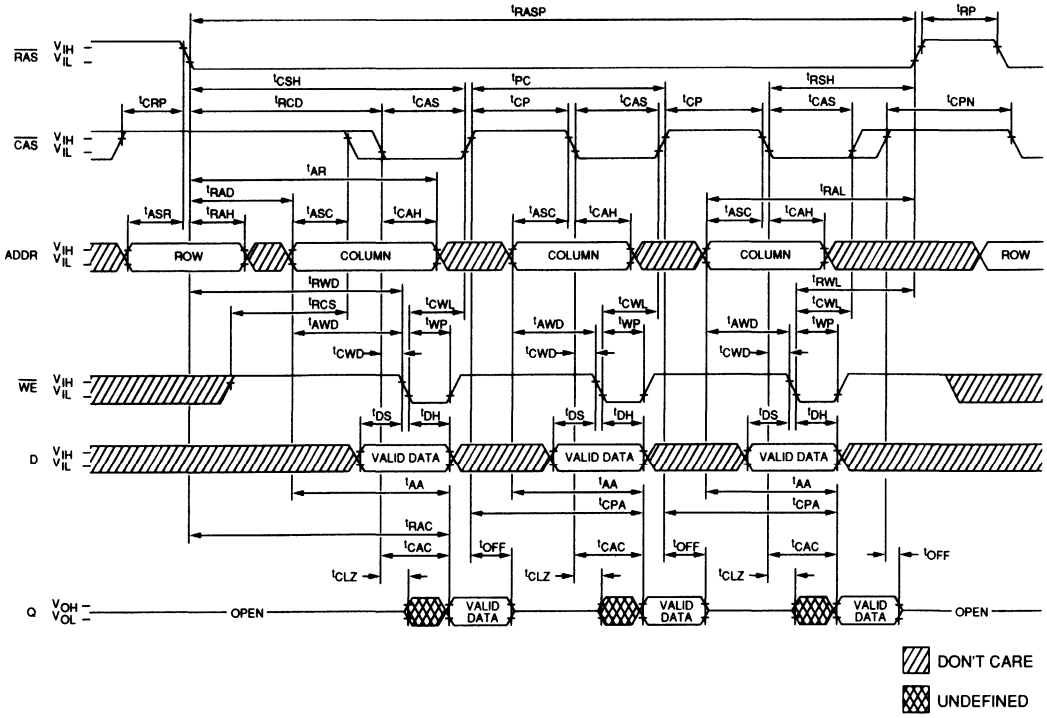
PAGE-MODE READ CYCLE



PAGE-MODE EARLY-WRITE CYCLE

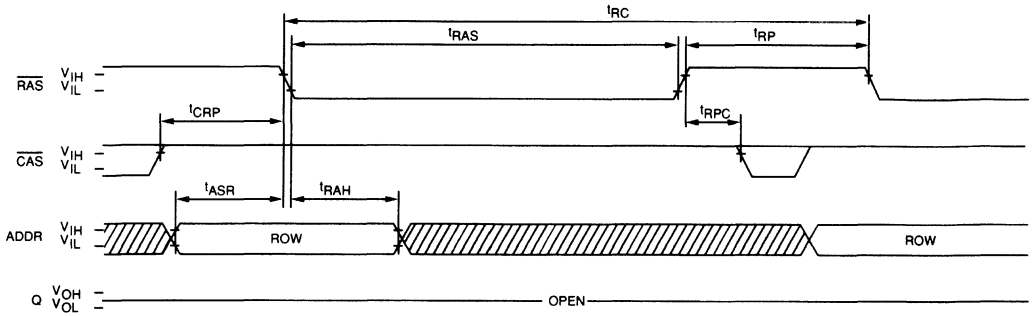


PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



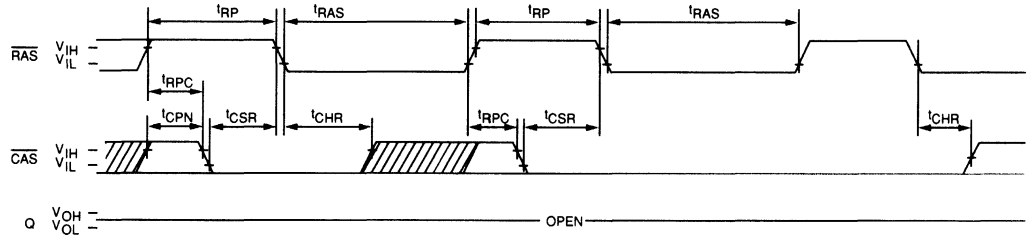
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



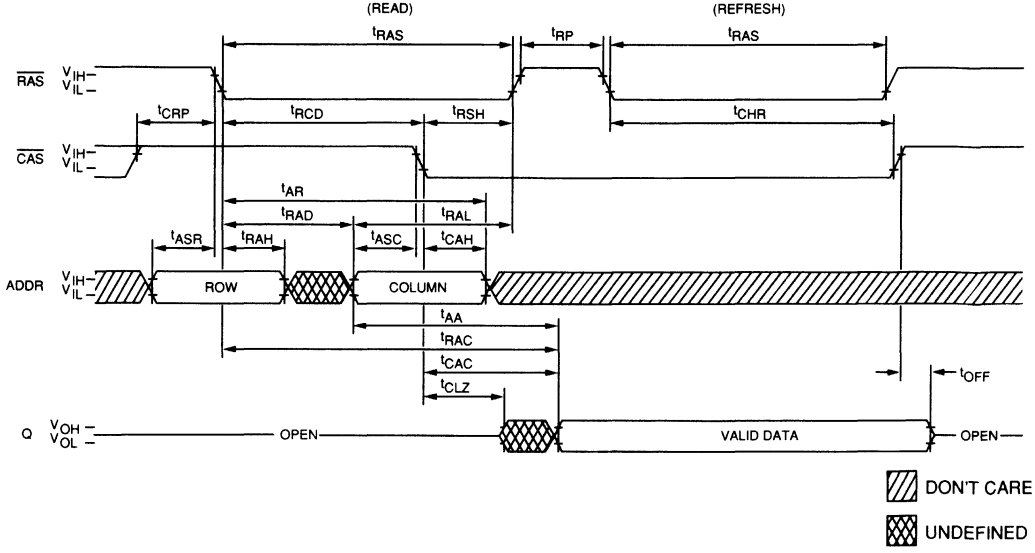
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



DRAM MODULE

1MEG x 8 DRAM

NIBBLE MODE

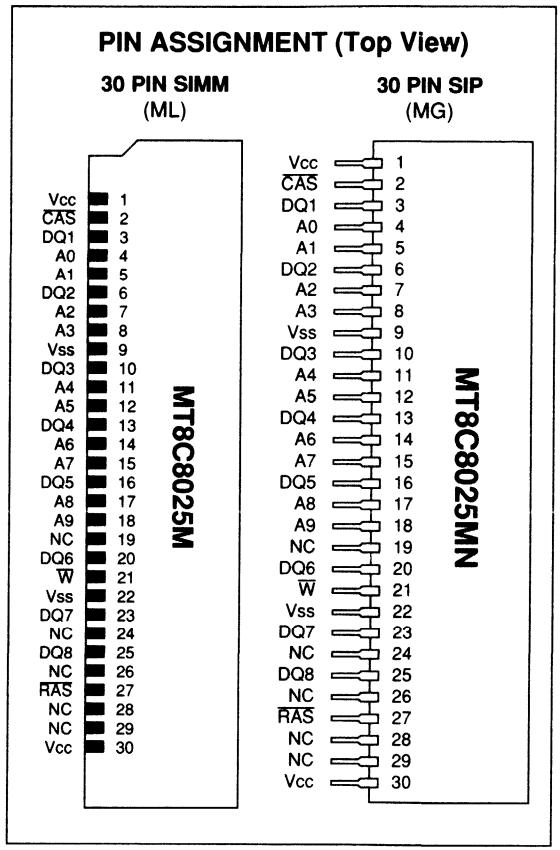
FEATURES

- Industry standard pin-out in a 30-pin single-in-line package
- High performance CMOS silicon gate process
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 45mW standby; 1575mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512 cycle refresh distributed across 8ms.
- Optional Nibble access mode.

OPTIONS MARKING

• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages:	
Leaded 30-pin SIP	MN
Leadless 30-pin SIMM	M

PIN ASSIGNMENT (Top View)

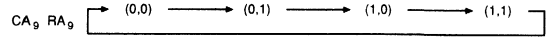


GENERAL DESCRIPTION

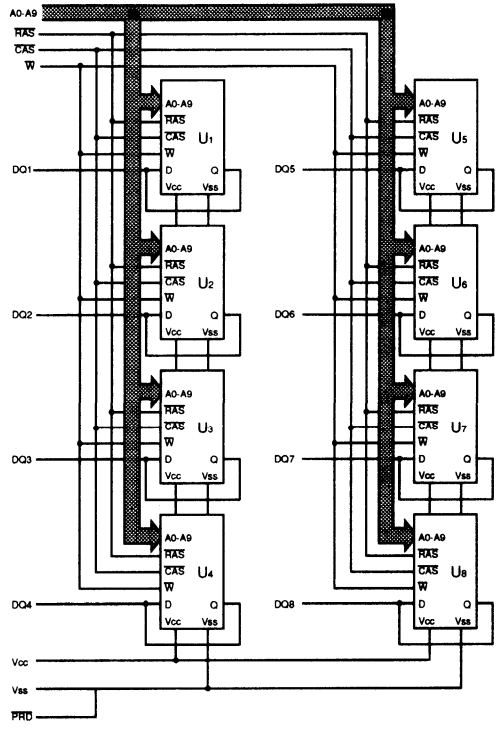
The MT8C8025 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

NIBBLE MODE operation allows faster sequential serial data operations (READ, WRITE or READ-MODIFY-WRITE) on up to 4 bits. The first of 4 bits is accessed in the usual manner with $\overline{CAS}$ address A9 (nibble MSB) and $\overline{RAS}$ address A9 (nibble LSB) selecting on of 4 bits within a nibble for initial access. By holding $\overline{RAS}$ LOW, $\overline{CAS}$ can be toggled incrementing the nibble address field in modulo 4 fashion with wrap around (see below).



FUNCTIONAL BLOCK DIAGRAM



U1 - U8 = MT4C1025DJ

TRUTH TABLE

Function	RAS	CAS	WE	TF	Addresses tR	Addresses tC		NOTES
Standby	H	H	H	GND/NC	X	X	High Impedance	
READ	L	L	H	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	GND/NC	ROW	COL	Data In	
NIBBLE MODE READ	L	H→L→H	H	GND/NC	ROW	COL	Valid Data Out, Valid Data Out	
NIBBLE MODE WRITE	L	H→L→H	L	GND/NC	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	H	H	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	GND/NC	X	X	High Impedance	
TEST FUNCTION	L	L	H	H	ROW	COL	Data Out, Test Function Mode	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 8 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-80	80	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-80	80	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		400	mA	3, 4
OPERATING CURRENT: NIBBLE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		400	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		16	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		8	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		280	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		280	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_9	C_{I1}		40	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		56	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$; $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	150		180		220		ns	
READ-MODIFY-WRITE cycle time	t_{RWC}	175		210		255		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		25		30	ns	15
Access time from column address	t_{AA}		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		55		65	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{RAS}$ precharge time	t_{RP}	60		80		90		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		20		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	60	10	75	15	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		10		15		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		20		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	40	20	50	15	60	ns	18
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	60		75		110		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		50		60		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	25	ns	20
$\overline{WE}$ command set-up time	t_{WCS}	0		0		0		ns	21
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	t_{WCR}	60		75		80		ns	
Write command pulse width	t_{WP}	15		20		25		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

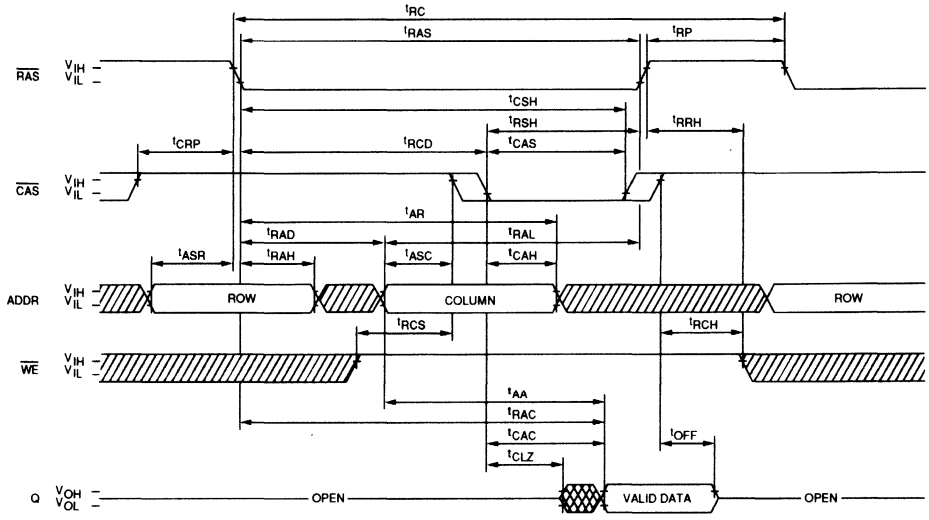
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		110		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		100		120		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		25		35		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5
$\overline{RAS}$ pulse width (NIBBLE MODE)	^tRASN	80	100,000	100	100,000	120	100,000	ns	
$\overline{CAS}$ precharge time (NIBBLE MODE)	^tNCP	10		10		15		ns	
NIBBLE MODE cycle time	^tNC	40		45		55		ns	
NIBBLE MODE READ-MODIFY-WRITE cycle time	^tNRWC	65		75		85		ns	
NIBBLE MODE access time	^tNCAC		20		20		35	ns	15
NIBBLE MODE pulse width	^tNCAS	20		25		35		ns	
NIBBLE MODE $\overline{CAS}$ precharge time	^tNCP	10		10		10		ns	
NIBBLE MODE $\overline{RAS}$ hold time	^tNRSH	20		25		30		ns	
NIBBLE MODE $\overline{CAS}$ to $\overline{WE}$ delay time	^tNCWD	20		25		35		ns	
NIBBLE MODE $\overline{WE}$ command to $\overline{RAS}$ lead time	^tNRWL	20		25		30		ns	
NIBBLE MODE $\overline{WE}$ command to $\overline{CAS}$ lead time	^tNCWL	20		25		30		ns	

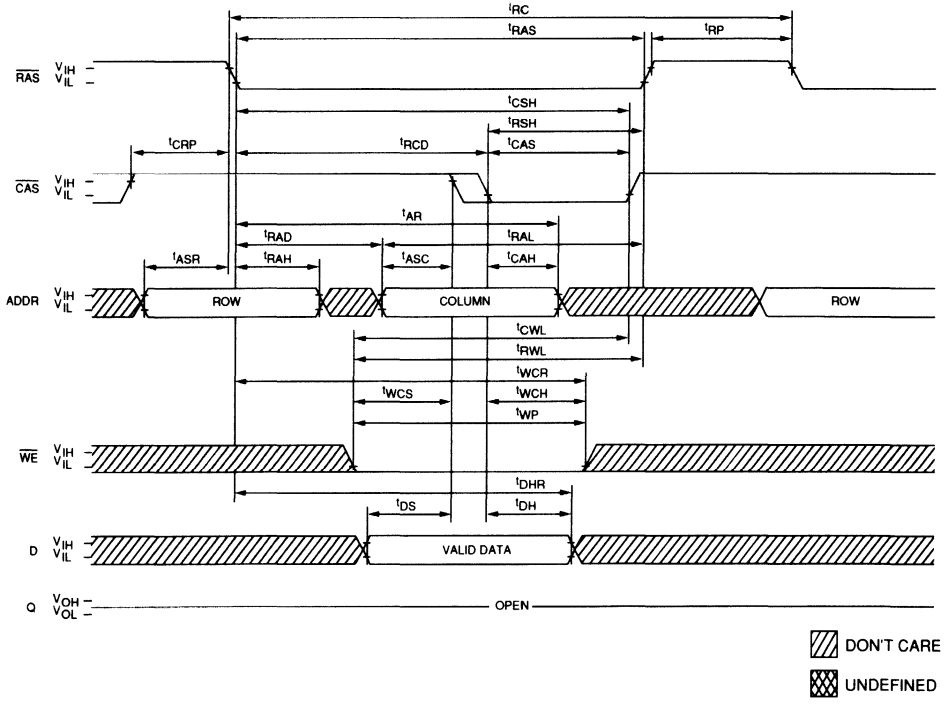
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq ^tRWD$ (min), $^tAWD \geq ^tAWD$ (min) and $^tCWD \geq ^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

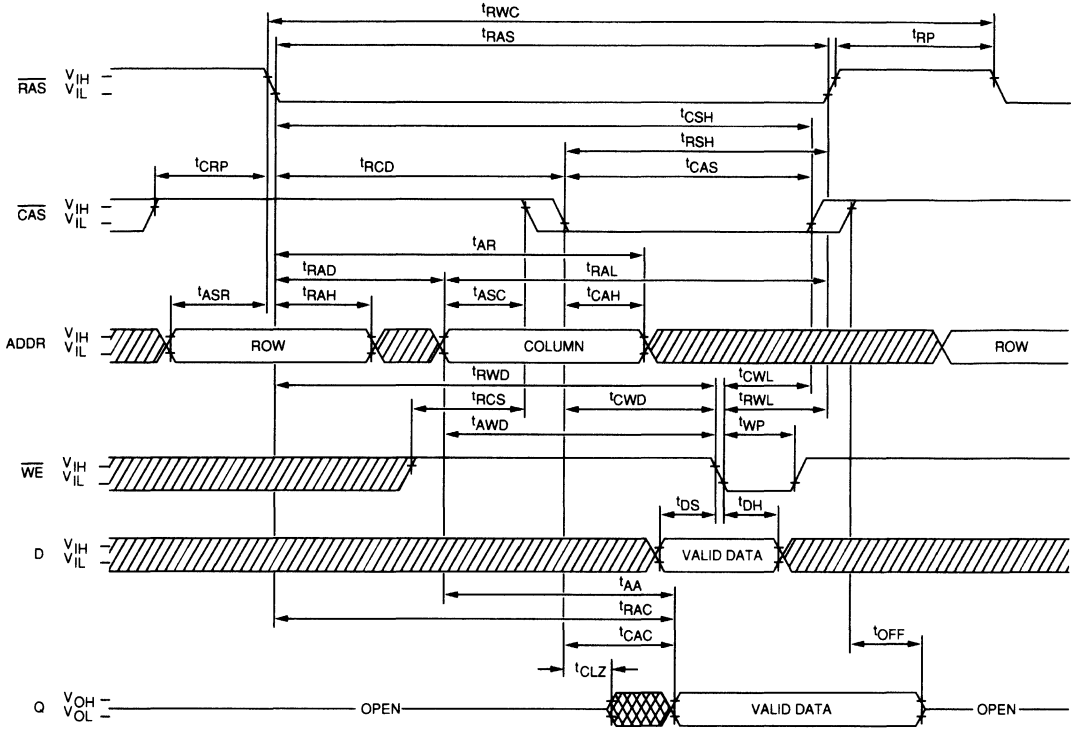
READ CYCLE



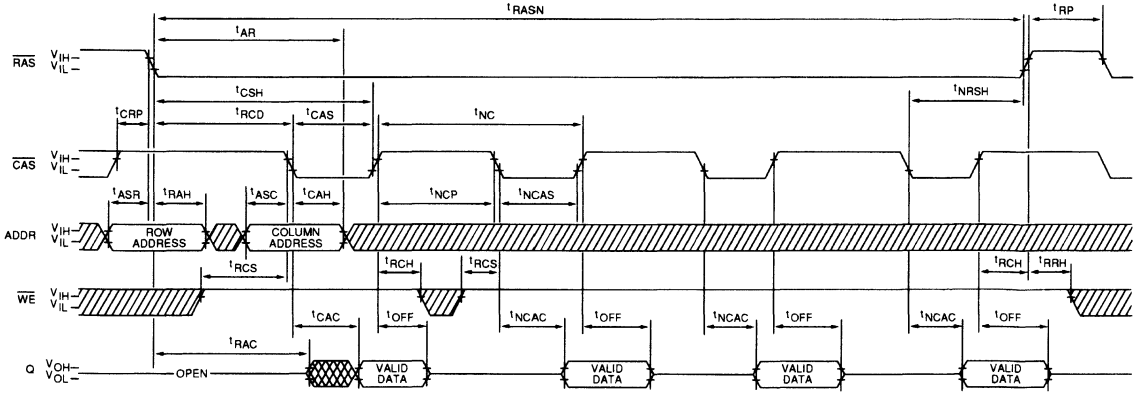
EARLY-WRITE CYCLE



READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



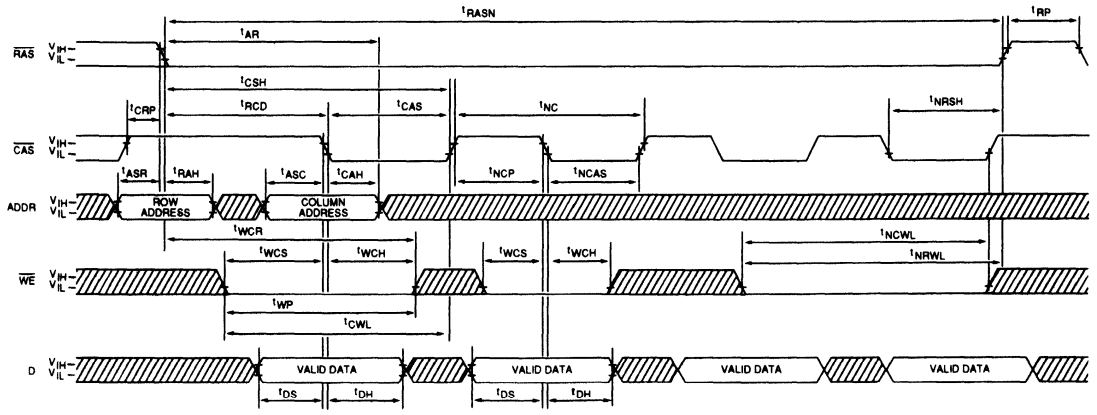
NIBBLE MODE READ CYCLE



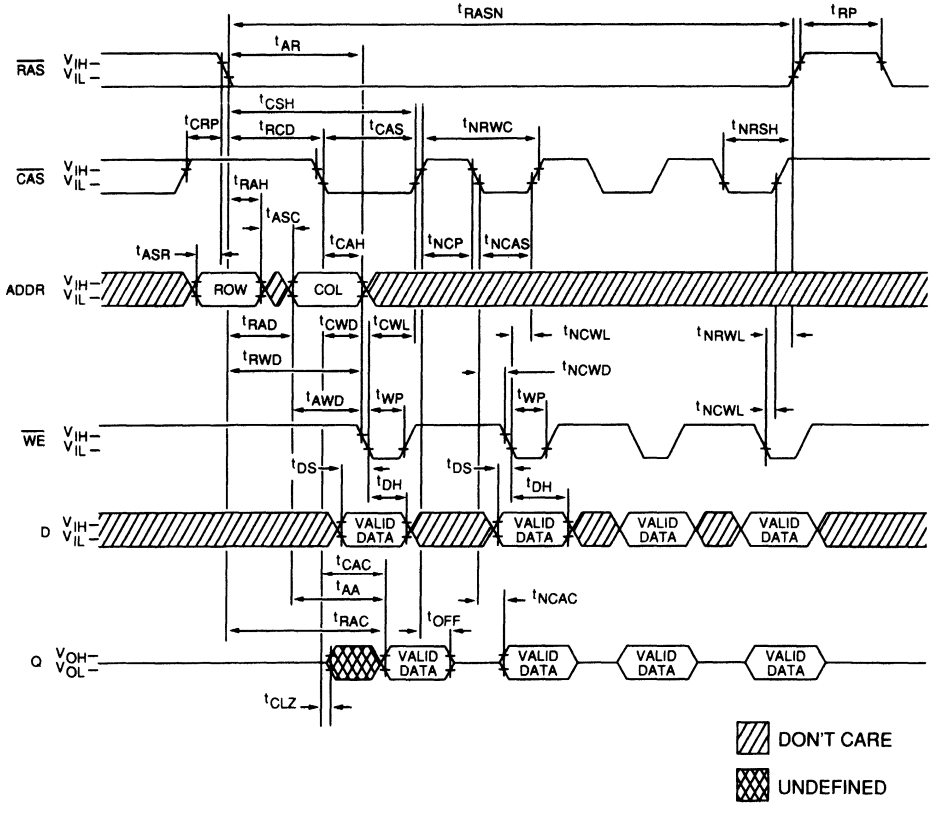
DON'T CARE

UNDEFINED

NIBBLE MODE EARLY-WRITE CYCLE

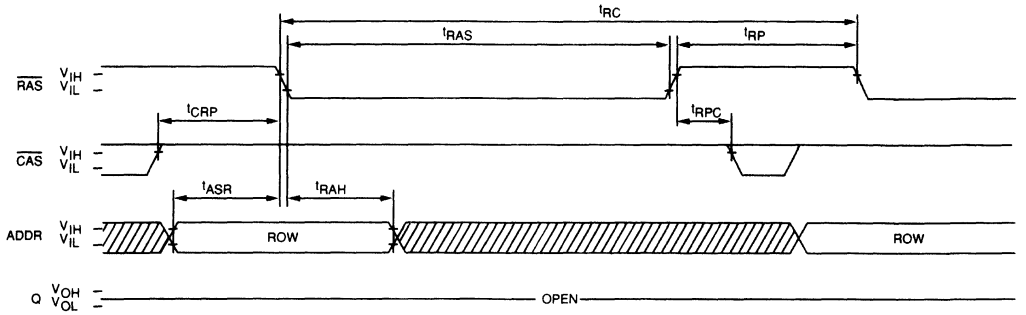


NIBBLE MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



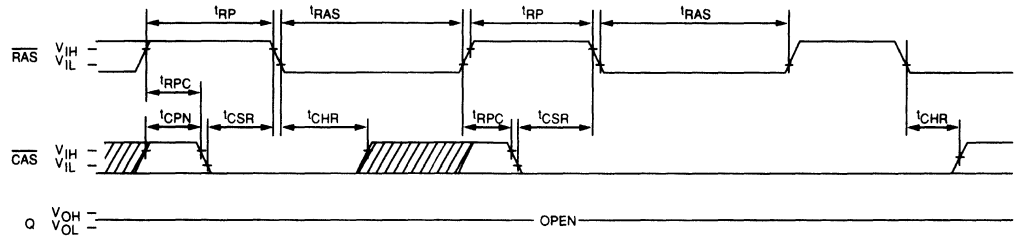
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



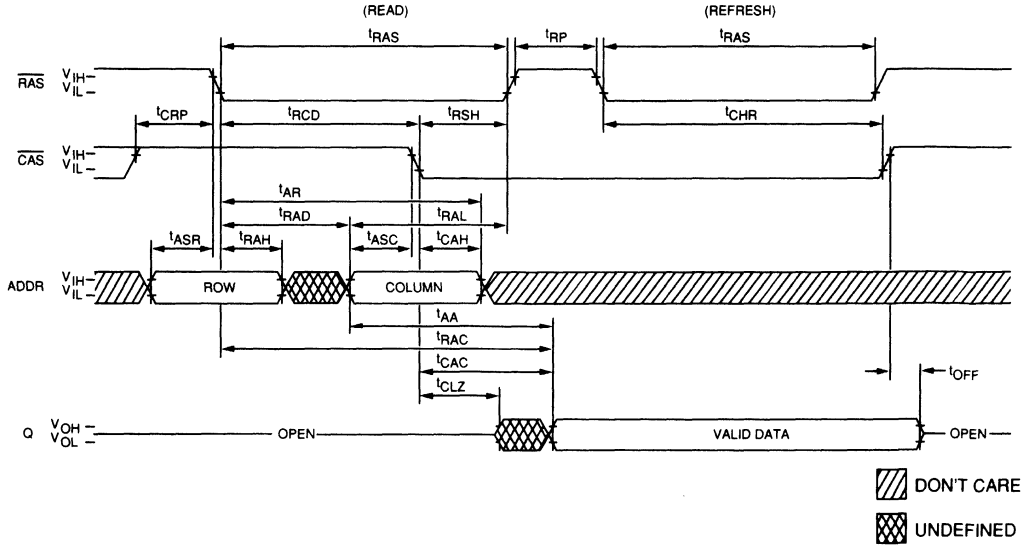
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)



DRAM MODULE

1MEG x 8 DRAM

STATIC COLUMN

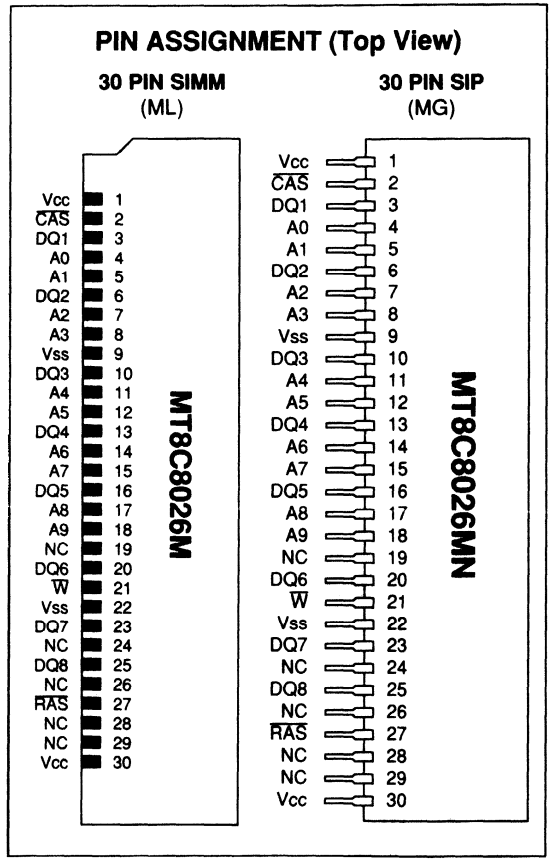
FEATURES

- Industry standard pin-out in a 30-pin single-in-line package
- High performance CMOS silicon gate process.
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 45mW standby; 1575mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512 cycle refresh distributed across 8ms
- Optional Static Column access mode

OPTIONS MARKING

• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages:	
Leaded 30-pin SIP	MN
Leadless 30-pin SIMM	M

PIN ASSIGNMENT (Top View)



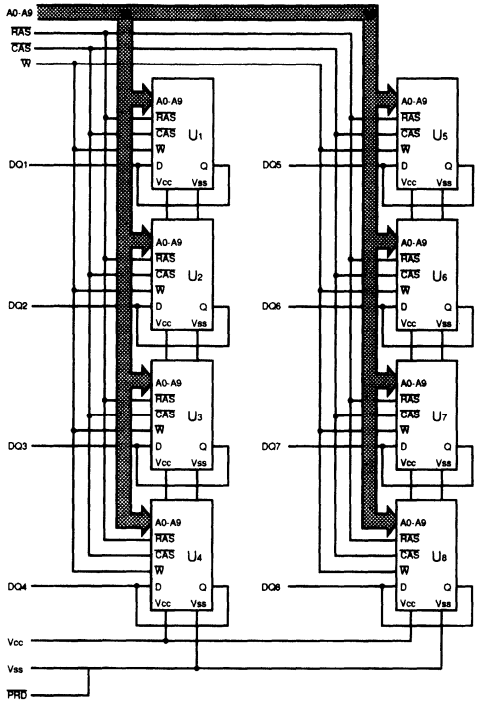
GENERAL DESCRIPTION

The MT8C8026 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x1 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

FUNCTIONAL BLOCK DIAGRAM



U1 - U8 = MT4C1026DJ

TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	TF	Addresses			NOTES
					tR	tC		
Standby	H	H	H	GND/NC	X	X	High Impedance	
READ	L	L	H	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	GND/NC	ROW	COL	Data In	
STATIC COLUMN READ	L	L	H	GND/NC	ROW	COL COL	Valid Data Out, Valid Data Out	
STATIC COLUMN WRITE	L	L	L	GND/NC	ROW	COL COL	Valid Data In, Valid Data Out	
$\overline{RAS}$ ONLY REFRESH	L	H	H	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	GND/NC	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	GND/NC	X	X	High Impedance	
TEST FUNCTION	L	L	H	H	ROW	COL	Data Out, Test Function Mode	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 8 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-80	80	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-80	80	µA	
OUTPUT LEVELS					
Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		400	mA	3, 4
OPERATING CURRENT: STATIC COLUMN ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		400	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		16	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		8	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		280	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		280	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_9	C_{I1}		40	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		56	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	150		180		220	ns		
READ-MODIFY-WRITE cycle time	^tRWC	175		210		255		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		30	ns	15
Access time from column address	^tAA		40		50		60	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		30		ns	
$\overline{RAS}$ precharge time	^tRP	60		70		90		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	10		15		20		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	25	75	15	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	40	20	50	20	60	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	90		115		115		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	25	ns	20
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		80		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

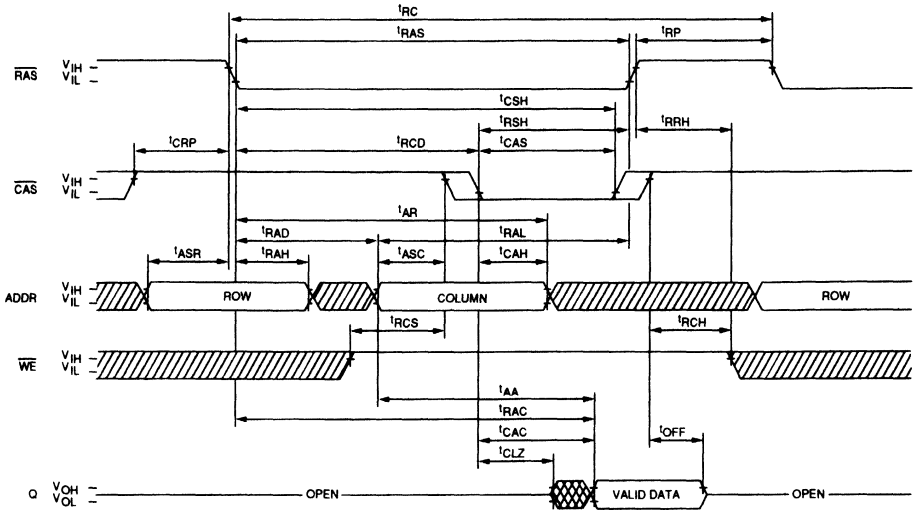
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
$\overline{WE}$ inactive time	^tWI	10		10		10		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		80		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		100		110		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		25		30		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	80	100,000	100	100,000	120	100,000	ns	
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		10		15		ns	
STATIC COLUMN MODE cycle time	^tSC	45		55		65		ns	
STATIC COLUMN READ-MODIFY-WRITE cycle time	^tSRMW	80		100		160		ns	
Last Write to column address delay time	^tLWAD	20	35	25	45	30	55	ns	
Last Write to column address hold time	^tAHLW	75		95		115		ns	
Output data hold time from column address	^tAOH	5		5		5		ns	
Output data enable from Write	^tOW		20		25		25	ns	

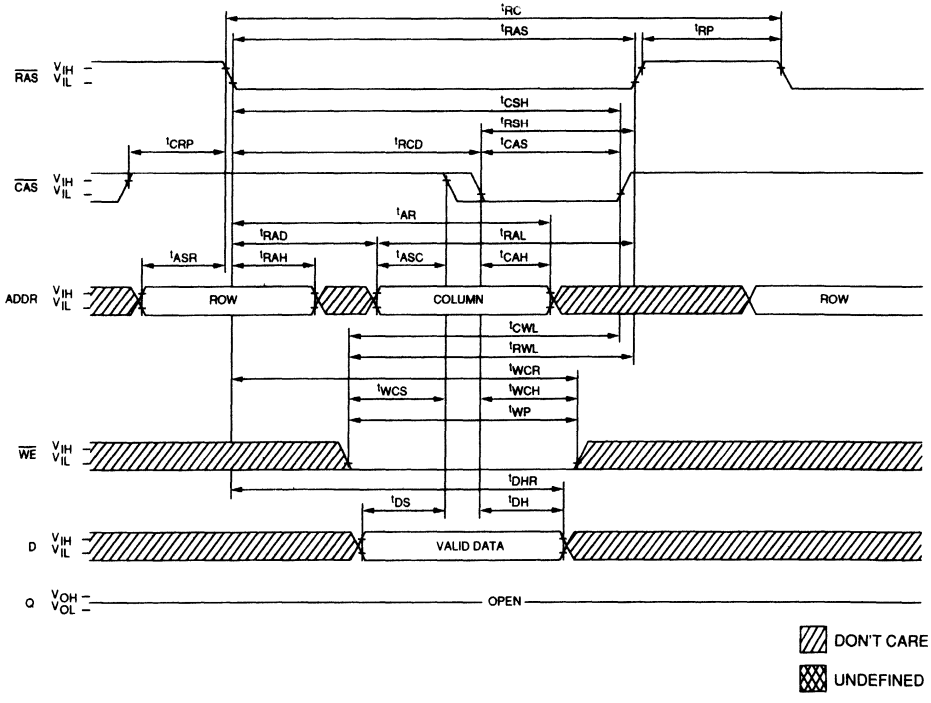
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \geq ^tRWD$ (min), $^tAWD \geq ^tAWD$ (min) and $^tCWD \geq ^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

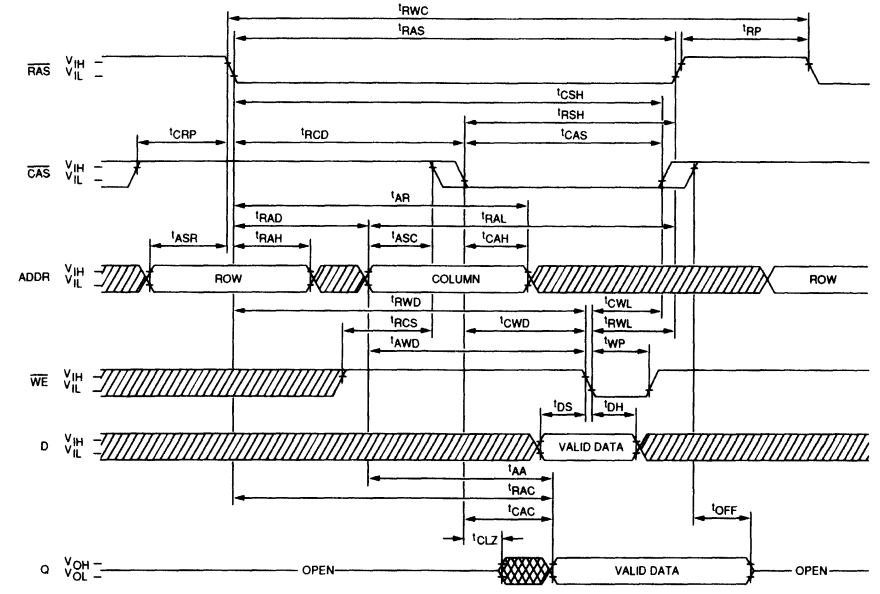
READ CYCLE



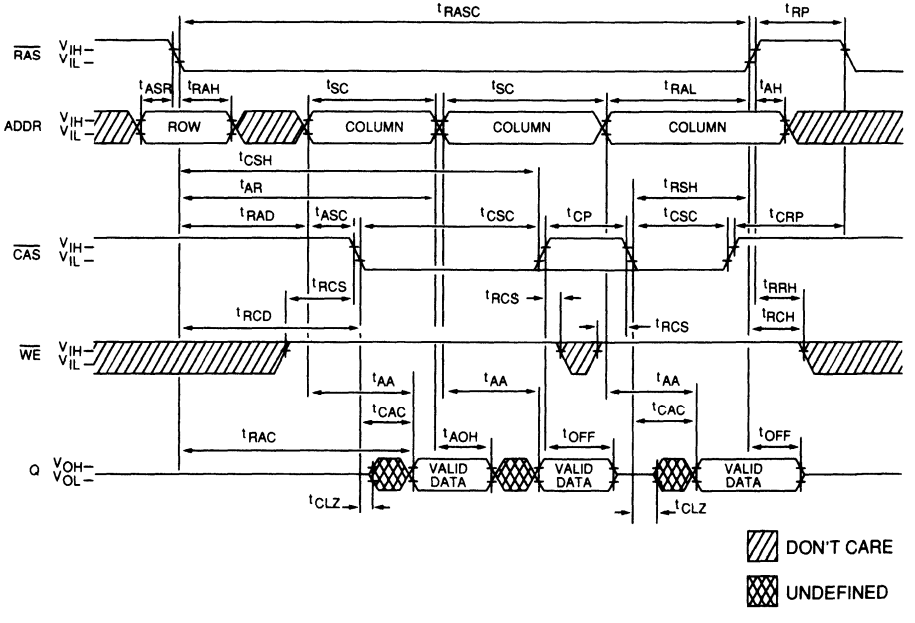
EARLY-WRITE CYCLE



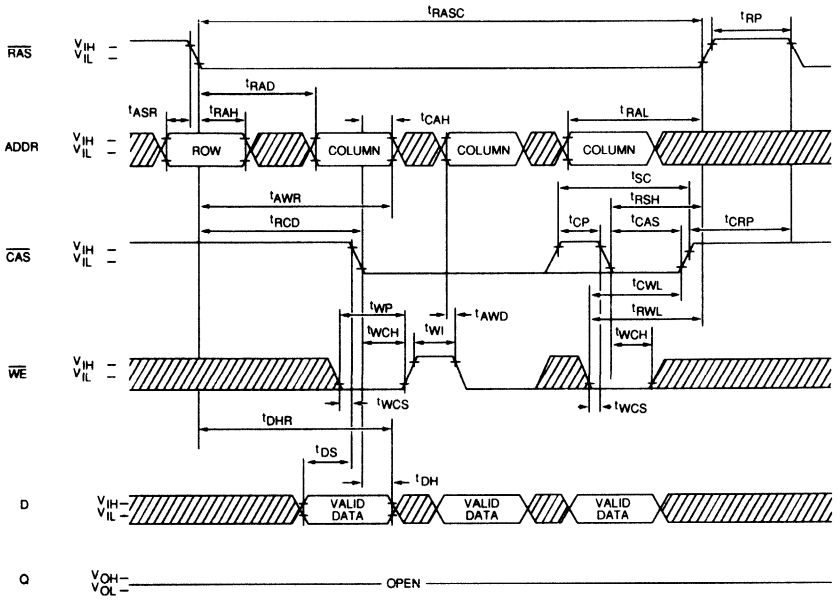
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



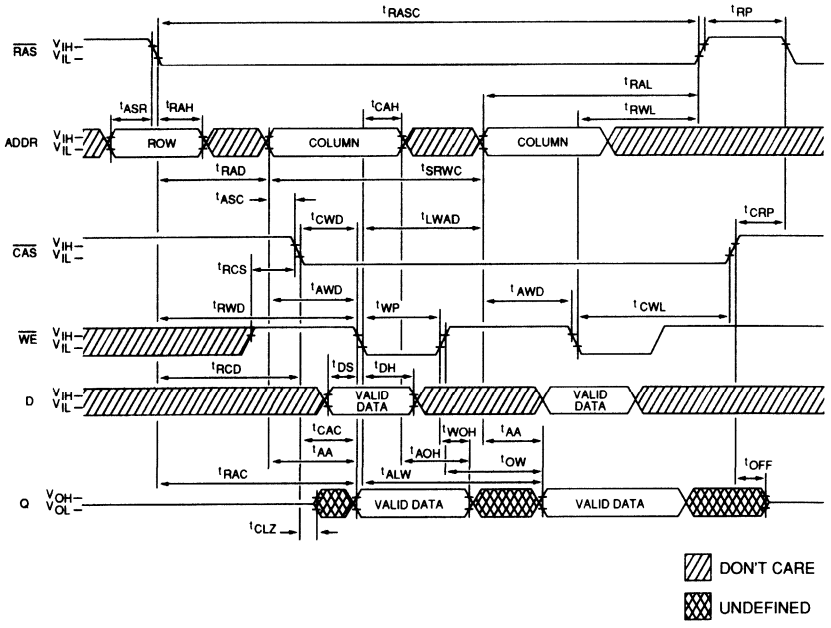
STATIC COLUMN READ CYCLE



STATIC COLUMN EARLY-WRITE CYCLE

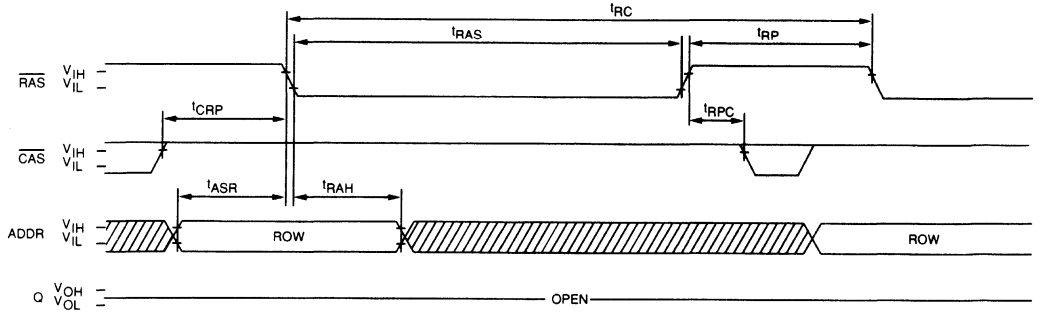


STATIC COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



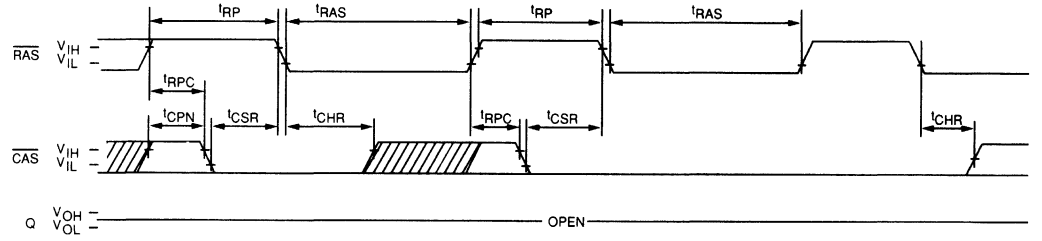
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



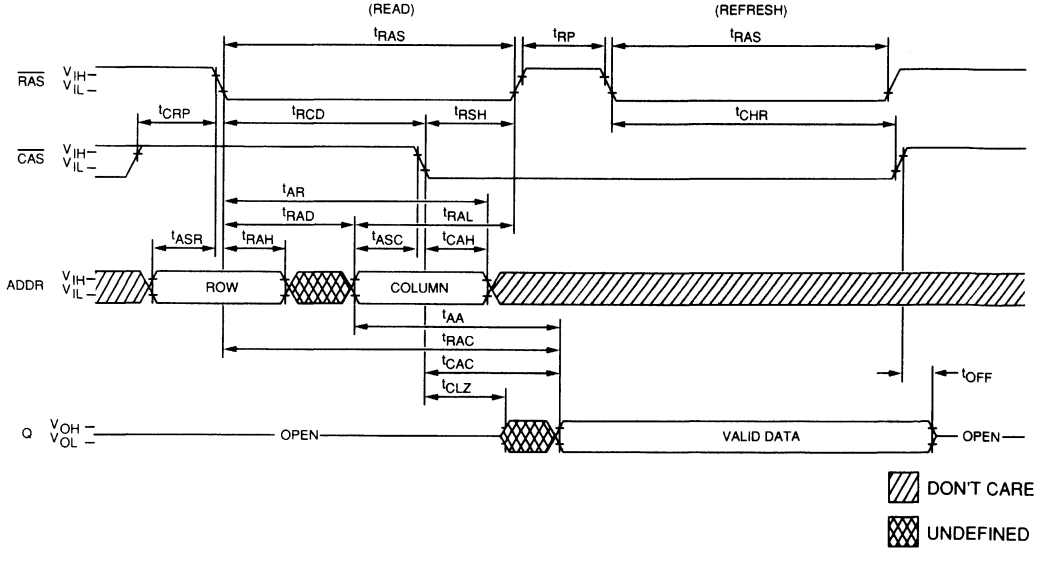
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[23]



DRAM MODULE

1MEG x 9 DRAM

FAST PAGE MODE

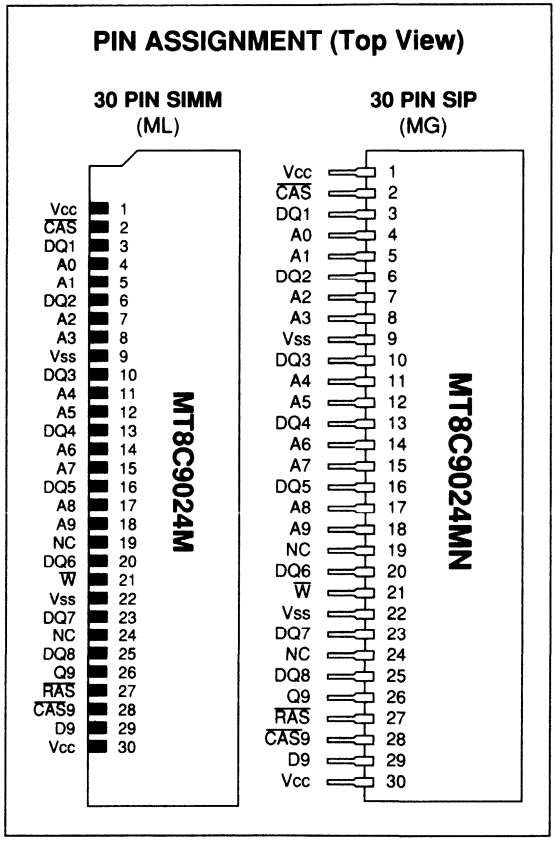
FEATURES

- Industry standard pin-out in a 30-pin single-in-line package
- High performance CMOS silicon gate process
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 45mW standby; 1575mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512 cycle refresh distributed across 8ms
- Optional Fast Page Mode

OPTIONS MARKING

• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Packages:	
Leadless 30-pin SIMM	M
Leadless 30-pim SIP	MN

PIN ASSIGNMENT (Top View)



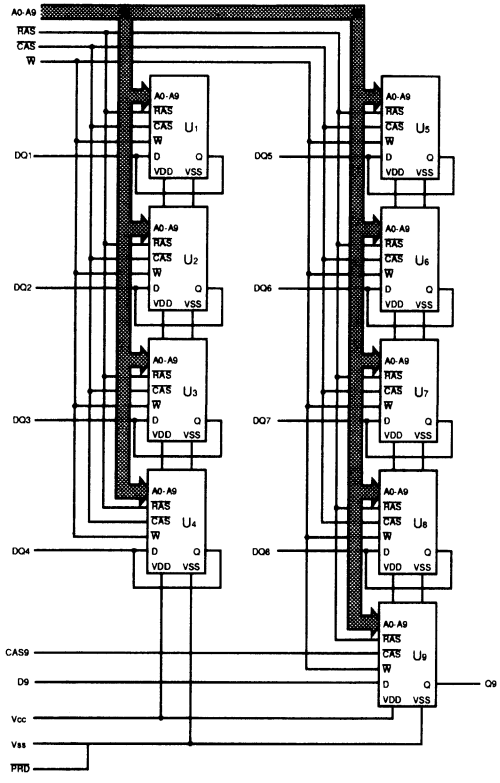
GENERAL DESCRIPTION

The MT8C9024 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x8 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM



U1 - U9 = MT4C1024DJ

TRUTH TABLE

Function	RAS	CAS	WE	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 9 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-90	90	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-90	90	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		450	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		450	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		18	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		9	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		315	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		315	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_9	C_{I1}		45	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		63	pF	2
Input Capacitance: D	C_{I3}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	160		190		220		ns	
READ-WRITE cycle time	^tRWC	185		220		255		ns	
FAST PAGE-MODE READ or WRITE cycle time	^tPC	45		55		70		ns	
FAST PAGE-MODE READ-WRITE cycle time	^tPRWC	70		85		105		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		30	ns	15
Access time from column address	^tAA		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		55		65	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		25		30		ns	
$\overline{RAS}$ precharge time	^tRP	70		80		90		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	15		15		20		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	25	75	25	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	12		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	17	40	20	50	20	60	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		85		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

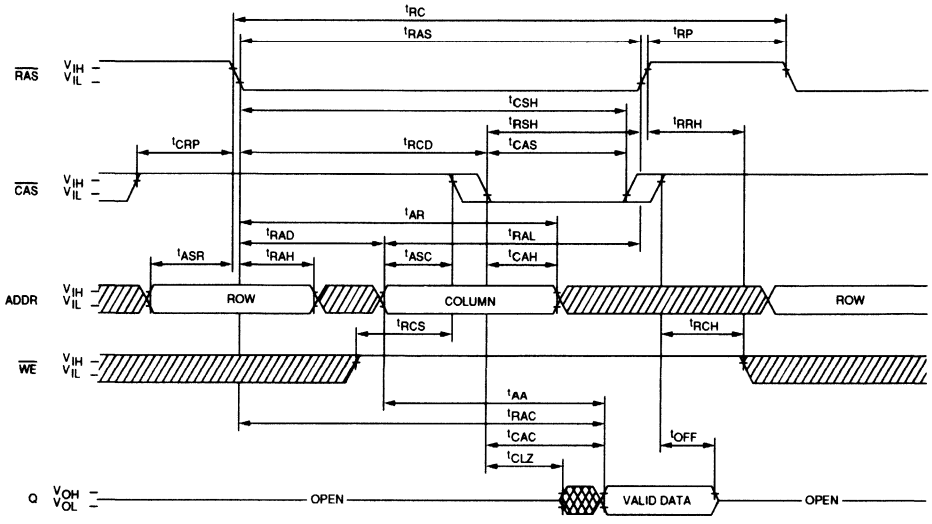
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	35	ns	20
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		85		ns	
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	20		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		100		120		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		25		30		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5

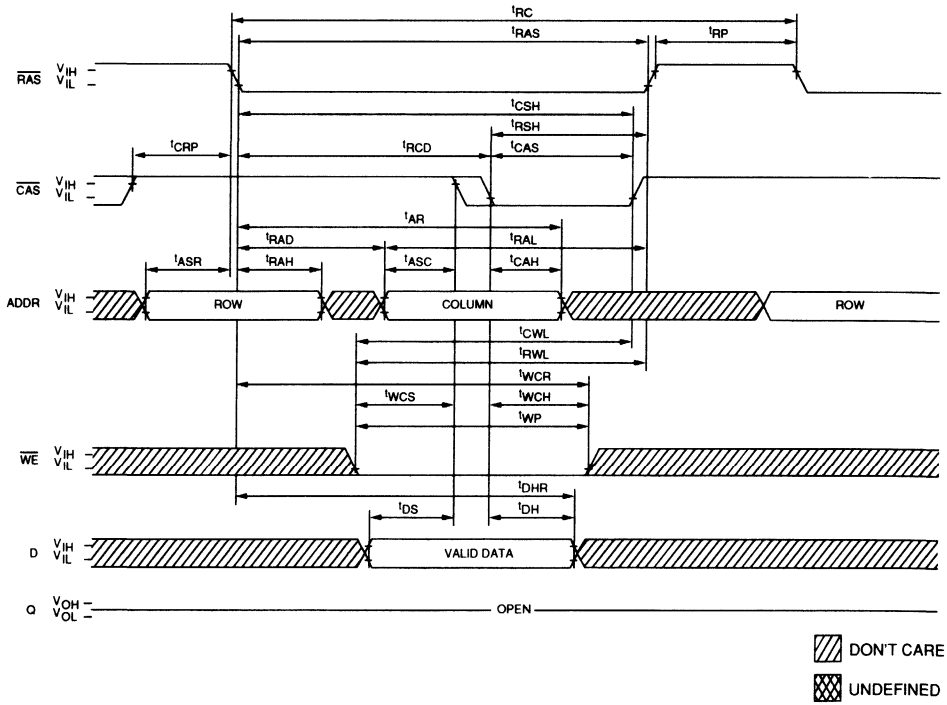
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5ns$.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \geq ^tRWD$ (min), $^tAWD \geq ^tAWD$ (min) and $^tCWD \geq ^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.
24. All other inputs equal Vcc -0.2V.

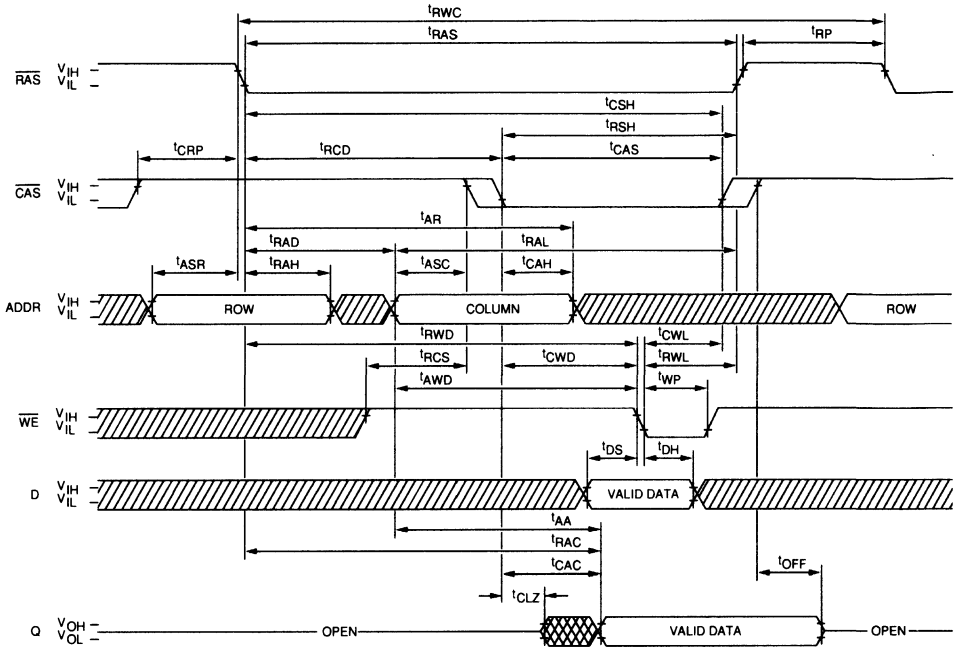
READ CYCLE



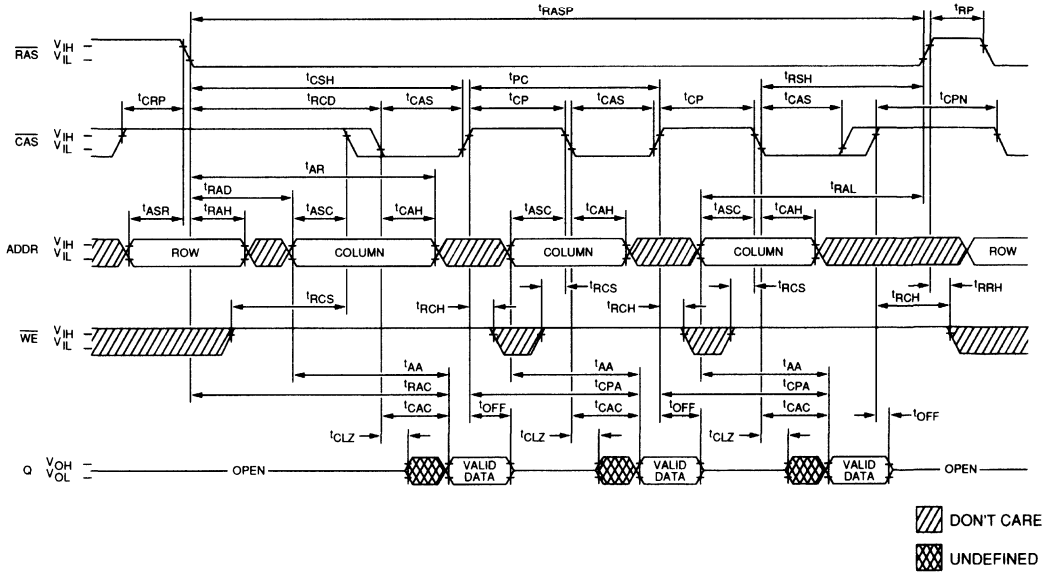
EARLY-WRITE CYCLE



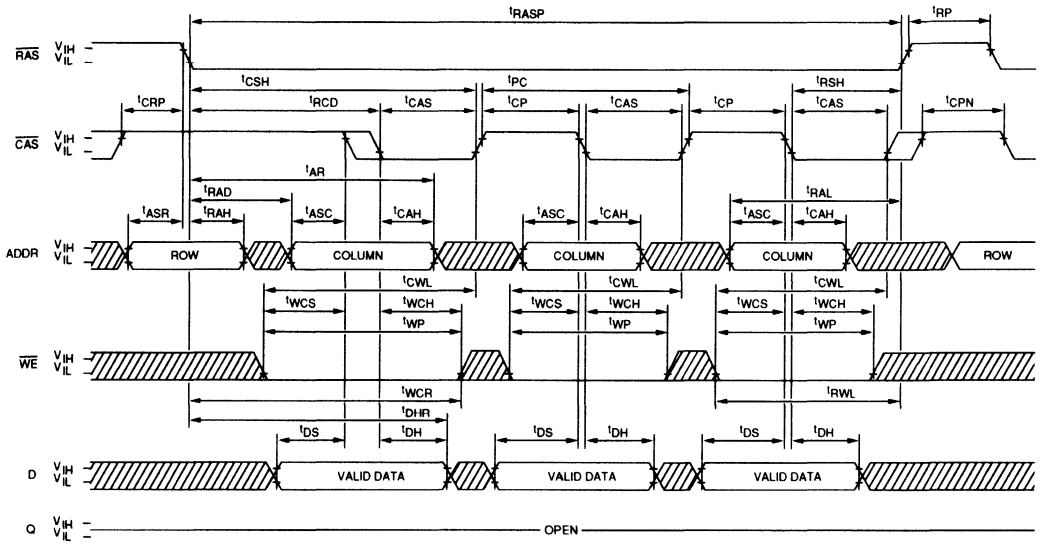
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



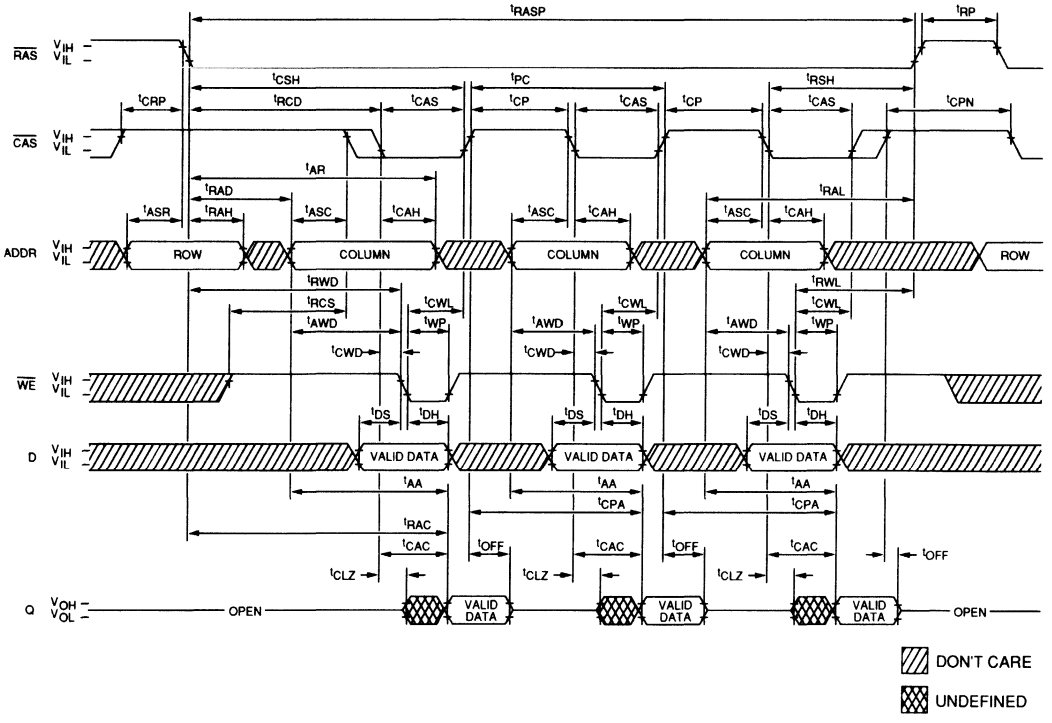
PAGE-MODE READ CYCLE



PAGE-MODE EARLY-WRITE CYCLE

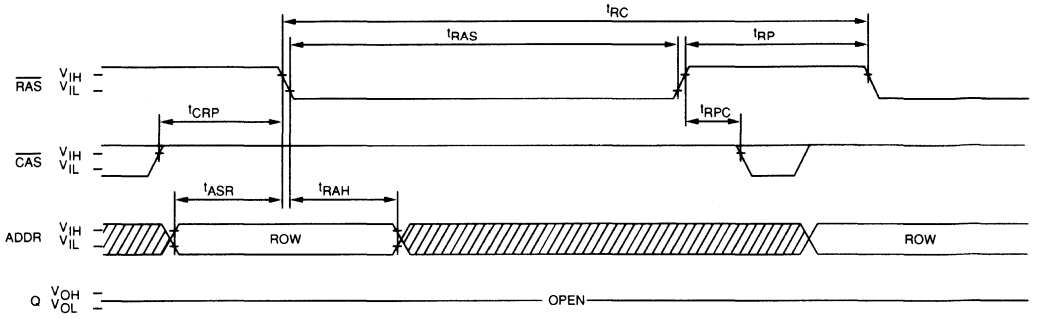


PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



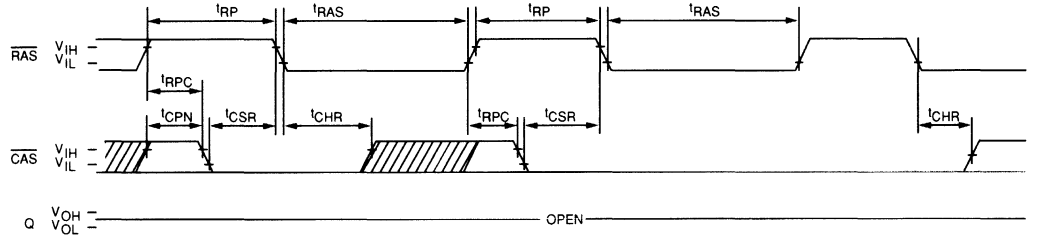
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



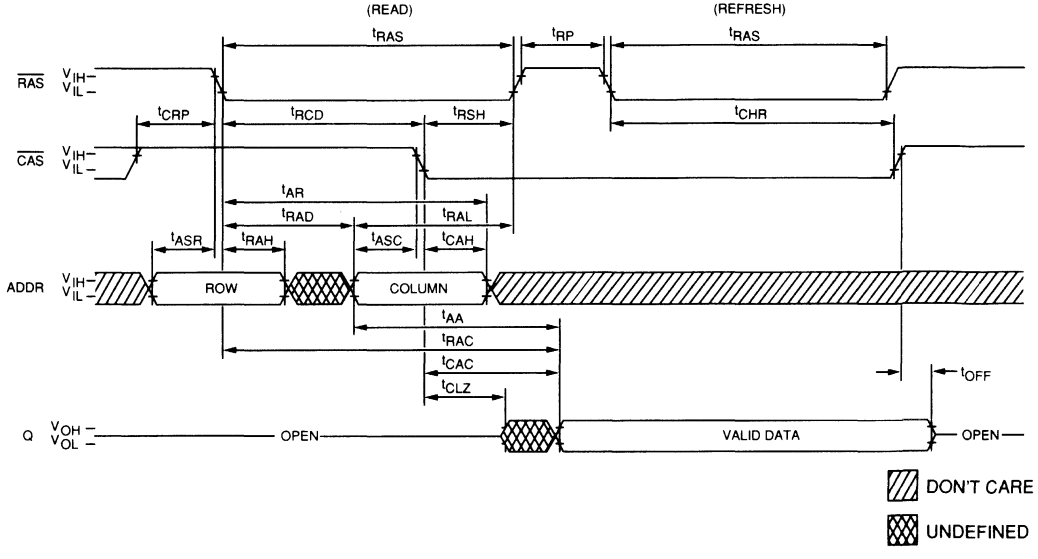
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[23]



DRAM MODULE

1MEG x 9 DRAM

LOW PROFILE

FEATURES

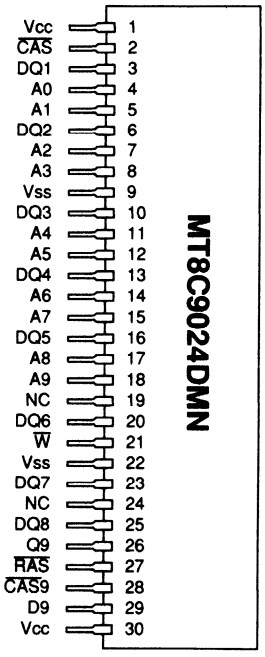
- Industry standard pin-out in a 30-pin single-in-line package
- High performance CMOS silicon gate process
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 45mW standby; 1575mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512 cycle refresh distributed across 8ms
- Optional Fast Page Mode

OPTIONS MARKING

- Timing
  - 80ns access - 8
  - 100ns access -10
  - 120ns access -12
- Packages:
  - Leadless 30-pim SIP (low profile) DN

PIN ASSIGNMENT (Top View)

30 PIN SIP
(MI)



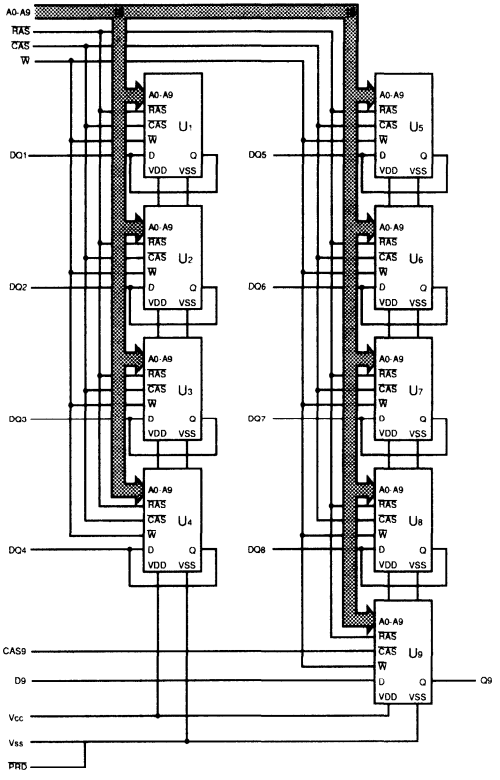
GENERAL DESCRIPTION

The MT8C9024 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x8 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the PAGE MODE operation.

FUNCTIONAL BLOCK DIAGRAM



U1 - U9 = MT4C1024DJ

TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 9 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-90	90	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-90	90	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		450	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		450	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		18	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		9	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		315	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		315	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		45	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		63	pF	2
Input Capacitance: D	C_{I3}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	160		190		220		ns	
READ-WRITE cycle time	t_{RWC}	185		220		255		ns	
FAST PAGE-MODE READ or WRITE cycle time	t_{PC}	45		55		70		ns	
FAST PAGE-MODE READ-WRITE cycle time	t_{PRWC}	70		85		105		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		25		30	ns	15
Access time from column address	t_{AA}		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		55		65	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	t_{RASP}	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{CAS}$ precharge time	t_{CPN}	15		15		20		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	t_{CP}	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	60	25	75	25	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		15		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	20	60	ns	18
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	60		70		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		50		60		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

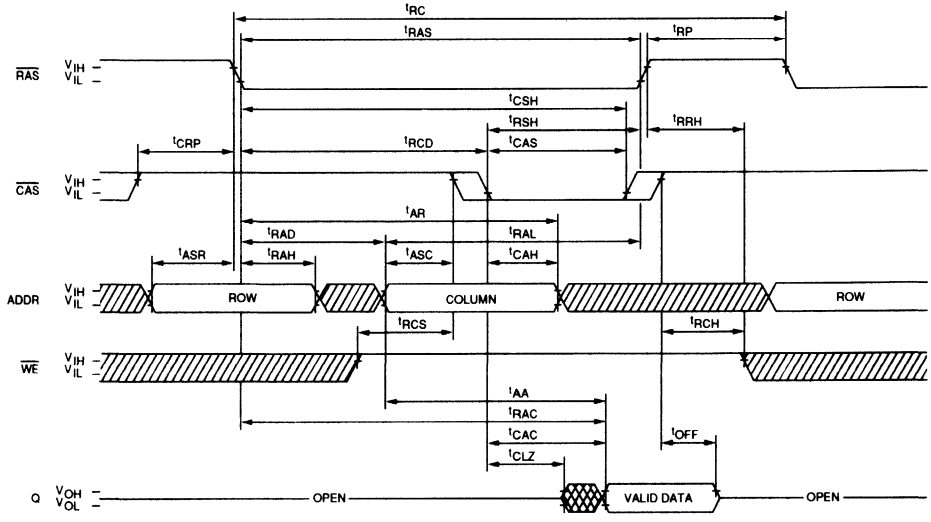
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \leq T_A \leq +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	35	ns	20
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		85		ns	
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	20		20		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		90		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		100		120		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		25		30		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5

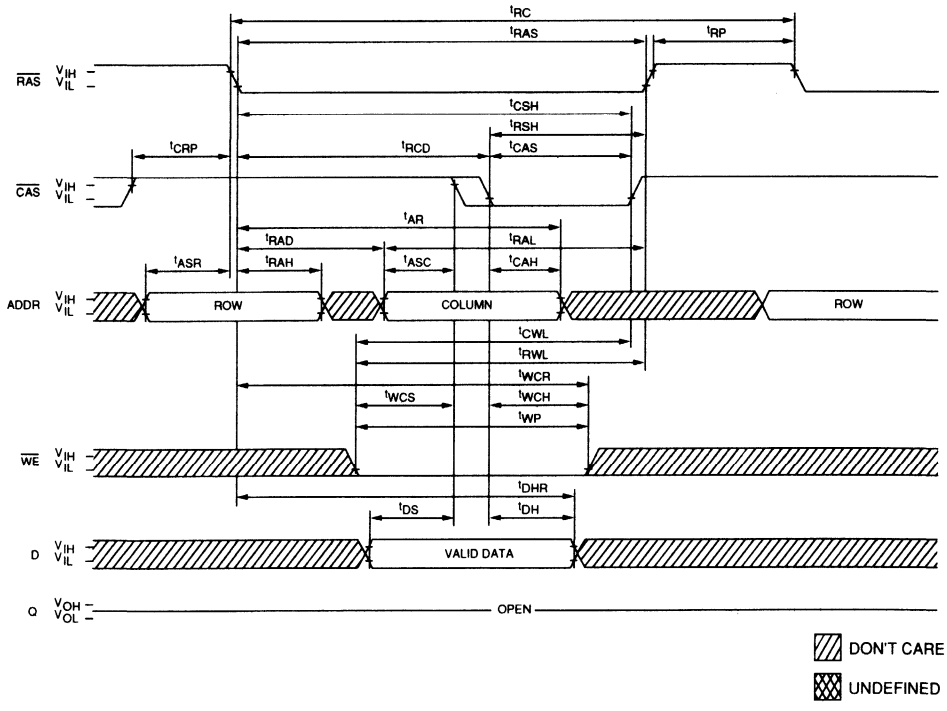
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit through out the entire cycle. If $^tRWD \ge {}^tRWD$ (min), $^tAWD \ge {}^tAWD$ (min) and $^tCWD \ge {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.
24. All other inputs equal Vcc -0.2V.

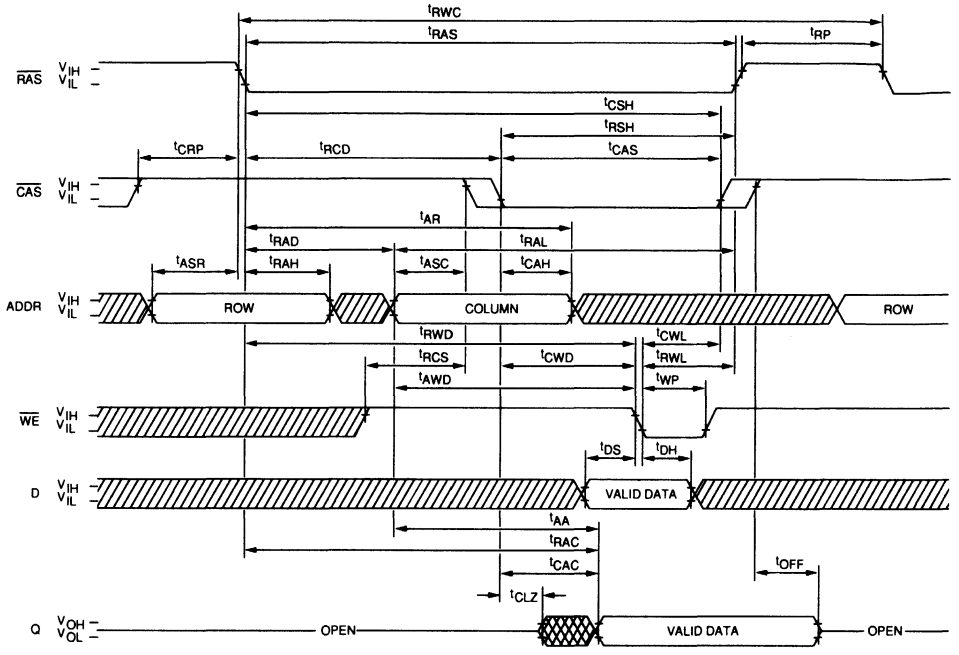
READ CYCLE



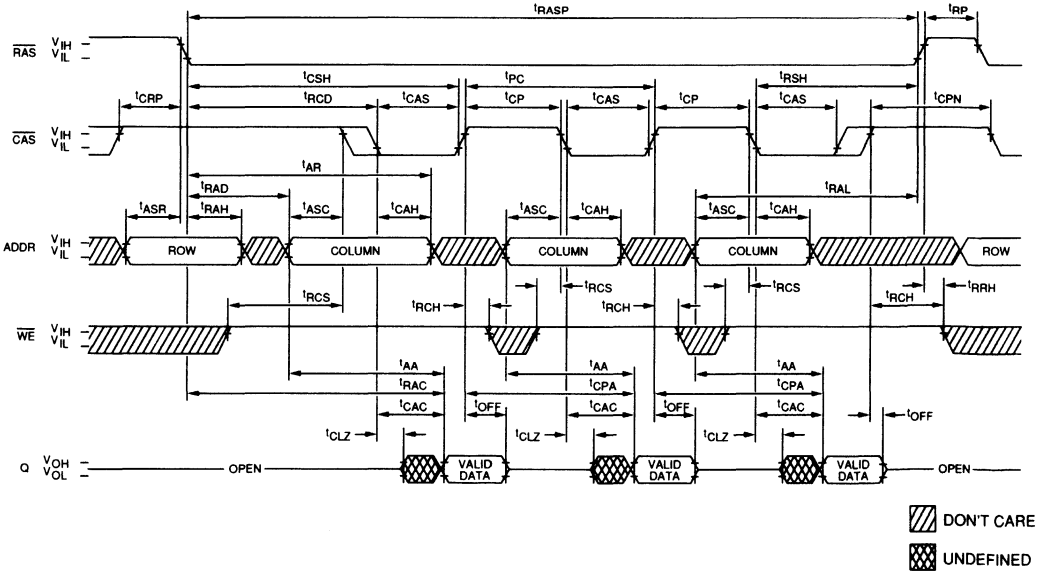
EARLY-WRITE CYCLE



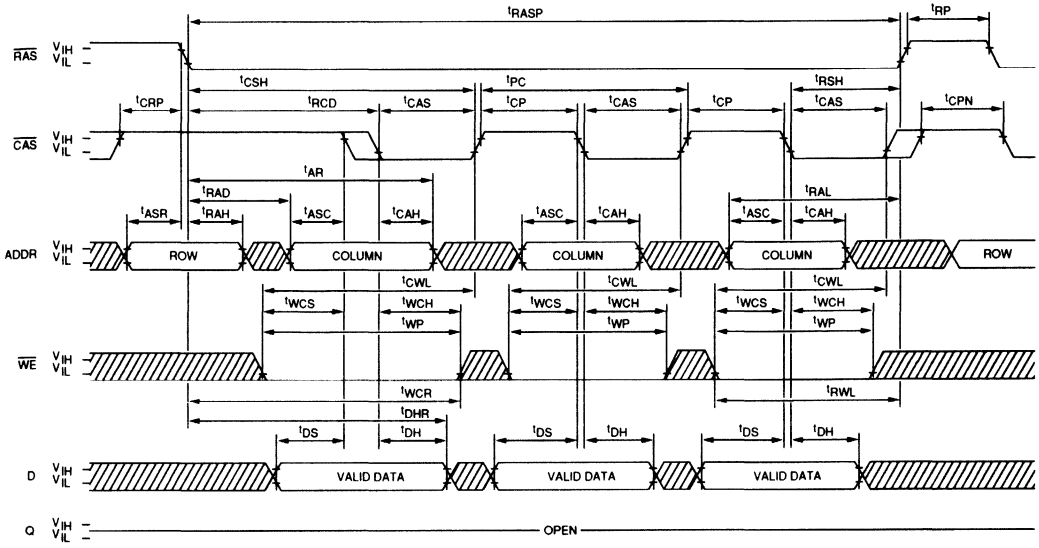
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



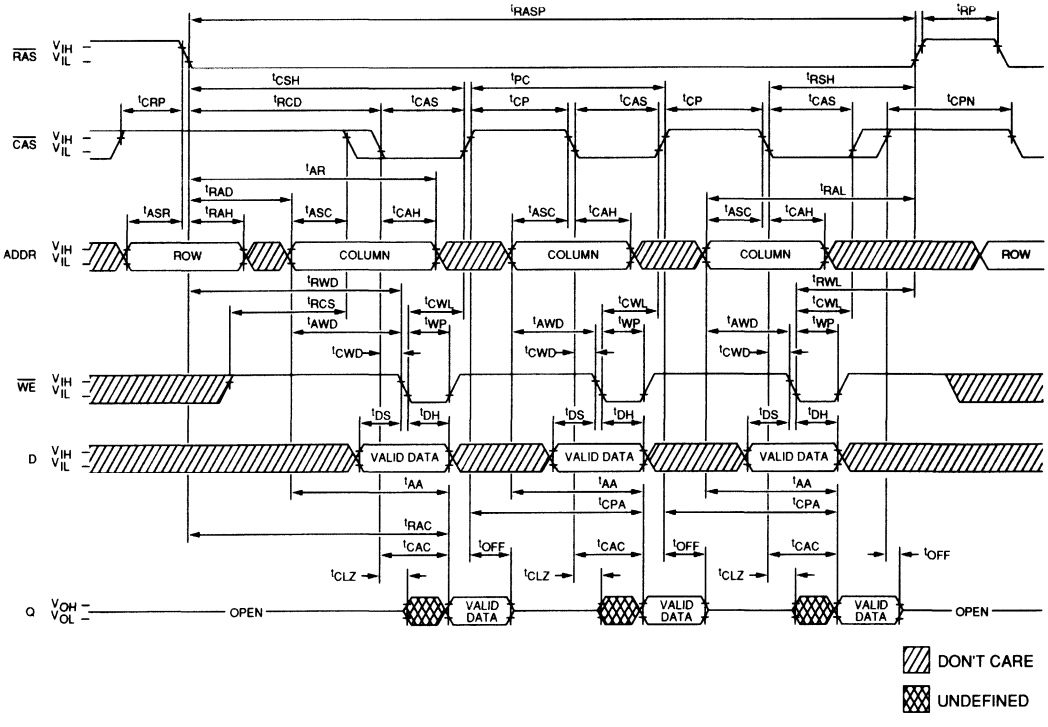
PAGE-MODE READ CYCLE



PAGE-MODE EARLY-WRITE CYCLE

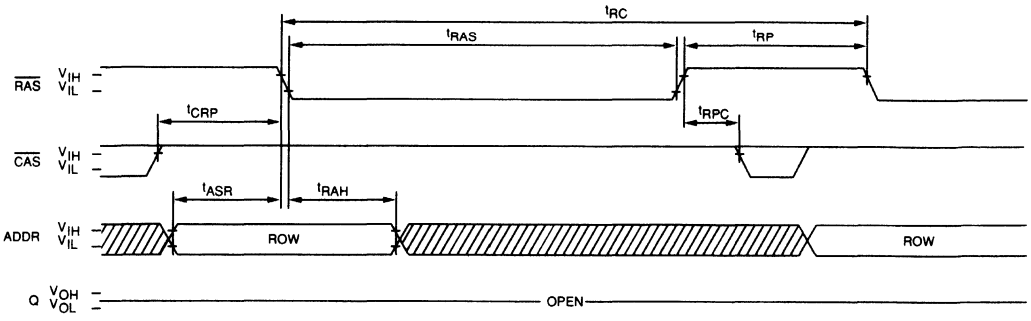


PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



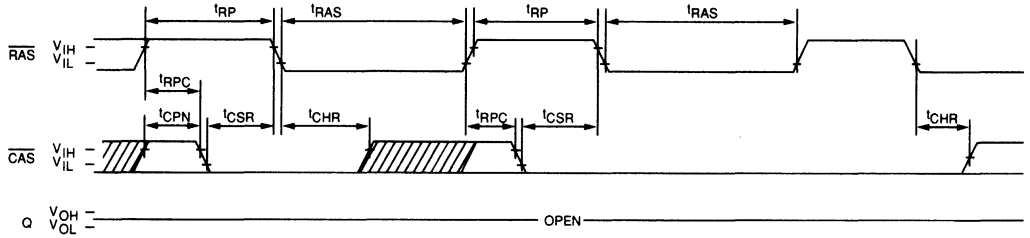
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



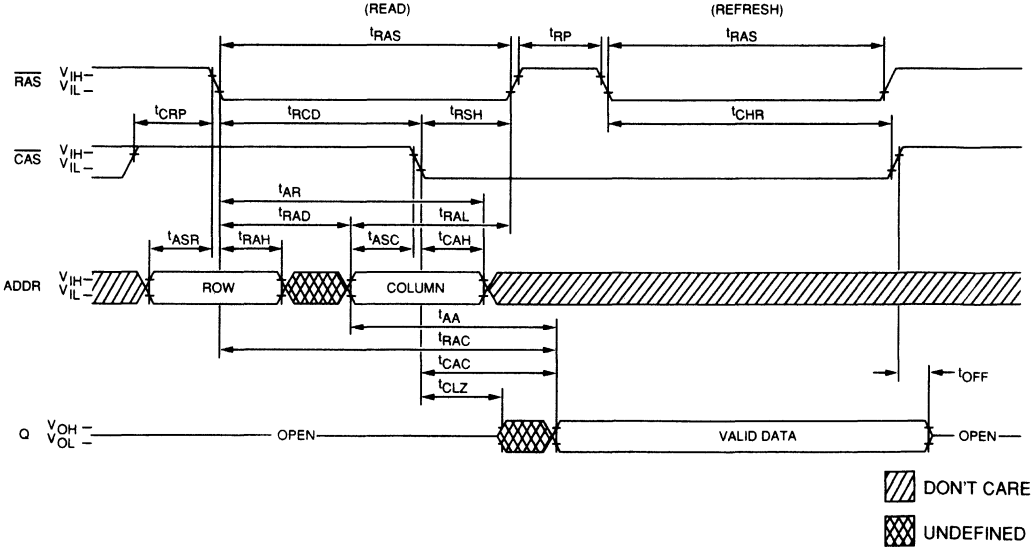
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[23]



DRAM MODULE

1MEG x 9 DRAM

NIBBLE MODE

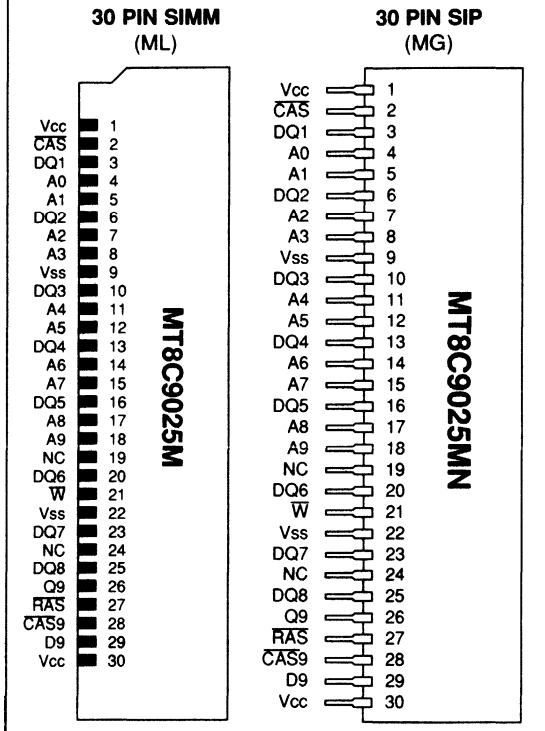
FEATURES

- Industry standard pin-out in a 30-pin single-in-line package
- High performance CMOS silicon gate process
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 45mW standby; 1575mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512 cycle refresh distributed across 8ms
- Optional Nibble access mode

OPTIONS MARKING

- Timing
  - 80ns access - 8
  - 100ns access -10
  - 120ns access -12
- Packages:
  - Leaded 30-pin SIP MN
  - Leadless 30-pin SIMM N

PIN ASSIGNMENT (Top View)

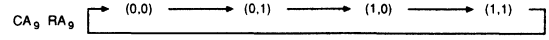


GENERAL DESCRIPTION

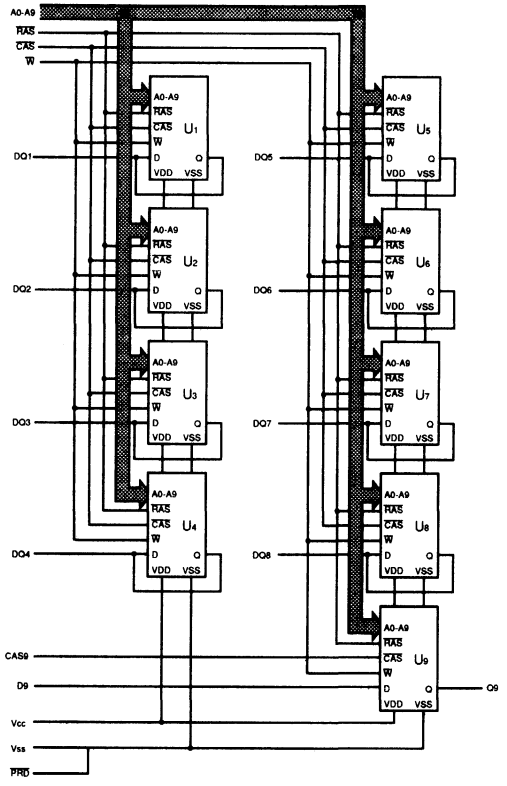
The MT8C9025 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x9 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

NIBBLE MODE operation allows faster sequential serial data operations (READ, WRITE or READ-MODIFY-WRITE) on up to 4 bits. The first of 4 bits is accessed in the usual manner with $\overline{CAS}$ address A9 (nibble MSB) and $\overline{RAS}$ address A9 (nibble LSB) selecting on of 4 bits within a nibble for initial access. By holding $\overline{RAS}$ LOW, $\overline{CAS}$ can be toggled incrementing the nibble address field in modulo 4 fashion with wrap around (see below).



FUNCTIONAL BLOCK DIAGRAM



U1 - U9 = MT4C1025DJ

TRUTH TABLE

Function	RAS	CAS	WE	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
NIBBLE MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
NIBBLE MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
RAS ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High Impedance	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 9 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-90	90	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-90	90	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		450	mA	3, 4
OPERATING CURRENT: NIBBLE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		450	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		18	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		9	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		315	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		315	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_9	C_{I1}		45	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		63	pF	2
Input Capacitance: D	C_{I3}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	150		180		220		ns	
READ-MODIFY-WRITE cycle time	t_{RWC}	175		210		255		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		25		30	ns	15
Access time from column address	t_{AA}		40		50		60	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		55		65	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{RAS}$ precharge time	t_{RP}	60		80		90		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		20		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	60	10	75	15	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		10		15		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		20		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	40	20	50	15	60	ns	18
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	t_{AR}	60		75		110		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		50		60		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	25	ns	20
$\overline{WE}$ command set-up time	t_{WCS}	0		0		0		ns	21
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	t_{WCR}	60		75		80		ns	
Write command pulse width	t_{WP}	15		20		25		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

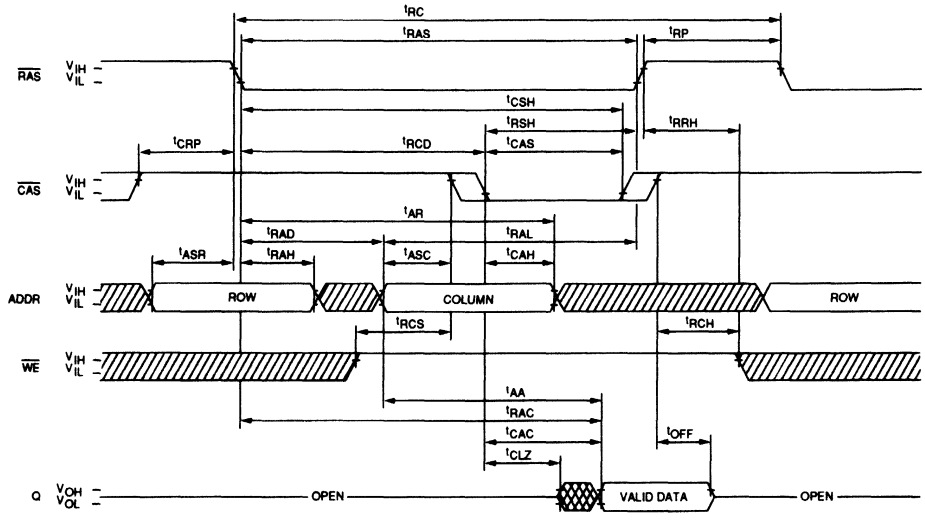
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0°C \le T_A \le +70°C$, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		110		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		100		120		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		25		35		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5
$\overline{RAS}$ pulse width (NIBBLE MODE)	^tRASN	80	100,000	100	100,000	120	100,000	ns	
$\overline{CAS}$ precharge time (NIBBLE MODE)	^tNCP	10		10		15		ns	
NIBBLE MODE cycle time	^tNC	40		45		55		ns	
NIBBLE MODE READ-MODIFY-WRITE cycle time	^tNRWC	65		75		85		ns	
NIBBLE MODE access time	^tNCAC		20		20		35	ns	15
NIBBLE MODE pulse width	^tNCAS	20		25		35		ns	
NIBBLE MODE $\overline{CAS}$ precharge time	^tNCP	10		10		10		ns	
NIBBLE MODE $\overline{RAS}$ hold time	^tNRSH	20		25		30		ns	
NIBBLE MODE $\overline{CAS}$ to $\overline{WE}$ delay time	^tNCWD	20		25		35		ns	
NIBBLE MODE $\overline{WE}$ command to $\overline{RAS}$ lead time	^tNRWL	20		25		30		ns	
NIBBLE MODE $\overline{WE}$ command to $\overline{CAS}$ lead time	^tNCWL	20		25		30		ns	

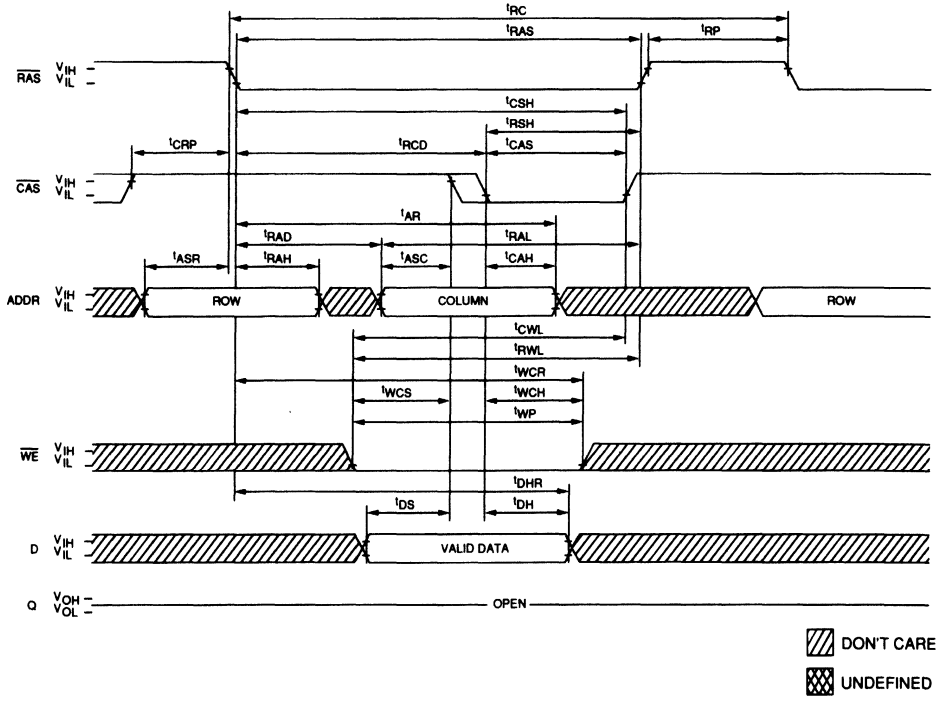
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (min), $^tAWD \geq {}^tAWD$ (min) and $^tCWD \geq {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

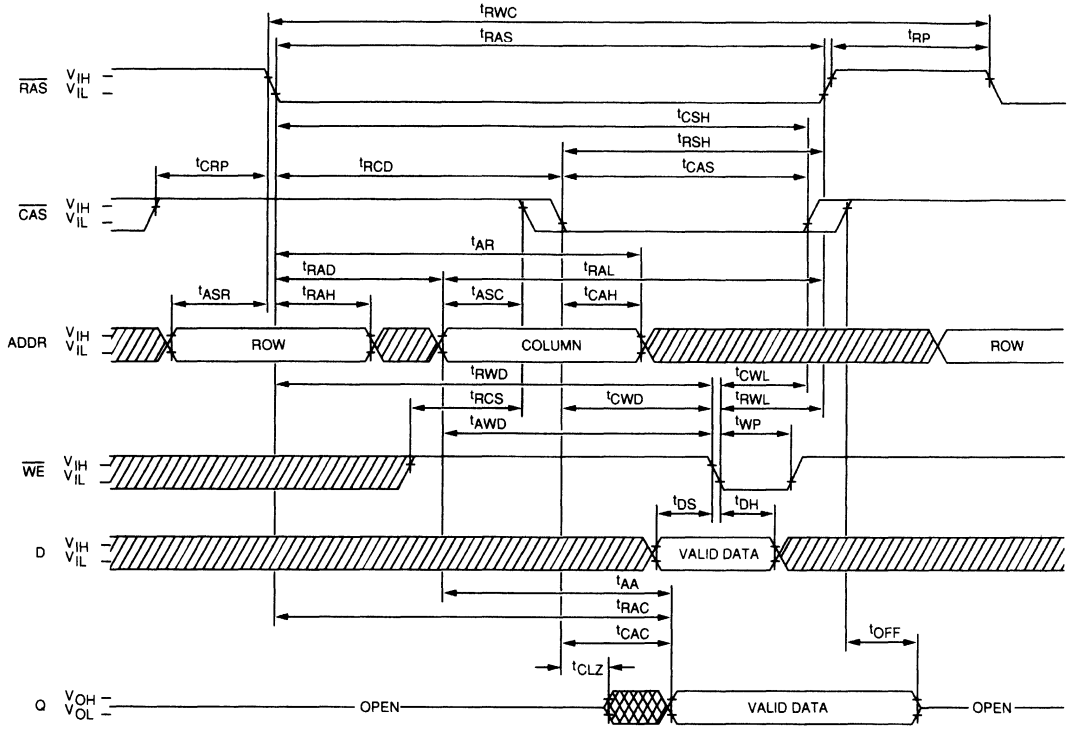
READ CYCLE



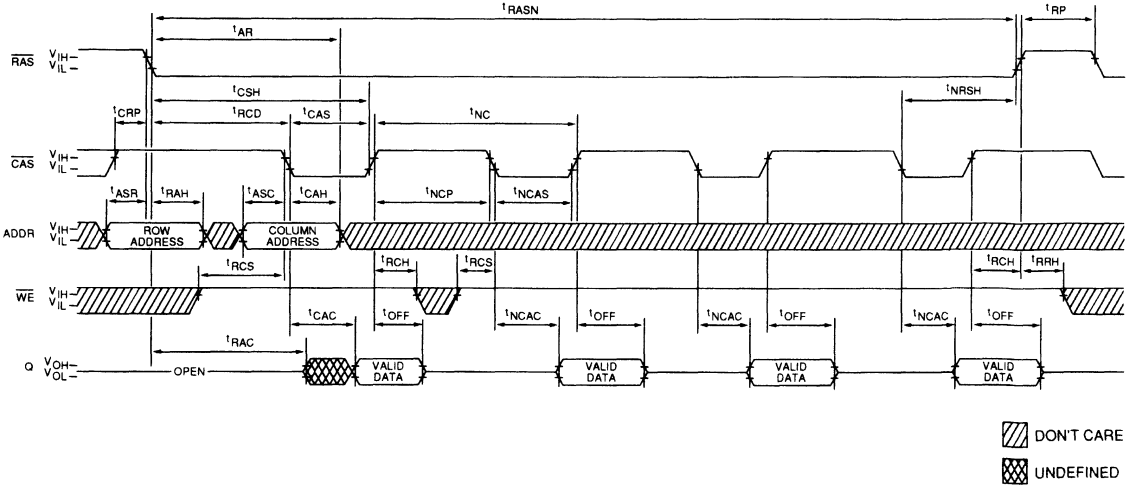
EARLY-WRITE CYCLE



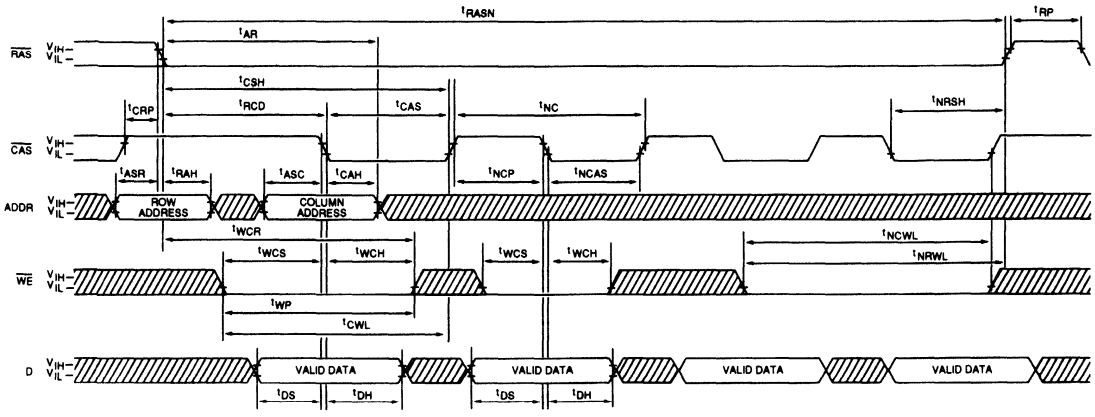
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



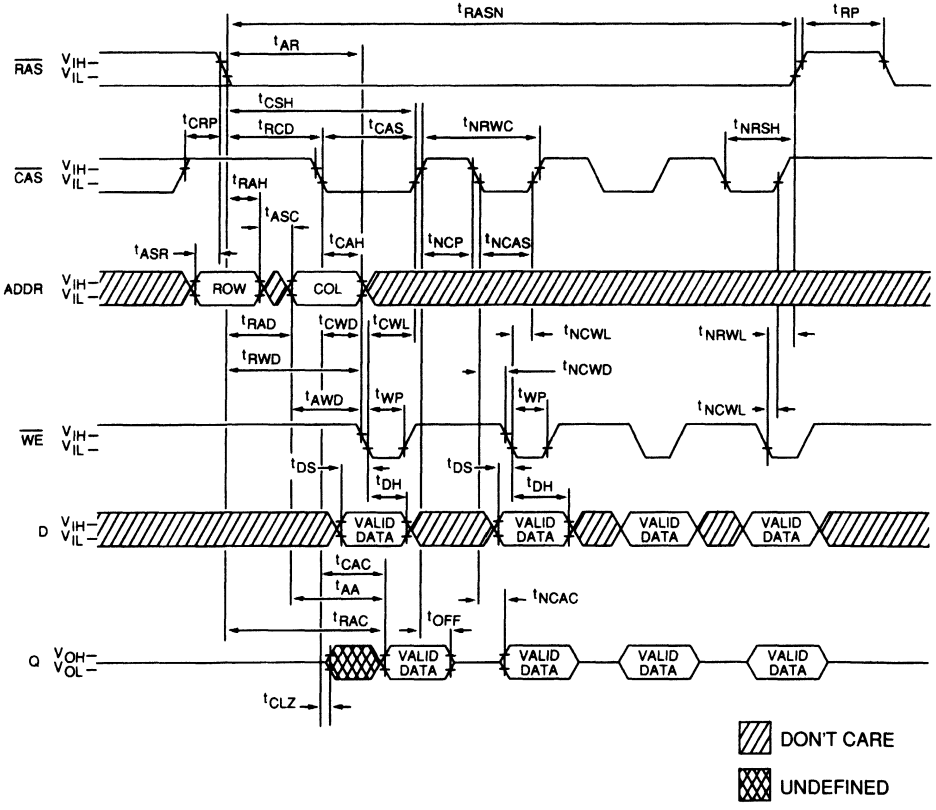
NIBBLE MODE READ CYCLE



NIBBLE MODE EARLY-WRITE CYCLE

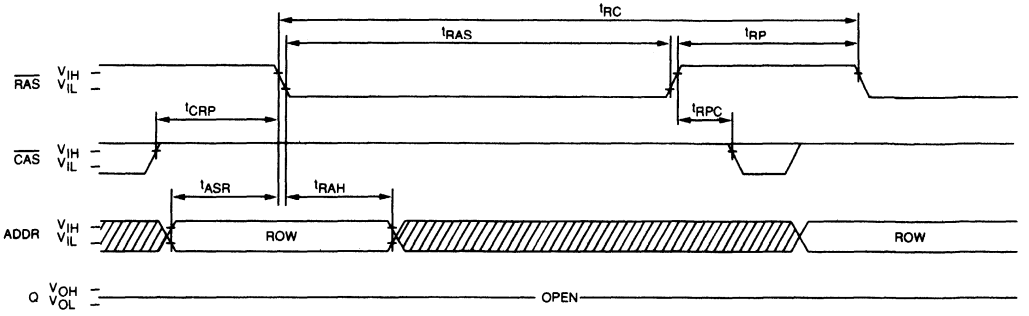


NIBBLE MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



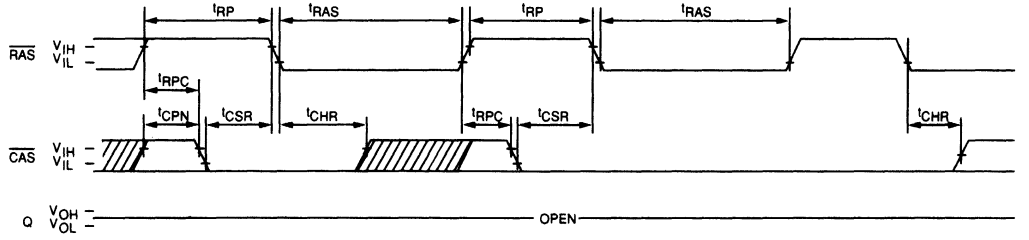
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_8; A_9 and $\overline{WE}$ = DON'T CARE.)



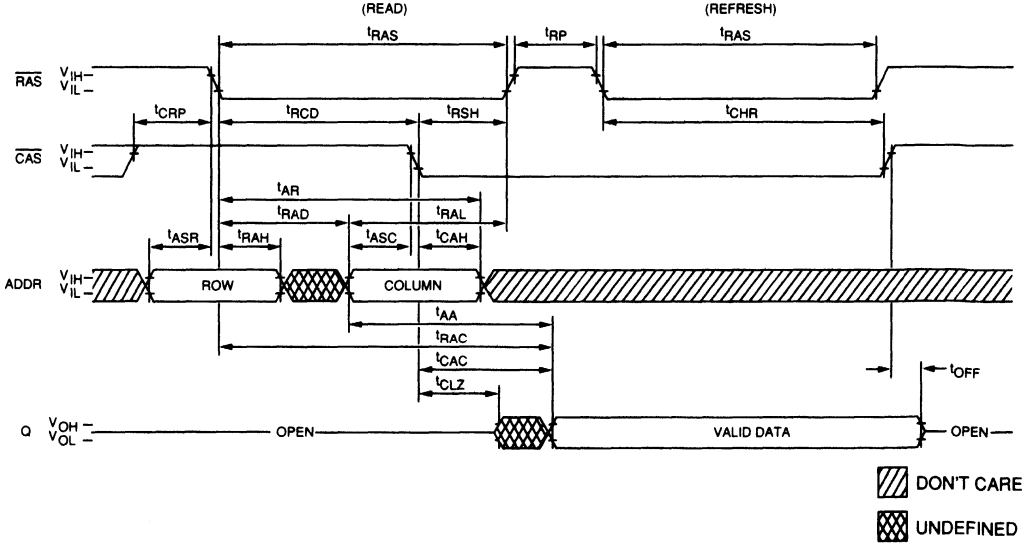
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

(A_0 - A_9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[23]



DRAM MODULE

1MEG x 9 DRAM

STATIC COLUMN

FEATURES

- Industry standard pin-out in a 30-pin single-in-line package
- High performance CMOS silicon gate process
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 45mW standby; 1575mW active, typical.
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$ -BEFORE-$\overline{RAS}$, and HIDDEN
- 512 cycle refresh distributed across 8ms
- Optional Static Column access mode

OPTIONS MARKING

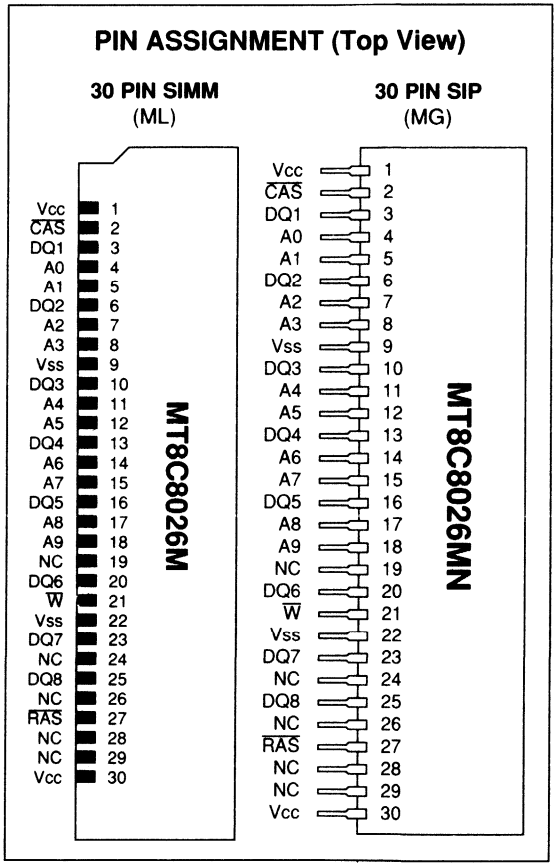
- Timing

80ns access	- 8
100ns access	-10
120ns access	-12

- Packages:

Leaded 30-pin SIP	MN
Leadless 30-pin SIMM	M

PIN ASSIGNMENT (Top View)



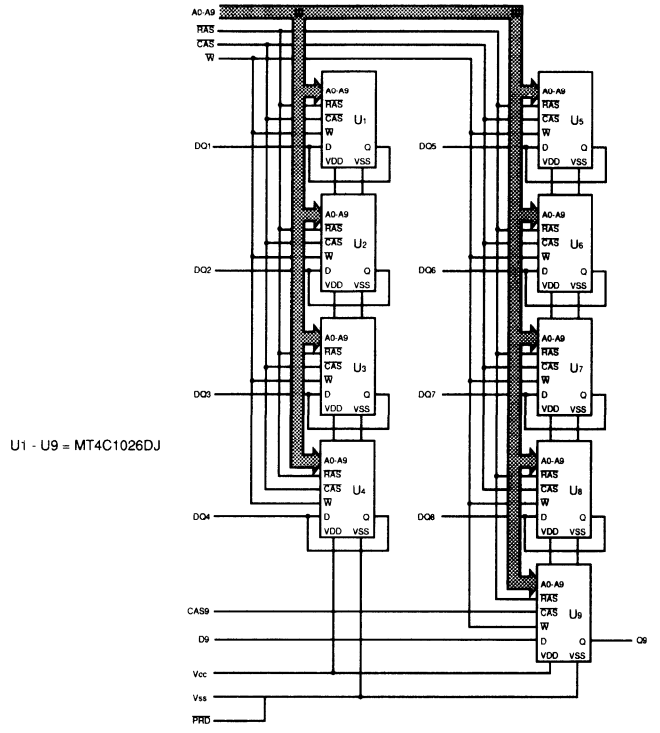
GENERAL DESCRIPTION

The MT8C9026 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x9 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle data in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed in by $\overline{RAS}$ followed by a column address strobed in by $\overline{CAS}$. By holding $\overline{RAS}$ LOW, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

FUNCTIONAL BLOCK DIAGRAM



U1 - U9 = MT4C1026DJ

TRUTH TABLE

Function	RAS	CAS	WE	TF	Addresses tR	Addresses tC		NOTES
Standby	H	H	H	GND/NC	X	X	High Impedance	
READ	L	L	H	GND/NC	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	GND/NC	ROW	COL	Data In	
STATIC COLUMN READ	L	H→L→H	H	GND/NC	ROW	COL COL	Valid Data Out, Valid Data Out	
STATIC COLUMN WRITE	L	H→L→H	L	GND/NC	ROW	COL COL	Valid Data In, Valid Data Out	
RAS ONLY REFRESH	L	H	H	GND/NC	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	GND/NC	ROW	COL	Valid Data Out	
CAS-BEFORE-RAS REFRESH	H→L	L	H	GND/NC	X	X	High Impedance	
TEST FUNCTION	L	L	H	H	ROW	COL	Data Out, Test Function Mode	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 9 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts)	I_I	-90	90	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-90	90	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		450	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		450	mA	3, 4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		18	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V)	I_{CC4}		9	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		315	mA	3
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		315	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		45	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		63	pF	2
Input Capacitance: D	C_{I3}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		12	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, V_{CC} = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	150		180		220	ns		
READ-MODIFY-WRITE cycle time	^tRWC	175		210		255		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		30	ns	15
Access time from column address	^tAA		40		50		60	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		25		30		ns	
$\overline{RAS}$ precharge time	^tRP	60		70		90		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		ns	
$\overline{CAS}$ precharge time	^tCPN	10		15		20		ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	25	75	15	90	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	40	20	50	20	60	ns	18
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		20		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	90		115		115		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		ns	
Read command set-up time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	25	ns	20
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		80		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

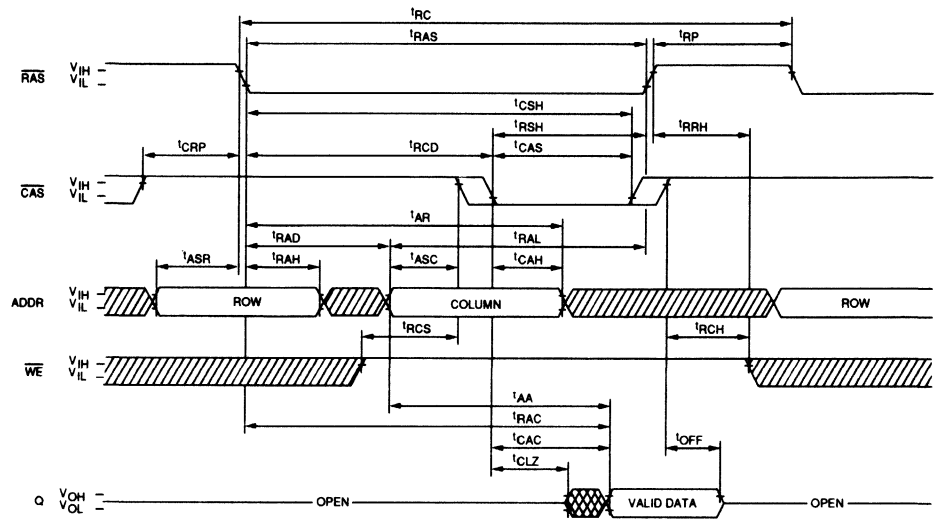
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command pulse width	^tWP	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		30		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		25		30		ns	
$\overline{WE}$ inactive time	^tWI	10		10		10		ns	
Data-in set-up time	^tDS	0		0		0		ns	22
Data-in hold time	^tDH	15		20		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		80		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		100		110		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	40		50		60		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	20		25		30		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		ns	5
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	80	100,000	100	100,000	120	100,000	ns	
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		10		15		ns	
STATIC COLUMN MODE cycle time	^tSC	45		55		65		ns	
STATIC COLUMN READ-MODIFY-WRITE cycle time	^tSRMW	80		100		160		ns	
Last Write to column address delay time	^tLWAD	20	35	25	45	30	55	ns	
Last Write to column address hold time	^tAHLW	75		95		115		ns	
Output data hold time from column address	^tAOH	5		5		5		ns	
Output data enable from Write	^tOW		20		25		25	ns	

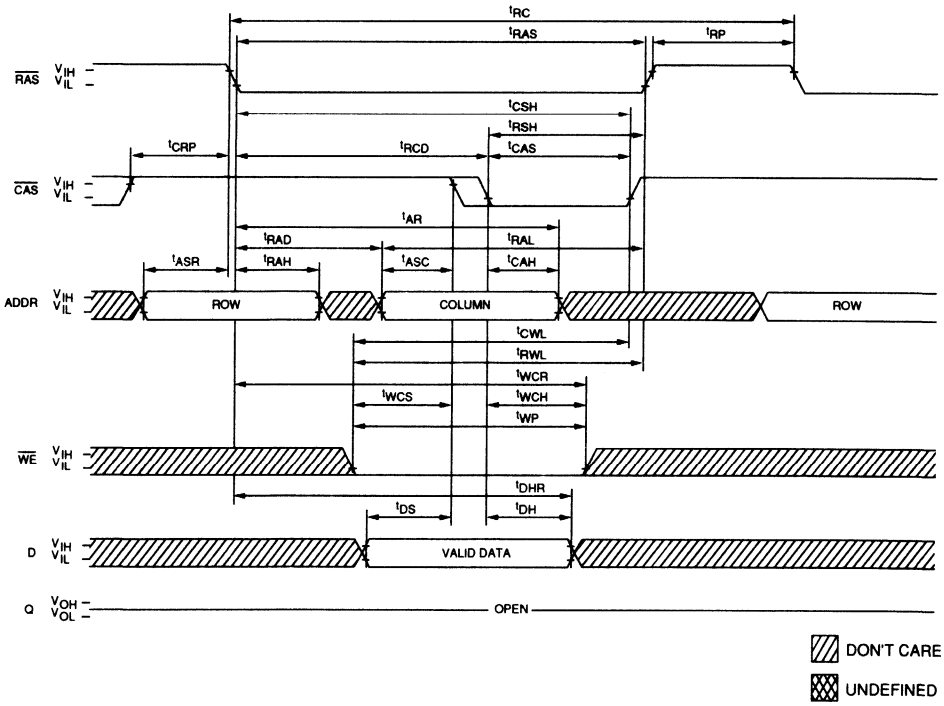
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (min), $^tAWD \geq {}^tAWD$ (min) and $^tCWD \geq {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.

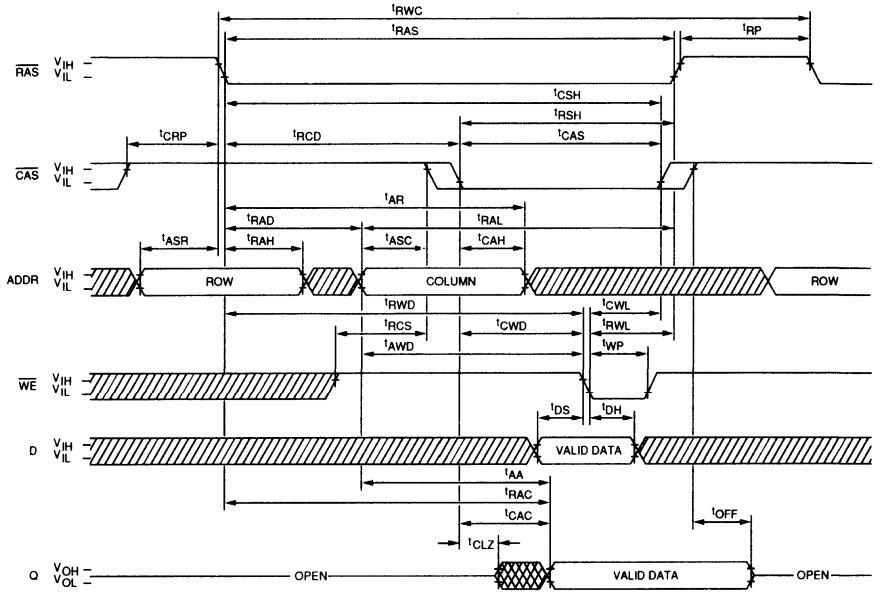
READ CYCLE



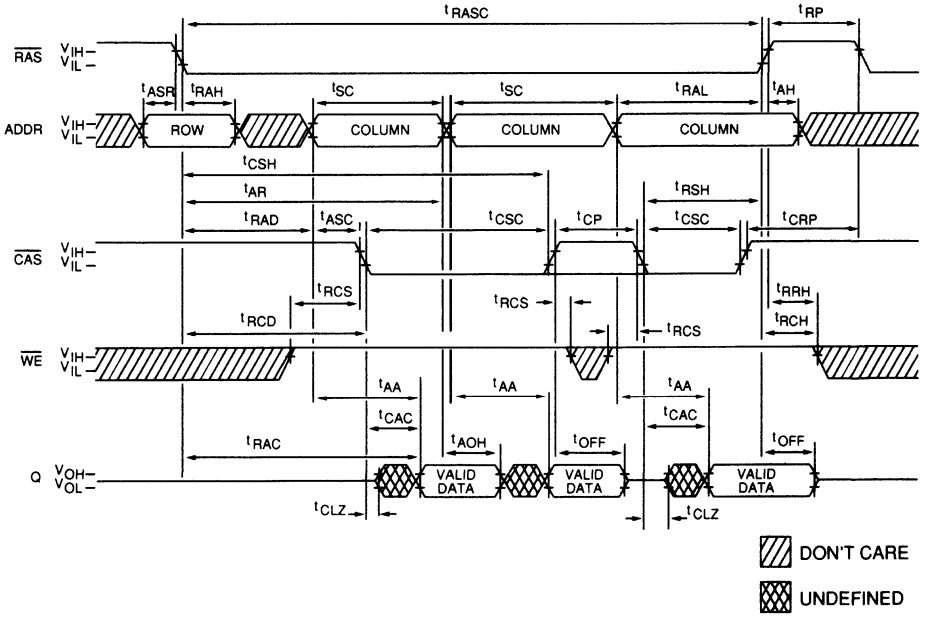
EARLY-WRITE CYCLE



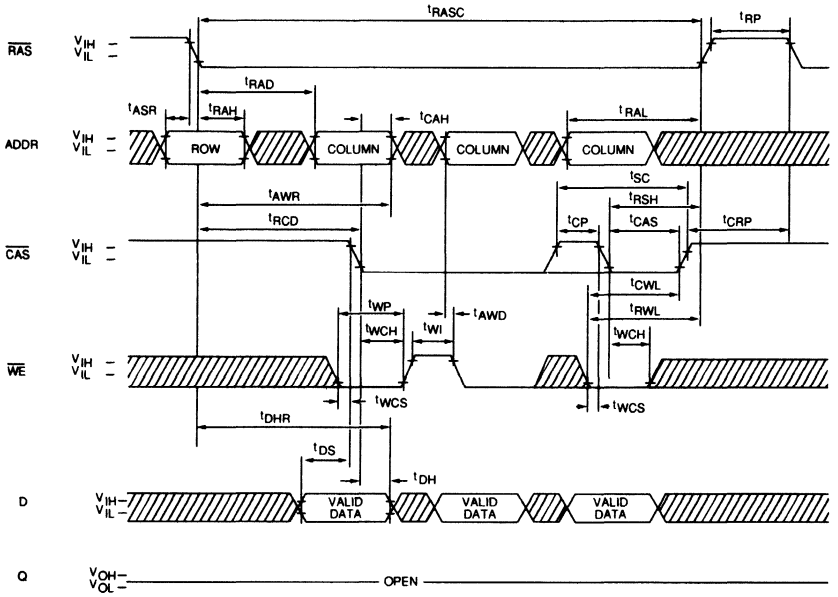
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



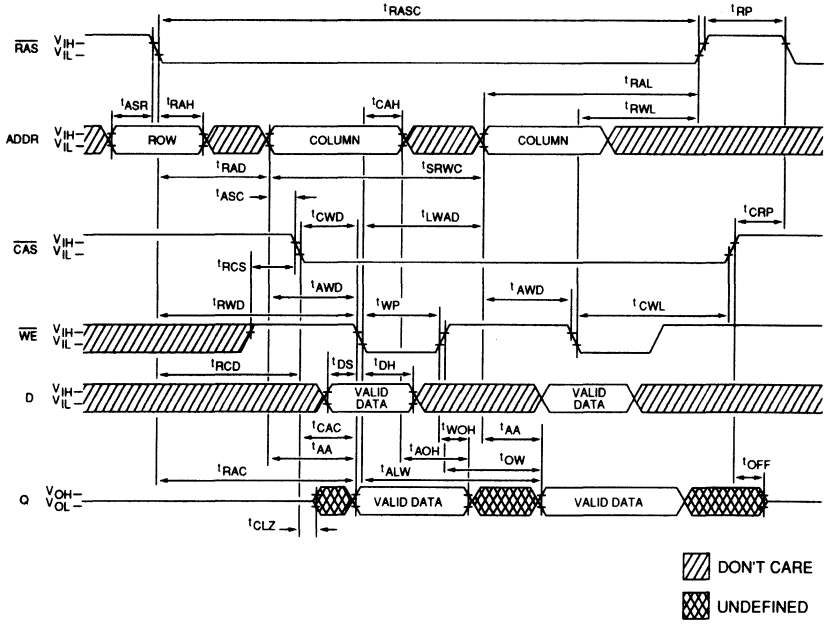
STATIC COLUMN READ CYCLE



STATIC COLUMN EARLY-WRITE CYCLE

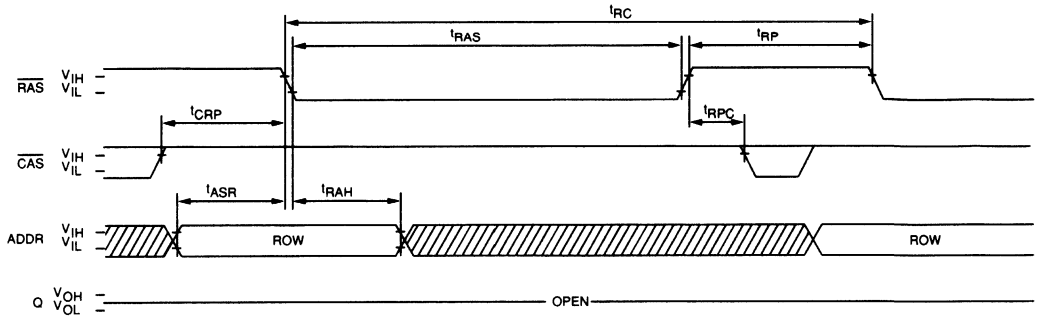


STATIC COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



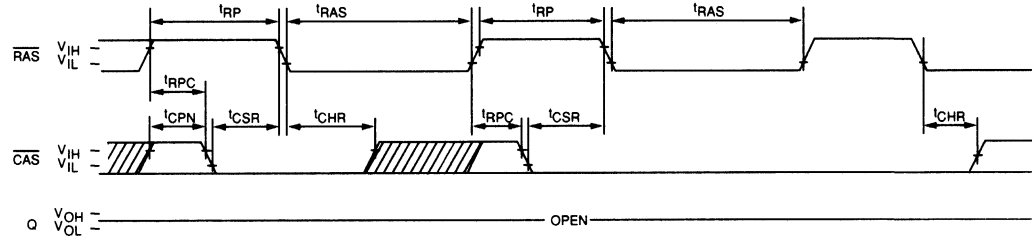
$\overline{RAS}$ ONLY REFRESH CYCLE

($ADDR = A_0 - A_8$; A_9 and $\overline{WE}$ = DON'T CARE.)



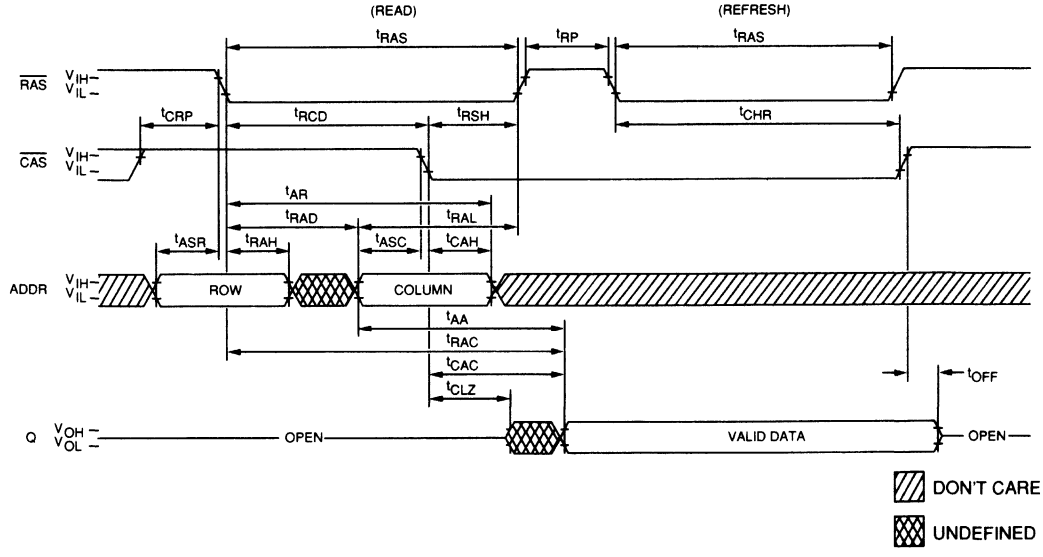
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

($A_0 - A_9$ and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE

($\overline{WE}$ = HIGH)[23]



DYNAMIC RAMs 1

DYNAMIC RAM MODULES 2

MULTIPORT DYNAMIC RAMs 3

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MULTIPORT PRODUCT SELECTION GUIDE

VRAM

Memory Configuration	Access Cycle	Part Number	Access Time (ns)	Power Dissipation		Package & Number of Pins				Process	Page
				Standby	Active	PDIP	ZIP	SOJ	CDIP		
64K x 4	Page Mode	MT42C4064	100,120,150	10mw	150mw	24	24	24	24	CMOS	3-3
128K x 8	Fast Page	MT42C8128	80,100,120,150	5mw	200mw	40	-	40	-	CMOS	3-27
256K x 4	Fast Page	MT42C4256	80,100,120,150	5mw	200mw	28	28	28	28	CMOS	3-65

VRAM

64K x 4 DRAM with 256 x 4 SAM

FEATURES

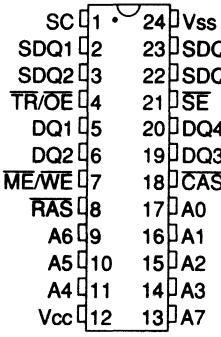
- Industry standard pin-out, timing and functions
- High performance CMOS silicon gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256 cycle refresh within 4ms
- Optional PAGE MODE access cycles
- Dual port organization: 64K x 4 DRAM port
  256 x 4 SAM port
- Bit MASKED WRITE mode capability on DRAM port
- No refresh required for Serial Access Memory
- Low power: 10mW standby; 150mW active, typical
- Fast access times – 100ns parallel, 33ns serial

OPTIONS

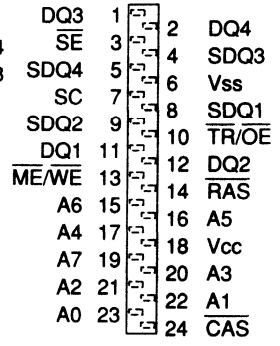
	MARKING
• Timing (DRAM, SAM)	
100ns, 33ns	-10
120ns, 40ns	-12
150ns, 60ns	-15
• Packages	
Plastic DIP (400 mil)	None
Ceramic DIP (400 mil)	C
Plastic ZIP	Z
Plastic SOJ (300 mil)	DJ

PIN ASSIGNMENT (Top View)

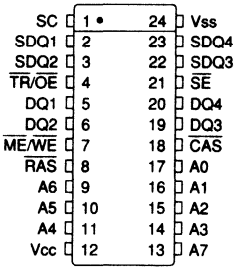
24 Pin DIP (PH, CG)



24 Pin ZIP (ZC)



24 Pin SOJ (DJB)



GENERAL DESCRIPTION

The MT42C4064 is a high speed, dual port CMOS dynamic random access memory (DPDRAM) containing 262,144 bits. They can be accessed either by a four bit wide DRAM port or by a 256 x 4 bit serial access memory (SAM) port. Data can be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the DPDRAM is functionally identical to the MT4067 (64K x 4) bit DRAM. Four 256 bit data registers make up the serial access memory portion of the DPDRAM. Data I/O and internal data transfer is accomplished using three separate bidirectional data paths; the four bit random access I/O port, the four internal 256 bit wide paths between the DRAM and the SAM, and the four bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the DPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the DPDRAM is fully static and does not require any refresh.

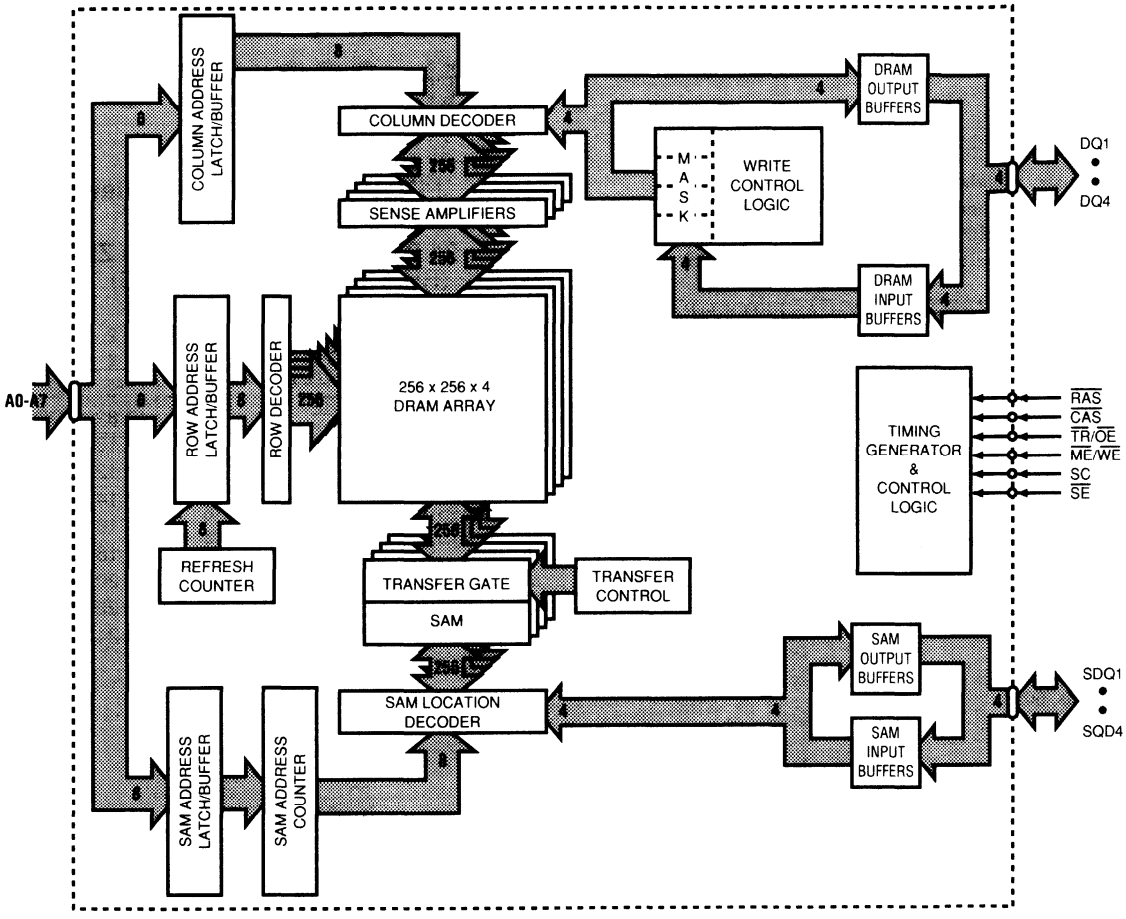


Figure 1
MT42C4064 BLOCK DIAGRAM

PIN DESCRIPTIONS

DIP/SOJ PIN NUMBER(S)	ZIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
1	7	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
4	8, 9, 4, 5	$\overline{TR}/\overline{OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a high impedance state.
7	13	$\overline{ME}/\overline{WE}$	Input	Mask Enable: If $\overline{ME}/\overline{WE}$ is LOW at the falling edge of $\overline{RAS}$ a MASKED WRITE cycle is performed, or Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = H) or WRITE ($\overline{WE}$ = L) cycle when accessing the DRAM. This includes a DRAM-TO-SAM TRANSFER ($\overline{WE}$ = H) or SAM- TO-DRAM TRANSFER ($\overline{WE}$ = L).
8	14	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 8 rowaddress bits and as a strobe for the MASK ENABLE and TRANSFER functions.
9, 10, 11, 13, 14, 15, 16, 17	23, 22, 21, 20 17, 16, 15, 19	A0 to A7	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select 4 bits out of the 256K available. During TRANSFER operations, A0 to A7 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and the SAM start address (when $\overline{CAS}$ goes LOW).
18	24	$\overline{CAS}$	Input	Column Address Strobe: $\overline{RAS}$ is used to clock in the 8 column address bits and enable the DRAM output buffers ($\overline{TR}/\overline{OE}$ must also be LOW).
21	3	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a high impedance state. $\overline{SE}$ is also used during a TRANSFER operation to indicate whether a SAM-TO-DRAM TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
5, 6, 19, 20	11,12,1,2	DQ1 - DQ4	Input/ Output	DRAM Data I/O: Inputs, Outputs, or high impedance, and/or Mask Data Inputs: For MASKED WRITE cycle only.
2, 3, 22, 23	8.9.4.5	SDQ1 - SDQ4	Input/ Output	Serial Data I/O: Input, Output, or high impedance.
12	18	Vcc	Supply	Power Supply: +5 Volts ±10%
24	6	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The DPDRAM can be divided into three functional blocks (see Figure 1); the DRAM, the transfer control circuitry, and the serial access memory (SAM). All of the operations described below are also shown in the AC Timing Diagrams section of this data sheet as well as summarized in the Truth Table.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing transfer operations the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$.*

DRAM OPERATION

The DRAM portion of the DPDRAM is functionally identical to standard 64K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or "don't care" states for the DRAM are specified for the DPDRAM. These conditions are highlighted in the following discussion.

READ/WRITE Cycles

The 16 address bits that are used to select four memory bits from the 65,536 x 4 available are latched into the chip using the A0 -A7, $\overline{RAS}$, and $\overline{CAS}$ inputs. First, the 8 row address bits are set up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH to LOW. Next, the 8 column address bits are set up on the address inputs and clocked in when $\overline{CAS}$ goes from HIGH to LOW.

For single port DRAMs the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. For the DPDRAM, $(\overline{TR})/\overline{OE}$ is used, when $\overline{RAS}$ goes LOW, to select between an internal transfer operation and a DRAM operation. $(\overline{TR})/\overline{OE}$ must be HIGH at the $\overline{RAS}$ HIGH to LOW transition for a DRAM port READ or WRITE operation.

If $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1 - DQ4 port. The $(\overline{TR})/\overline{OE}$ input must be LOW to enable the DRAM output port.

For single port DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the DPDRAM, $(\overline{ME})/\overline{WE}$ is used, when $\overline{RAS}$ goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If $(\overline{ME})/\overline{WE}$ is LOW at the $\overline{RAS}$ HIGH to LOW transition, a MASKED WRITE operation is selected. For a normal DRAM WRITE operation, $(\overline{ME})/\overline{WE}$ must be HIGH at the $\overline{RAS}$ HIGH to LOW transition. $(\overline{ME})/\overline{WE}$ is a "don't care" at the $\overline{RAS}$ HIGH to LOW transition for a DRAM READ cycle.

If $(\overline{ME})/\overline{WE}$ is LOW when $\overline{CAS}$ goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1 - DQ4 port will be written into the selected memory cells. If $\overline{ME}/(\overline{WE})$ is LOW when $\overline{RAS}$ goes LOW, the input data will be "masked" before being stored in the DRAM.

The DPDRAM can perform all the normal DRAM cycles including EARLY-WRITE, LATE-WRITE, READ-WRITE, READ-MODIFY-WRITE, PAGE-MODE READ, PAGE-MODE WRITE, and PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in this data sheet for more details on these operations.

MASK-WRITE

If $\overline{ME}/(\overline{WE})$ is LOW at the $\overline{RAS}$ HIGH to LOW transition, the data (mask data) present on the DQ1 - DQ4 inputs will be written into the bit mask data register. The mask data acts as an individual write enable for each of the four DQ1 - DQ4 pins. If a LOW (logic 0) is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operations to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1 - DQ4 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. Since the mask data register is reset (to all 1's) at the end of every MASKED WRITE cycle, new mask data must be supplied at the beginning of each MASKED WRITE cycle. An example of a typical MASK-WRITE cycle is shown in Figure 2.

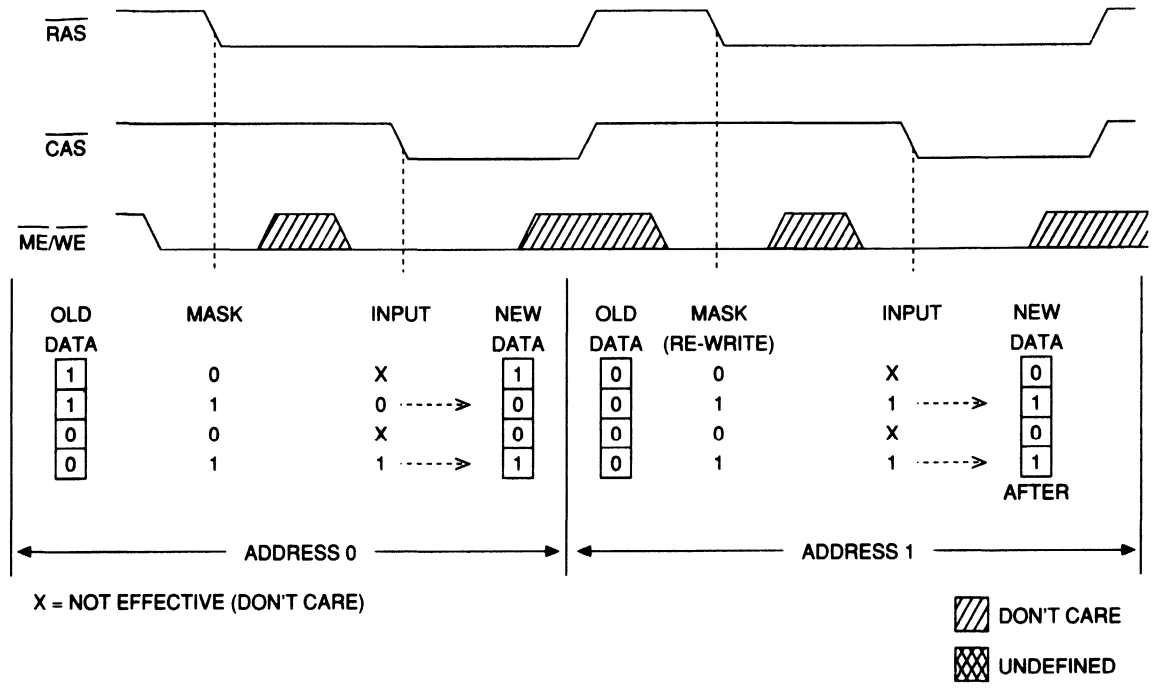


Figure 2
MT42C4064 Bit MASK-WRITE

REFRESH

The MT42C4064 supports $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN types of refresh cycles. All 256 row address combinations must be accessed within 4ms. For the $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh mode, the row addresses are generated internally and the user need not supply them as he must in $\overline{RAS}$ ONLY refresh. $\overline{TR}$/($\overline{OE}$) must be HIGH when $\overline{RAS}$ goes LOW for the $\overline{RAS}$ ONLY and $\overline{CAS}$-BEFORE-$\overline{RAS}$ types of refresh cycles. Any READ, WRITE, or TRANSFER operation also refreshes the DRAM row that is being accessed.

TRANSFER OPERATION

DRAM-TO-SAM TRANSFER (READ TRANSFER)

A TRANSFER operation is initiated when $\overline{TR}/(\overline{OE})$ is LOW at $\overline{RAS}$ (HIGH to LOW) time. $(\overline{ME})/\overline{WE}$ indicates the direction of the transfer and must be HIGH as $\overline{RAS}$ goes LOW for a DRAM-TO-SAM TRANSFER. In this case, the row address bits indicate the four 256 bit DRAM rows that are to be transferred to the four SAM data registers, and the column address bits indicate the start address of the next SERIAL OUTPUT cycle from the SAM data registers. $\overline{RAS}$ and $\overline{CAS}$ are used to strobe the address bits into the part. To complete the TRANSFER, $\overline{TR}/(\overline{OE})$ is taken HIGH while $\overline{RAS}$ and $\overline{CAS}$ are still LOW. The 1024 bits of DRAM data are then written into the SAM data registers and the serial shift start address is stored in an internal 8 bit register. There must be no rising edges on the serial clock (SC) input while the transfer is taking place (refer to the AC timing diagrams). TRANSFER cycles are the only time when SC must be synchronized with the DRAM $\overline{RAS}$ and $\overline{CAS}$ timing. If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation.

SAM-TO-DRAM TRANSFER (WRITE TRANSFER)

The SAM-TO-DRAM TRANSFER operation is identical to the DRAM-TO-SAM TRANSFER described above except that $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row that the SAM data registers will be written to and the column address indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. If $\overline{SE}$ is HIGH when $\overline{RAS}$ goes LOW, a SERIAL INPUT MODE ENABLE cycle is performed.

SAM OPERATION

SERIAL INPUT/OUTPUT MODE CONTROL

The SAM port is automatically placed in the serial output mode after a DRAM-TO-SAM TRANSFER operation. Conversely, after a SAM-TO-DRAM TRANSFER, the SAM port will be in the serial input mode.

SERIAL INPUT MODE ENABLE (PSEUDO WRITE TRANSFER)

It is possible to change the direction of the SAM port from output to input without performing a SAM-TO-DRAM TRANSFER. This operation, called a SERIAL INPUT MODE ENABLE cycle, is simply a SAM-TO-DRAM TRANSFER cycle with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the data registers will be ready to accept input data.

The only way to put the SAM port in the serial output mode is to do a DRAM-TO-SAM TRANSFER.

SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and $\overline{SE}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{SE}$ enables or disables the serial input/output buffers.

Serial output of the SAM data register contents will start at the serial start address that was loaded during the DRAM-TO-SAM TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the four bit port. $\overline{SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW to HIGH transition, regardless of whether $\overline{SE}$ is HIGH or LOW, and will wrap around to location 0 after reaching its maximum count of 255.

SC is also used to clock in data when the device is in the serial input mode. As in the serial output operation, the contents of the serial address register, which was loaded when the serial input mode was enabled, will determine the serial address that the first bit will be written. $\overline{SE}$ acts as an enable for serial data input and must be LOW for normal serial input. If $\overline{SE}$ is HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address register is incremented with every L → H transition of SC, regardless of the logic level on the $\overline{SE}$ input.

TRUTH TABLE

DRAM Operations (SC, $\overline{SE}$, and SDQ1 — SDQ4 are "don't care")

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{ME}/\overline{WE}$		$\overline{TR}/\overline{OE}$		Addresses		DQ1 to DQ4	Notes
			tR*	tC*	tR*	tC*	tR*	tC*		
Standby	H	H	X	X	X	X	X	X	High Impedance	
READ	L	L	X	H	H	H→L	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	H	L	H	X	ROW	COL	Data In	1
MASKED WRITE	H→L	L	L	L	H	X	ROW	COL	Mask Data In, Valid Data In	
READ-WRITE	L	L	H	H→L	H	L→H	ROW	COL	Valid Data Out,	1
PAGE-MODE READ	L	H→L→H, H→L→H	H	H	H	H→L	ROW	COL	Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	H	L	H	X	ROW	COL	Valid Data In	
PAGE-MODE READ-WRITE	L	H→L→H, H→L→H	H	H→L	H	L→H	ROW	COL	Valid Data Out, Valid Data In	1
$\overline{RAS}$ ONLY REFRESH	L	H	X	n/a	H	n/a	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	X	H	H	L	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	X	X	H	X	X	X	High Impedance	

TRANSFER Operations (DQ1 — DQ4 are "don't care")

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{ME}/\overline{WE}$		$\overline{TR}/\overline{OE}$		Addresses		SC	$\overline{SE}$	SDQ1 to SDQ4	Notes
			tR*	tC*	tR*	tC*	tR*	tC*				
DRAM-TO-SAM TRANSFER	L	L	H	X	L	L	ROW	SSA**	X	X	X	2
SAM-TO-DRAM TRANSFER	L	L	L	X	L	X	ROW	SSA**	X	L	X	3
SERIAL INPUT MODE ENABLE	L	L	L	X	L	X	ROW	SSA**	X	H	X	4

* tR = when $\overline{RAS}$ goes from HIGH to LOW
tC = when $\overline{CAS}$ goes from HIGH to LOW
** SSA = SAM Start Address, the serial address that the next serial input or output cycle will start with

Notes: 1. Any type of WRITE cycle may also be a MASKED WRITE cycle.
2. The SAM will be in a SERIAL OUTPUT mode after a DRAM-TO-SAM TRANSFER.
3. The SAM will be in a SERIAL INPUT mode after a SAM-TO-DRAM TRANSFER.
4. The SAM will be put in the SERIAL INPUT mode but the SAM-TO-DRAM TRANSFER will not occur.

Serial I/O Operations ($\overline{RAS}$, $\overline{CAS}$, $\overline{ME/WE}$, $\overline{TR/OE}$, and DQ1 - DQ4 are "don't care")

Function	SC	$\overline{SE}$	SDQ1 — SDQ4	Notes
SERIAL OUTPUT	L→H	L	Valid Data Out	5
SERIAL INPUT	L→H	L	Valid Data In	6

Notes: 5. The SAM must be in the SERIAL OUTPUT mode.
6. The SAM must be in the SERIAL INPUT mode.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V
Operating Temperature, Ta(Ambient) .....0°C to +70°C
Storage Temperature (Ceramic) .....-65°C to +150°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation .....1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	$V_{CC}+1$	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(Notes 3, 4, 5) ($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts).	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, $0V \le V_{OUT} \le V_{CC}$).	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_7	C_{I1}		5	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, SC, $\overline{SE}$	C_{I2}		7	pF	18
Output Capacitance: DQ, SDQ	C_O		7	pF	18

CURRENT DRAIN, SAM IN STANDBY

(Notes 2, 3) ($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

PARAMETER/CONDITION OF DRAM	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$=Cycling; T_{RC}=$T_{RC(MIN)}$).	I_{CC1}		40	mA	4
OPERATING CURRENT: PAGE-MODE ($\overline{RAS}$=V_{IL},$\overline{CAS}$=Cycling; T_{PC}=$T_{PC(MIN)}$).	I_{CC2}		40	mA	4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH} after 8 $\overline{RAS}$ cycles min).	I_{CC3}		10	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V).	I_{CC4}		4	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH}).	I_{CC5}		30	mA	
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling).	I_{CC6}		30	mA	5
SAM/DRAM DATA TRANSFER	I_{CC7}		60	mA	

CURRENT DRAIN, SAM ACTIVE (tsc = MIN)

(Notes 2, 3) ($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

PARAMETER/CONDITION OF DRAM	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$=Cycling; T_{RC}=$T_{RC(MIN)}$).	I_{CC8}		60	mA	4
OPERATING CURRENT: PAGE-MODE ($\overline{RAS}$=V_{IL},$\overline{CAS}$=Cycling; T_{PC}=$T_{PC(MIN)}$).	I_{CC9}		60	mA	4
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH} after 8 $\overline{RAS}$ cycles min).	I_{CC10}		30	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2V).	I_{CC11}		25	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH}).	I_{CC12}		50	mA	
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling).	I_{CC13}		50	mA	5
SAM/DRAM DATA TRANSFER	I_{CC14}		90	mA	

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 10, 11, 17) (0°C ≤ T_A ≤ + 70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^tRWC	250		295		345		ns	20, 21
PAGE-MODE READ or WRITE cycle time	^tPC	75		90		110		ns	6, 7
PAGE-MODE READ-MODIFY-WRITE cycle time	^tPRWC	125		150		175		ns	20, 21
Access time from $\overline{RAS}$	^tRAC		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	^tCAC		50		60		75	ns	7, 9
$\overline{RAS}$ pulse width	^tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ pulse width (PAGE-MODE)	^tRASP	100	100,000	120	100,000	150	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	50		60		75		ns	
$\overline{RAS}$ precharge time	^tRP	80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	15		20		25		ns	
$\overline{CAS}$ precharge time (PAGE-MODE)	^tCP	15		20		25		ns	19
$\overline{RAS}$ to $\overline{CAS}$ delay	^tRCD	10	50	15	60	15	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
Row address set-up time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	15		15		15		ns	
Column address set-up time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	20		20		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		70		80		ns	
READ command set-up time	^tRCS	0		0		0		ns	
READ command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
READ command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	

DRAM TIMING PARAMETERS (Continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 10, 11, 17) (0°C ≤ T_A ≤ + 70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{WE}$ command set-up time	^tWCS	0		0		0		ns	16
WRITE command hold time	^tWCH	20		25		30		ns	
WRITE command hold time (referenced to $\overline{RAS}$)	^tWCR	70		80		90		ns	
WRITE command pulse width	^tWP	20		25		30		ns	
WRITE command to $\overline{RAS}$ lead time	^tRWL	25		30		35		ns	
WRITE command to $\overline{CAS}$ lead time	^tCWL	25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	15		20		25		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	70		80		90		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	^tCWD	65		80		95		ns	16, 20
$\overline{RAS}$ to $\overline{WE}$ delay	^tRWD	120		150		185		ns	16, 20
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ Set Up Time	^tWSR	0		0		0	ns		
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ Hold Time	^tRWH	10		10		15	ns		
Mask Data (DQ_) to $\overline{RAS}$ Set Up Time	^tMS	0		0		0		ns	
Mask Data (DQ_) to $\overline{RAS}$ Hold Time	^tMH	20		20		25		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	
Refresh Period (256 cycles)	^tREF		4		4		4	ms	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	20		25		30		ns	22
$\overline{CAS}$ to output in low-Z	^tCLZ	5		5		5		ns	
Output buffer turn-off delay	^tOFF	0	25	0	25	0	30	ns	12
Output Enable	^tOE		25		25		30	ns	
Output Disable	^tOD		25		25		30	ns	

NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms static refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (max).
10. If $\overline{CAS}$ = V_{IH}, DRAM data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, DRAM data output may contain data from the last valid READ cycle.
12. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and to $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (min), the cycle is an EARLY-WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $^tCWD \ge ^tCWD$ (min) and $^tRWD \ge ^tRWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the state of data out (at access time and until $\overline{CAS}$ goes back toV_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. Includes the $\overline{OE}$ delay time (30ns for the -10, 40ns for the -12, and 50ns for the -15).
21. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH (V_{IH}) DQ goes open. If $\overline{OE}$ is tied permanently LOW a READ-MODIFY-WRITE operation is not possible.
22. Enables on-chip refresh and address counters.
23. TRANSFER command means that $\overline{TR}/(\overline{OE})$ is LOW when $\overline{RAS}$ goes LOW.
24. NON-TRANSFER command means that $\overline{TR}/(\overline{OE})$ is HIGH when $\overline{RAS}$ goes LOW.
25. Measured with a load equivalent to 2 TTL gates and 50pF.

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 17, 25) (0° C ≤ T_A ≤ + 70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
TRANSFER Command to $\overline{RAS}$ Set Up Time	^tTS	0		0		0		ns	23
TRANSFER Command to $\overline{RAS}$ Hold Time	^tRTH	80		90		100		ns	23
TRANSFER Command to $\overline{CAS}$ Hold Time	^tCTH	30		30		35		ns	23
TRANSFER Command to SC Lead Time	^tTSL	5		5		10		ns	23
TRANSFER Command to $\overline{RAS}$ Lead Time	^tTRL	10		10		10		ns	23
TRANSFER Command to $\overline{RAS}$ Delay Time	^tTRD	15		15		20		ns	23
TRANSFER Command to $\overline{CAS}$ Time	^tTCL	10		10		10		ns	23
TRANSFER Command to $\overline{CAS}$ Delay Time	^tTCD	15		15		20		ns	23
First SC edge to TRANSFER Command Delay Time	^tTSD	10		10		20		ns	23
SAM-TO-DRAM (WRITE) Transfer Command to $\overline{RAS}$ Hold Time	^tRTHW	10		10		15		ns	
Serial Output Buffer Turn Off Delay from $\overline{RAS}$	^tSDZ	10	40	10	50	10	60	ns	
SC to $\overline{RAS}$ Set Up Time	^tSRS	35		40		45		ns	
$\overline{RAS}$ to SC Delay Time	^tSRD	25		30		35		ns	
Serial Data Input to SE Delay Time	^tSZE	0		0		0		ns	
$\overline{RAS}$ to SD Buffer Turn On Time	^tSRO	0		0		0		ns	
Serial Data Input Delay from $\overline{RAS}$	^tSDD	50		55		60		ns	
Serial Data Input to $\overline{RAS}$ Delay Time	^tSZS	0		0		0		ns	
Serial Input Mode Enable (SE) to $\overline{RAS}$ Set Up Time	^tESR	0		0		0		ns	
Serial Input Mode Enable (SE) to $\overline{RAS}$ Hold Time	^tREH	10		10		15		ns	
NON-TRANSFER Command to $\overline{RAS}$ Set Up Time	^tYS	0		0		0		ns	24
NON-TRANSFER Command to $\overline{RAS}$ Hold Time	^tYH	15		15		20		ns	24

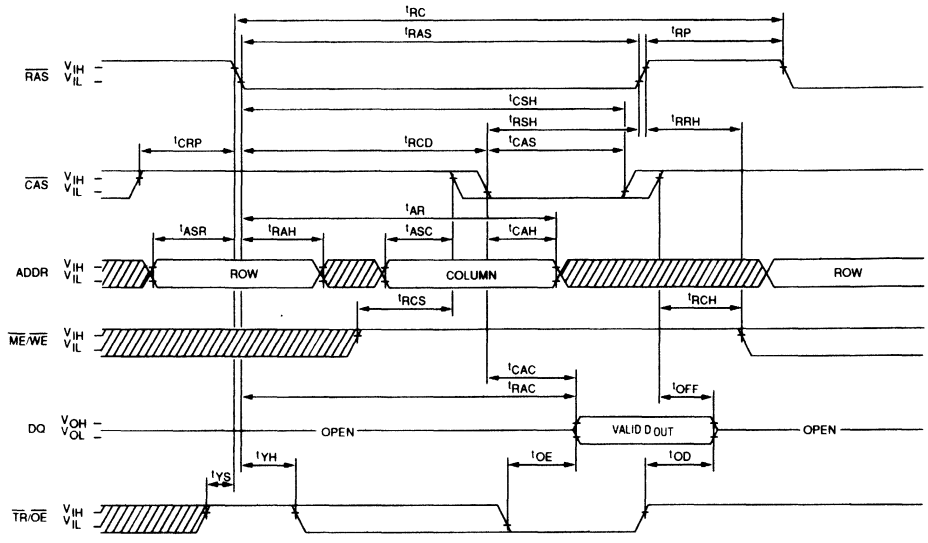
SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

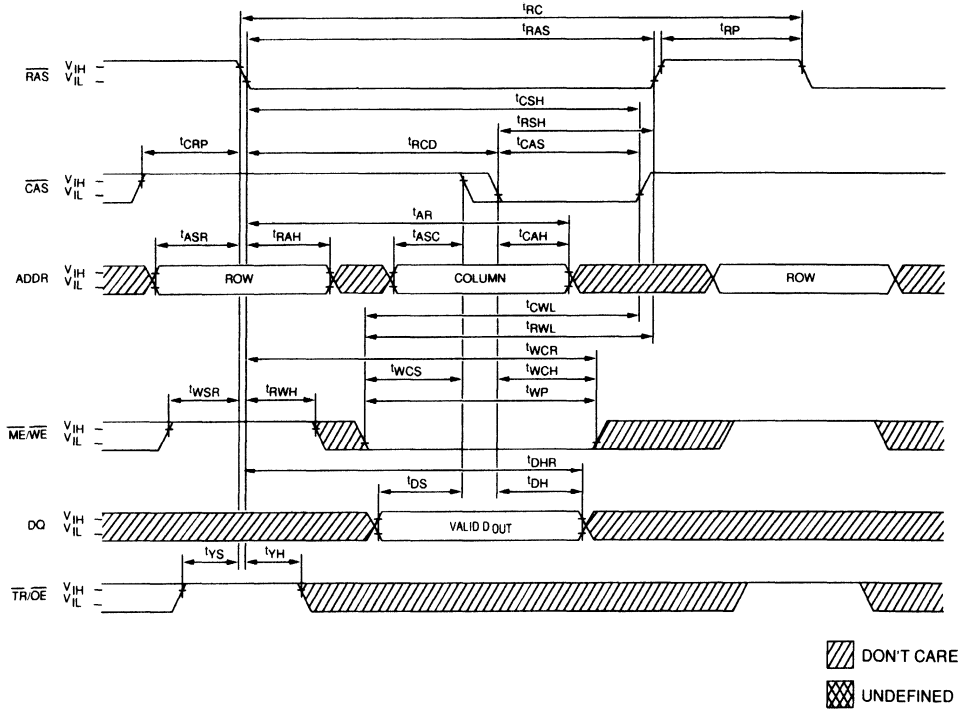
(Notes 3, 4, 5, 17, 25) (0° C ≤ T_A ≤ + 70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial Clock Cycle Time	^tSC	33	50000	40	50000	60	50000	ns	
Access Time from SC	^tSAC		33		40		60	ns	
SC Precharge Time	^tSP	10		10		20		ns	
SC Pulse Width	^tSAS	10		10		20		ns	
Access Time from SE	^tSEA		25		30		40	ns	
SE Precharge Time	^tSEP	10		15		20		ns	
SE Pulse Width	^tSE	15		15		20		ns	
Serial Data Out Hold Time after SC High	^tSOH	10		10		10		ns	
Serial Output Buffer Turn Off Delay from SE	^tSEZ	0	15	0	25	0	30	ns	
Serial Data in Set Up Time	^tSDS	0		0		0		ns	
Serial Data in Hold Time	^tSDH	15		20		25			
SERIAL INPUT (Write) Enable Set Up Time	^tSWS	0		0		0		ns	
SERIAL INPUT (Write) Enable Hold Time	^tSWH	20		35		45		ns	
SERIAL INPUT (Write) Disable Set Up Time	^tSWIS	0		0		0		ns	
SERIAL INPUT (Write) Disable Hold Time	^tSWIH	20		35		45		ns	

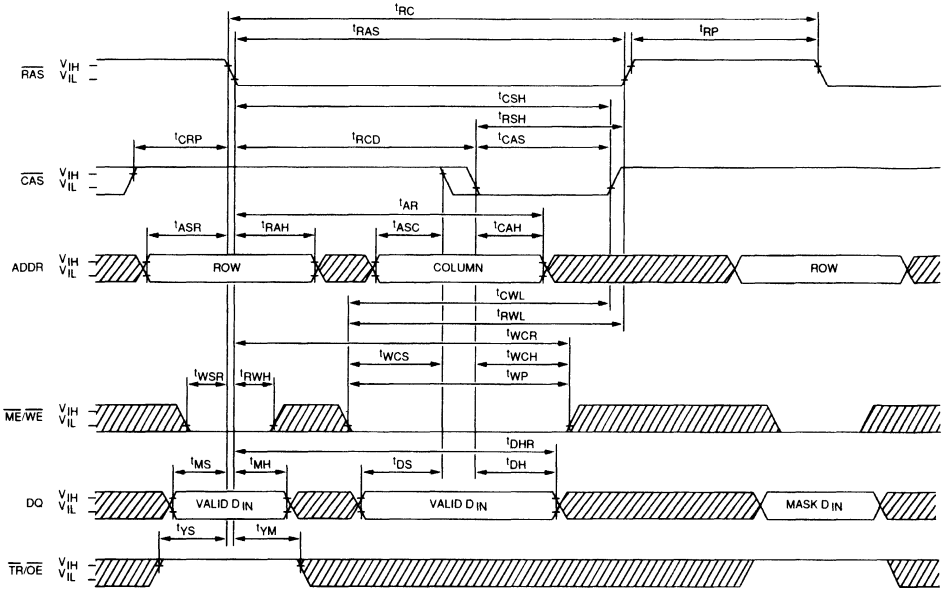
DRAM READ CYCLE



DRAM EARLY-WRITE CYCLE

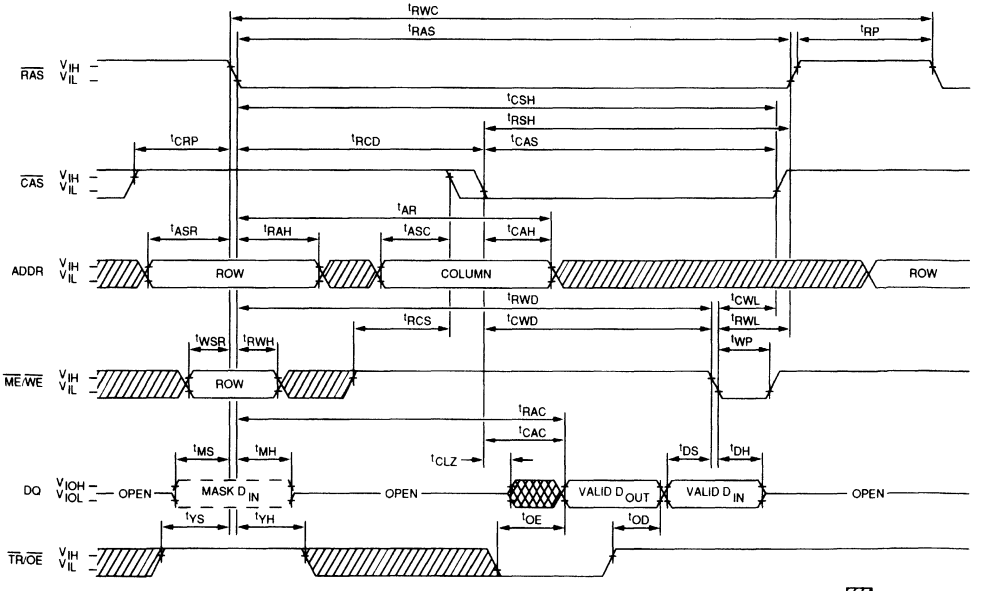


DRAM MASKED WRITE CYCLE



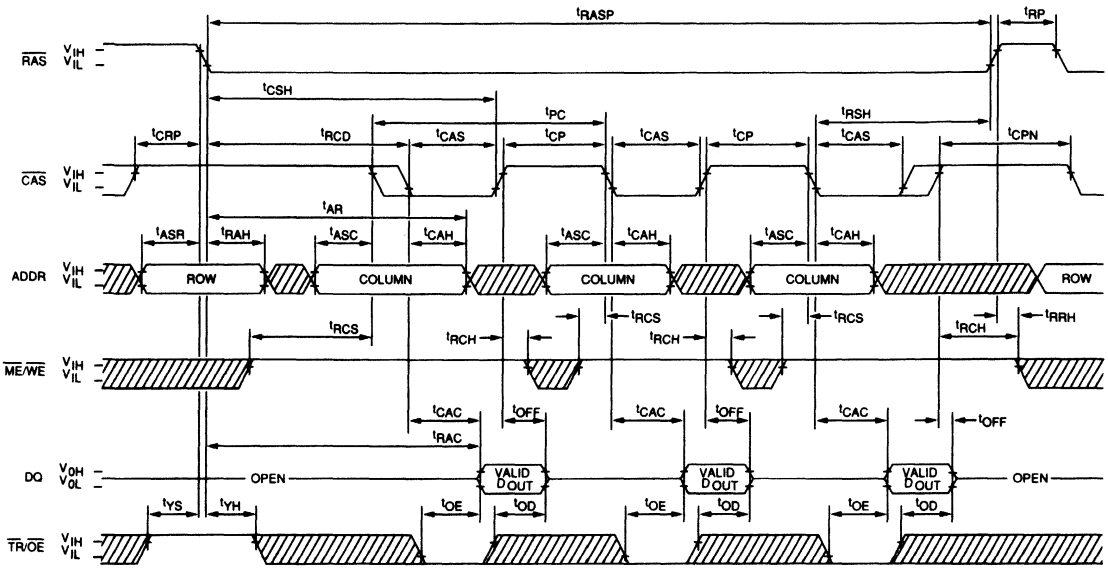
DRAM READ-WRITE CYCLE

(READ-MODIFY-WRITE CYCLE and LATE-WRITE CYCLE)

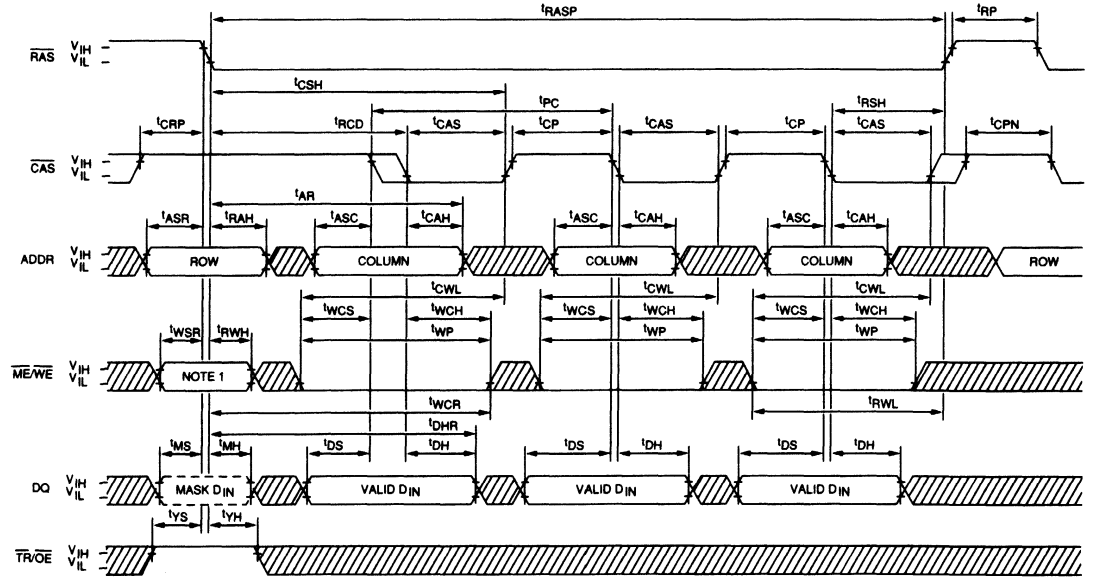


NOTE 1: If $\overline{ME}/\overline{WE}$ is LOW, a MASKED WRITE cycle will be performed.

DRAM PAGE-MODE READ CYCLE

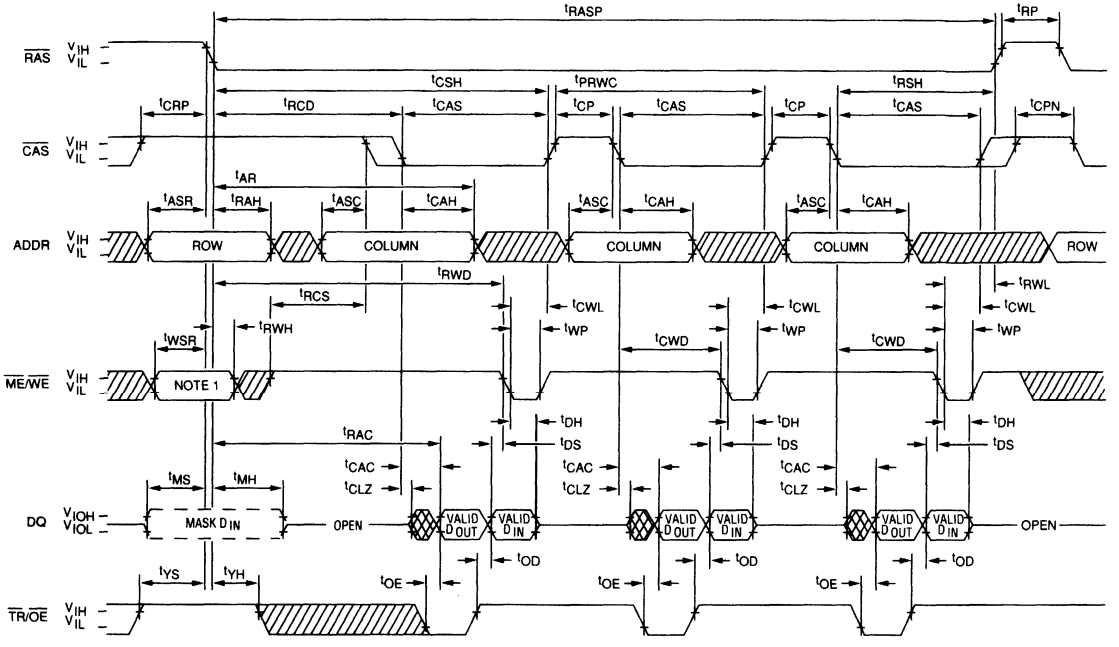


DRAM PAGE-MODE EARLY-WRITE CYCLE



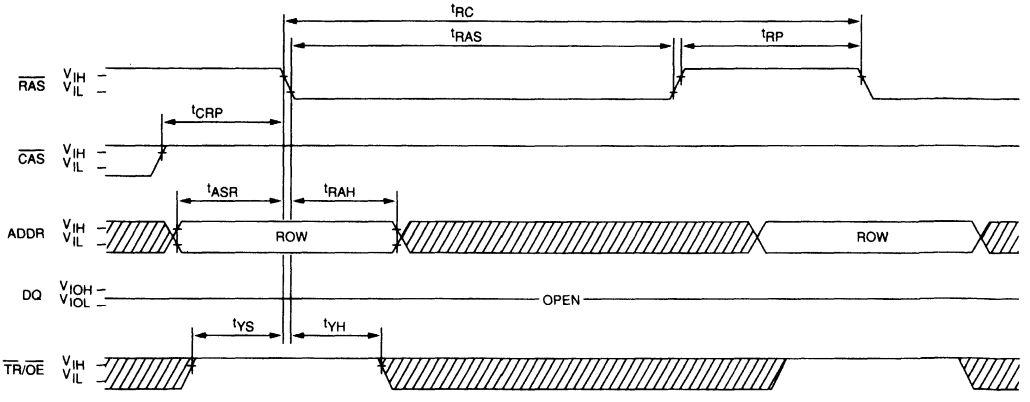
NOTE: If $\overline{ME}/\overline{WE}$ is LOW, a MASKED WRITE cycle will be performed.

DRAM PAGE-MODE READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



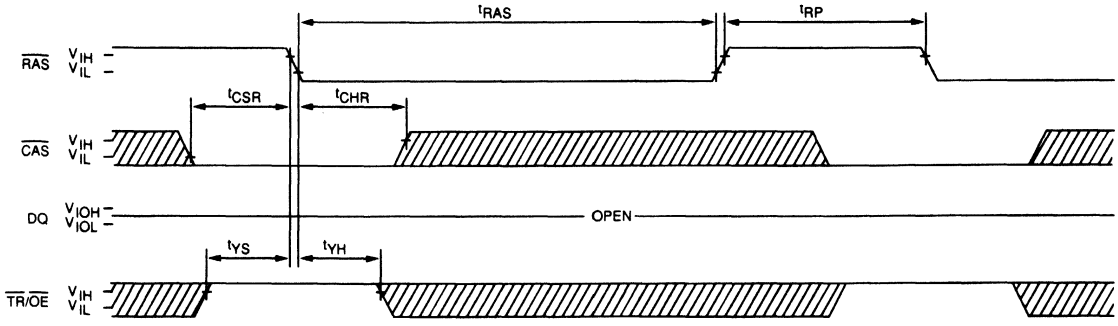
NOTE: 1: If $\overline{ME}/\overline{WE}$ is LOW, a MASKED WRITE cycle will be performed.

$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{ME}/\overline{WE}$ = Don't Care)

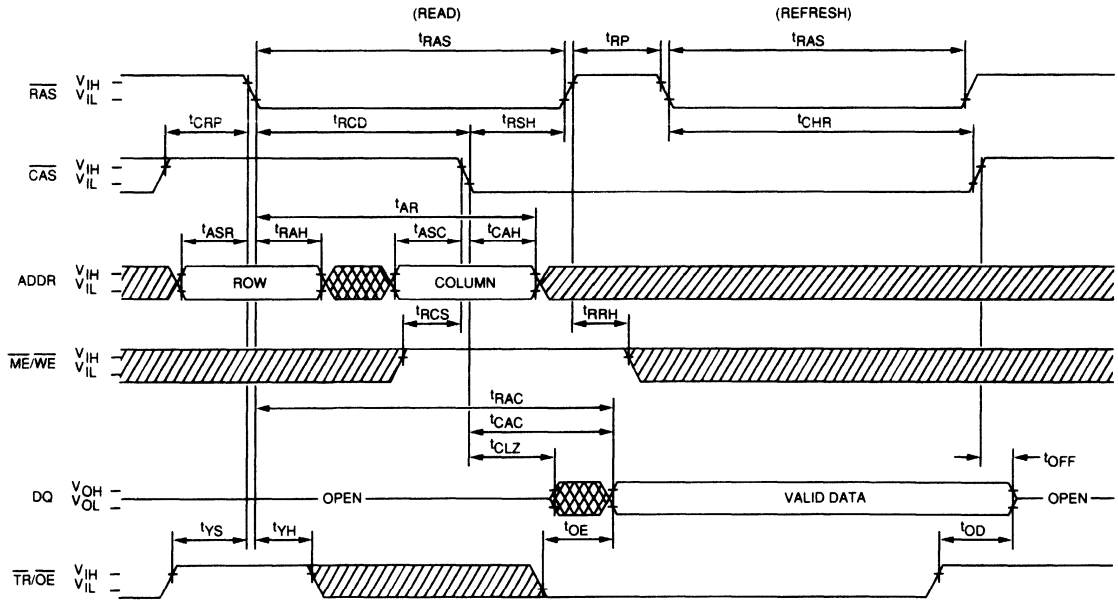


CAS-BEFORE-RAS REFRESH CYCLE

(A_0 - A_7 and ME/WE are Don't Care.)



HIDDEN REFRESH CYCLE



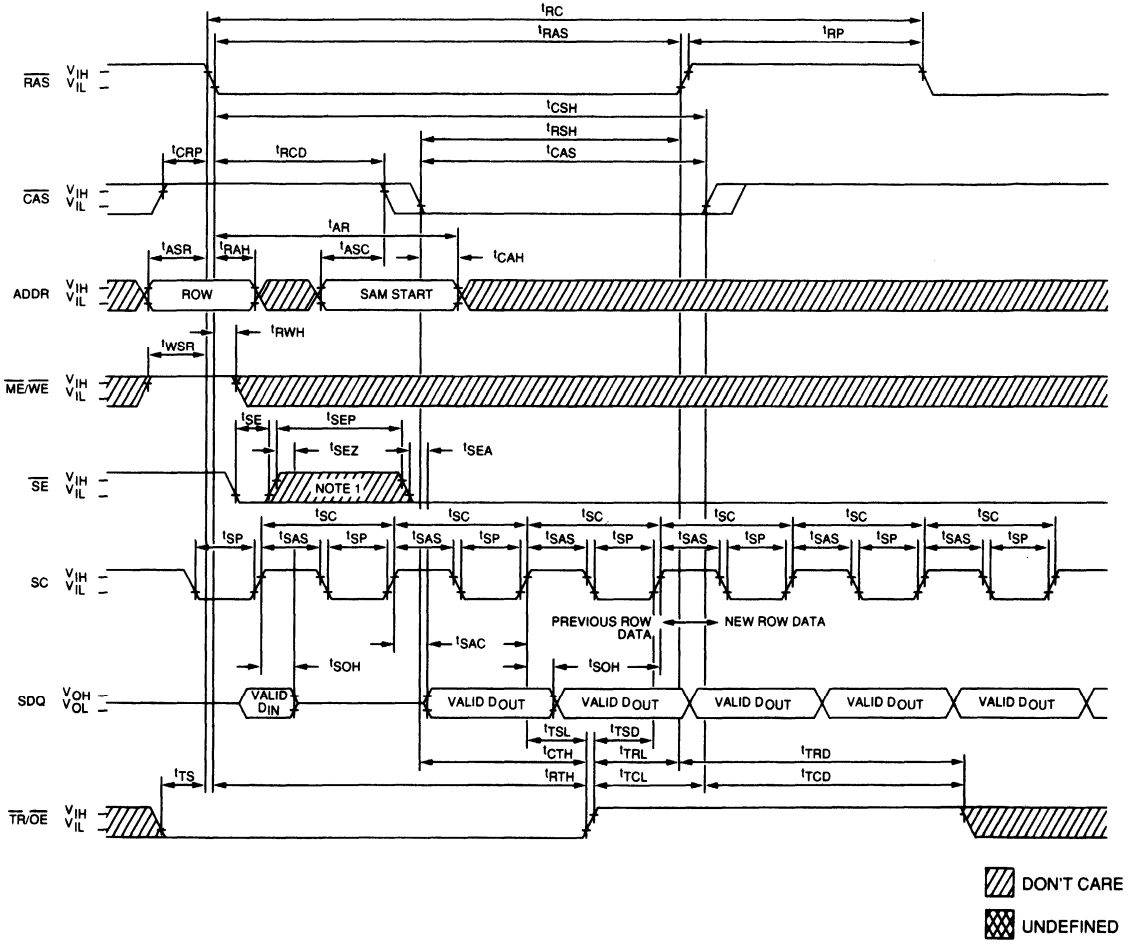
DON'T CARE

UNDEFINED

NOTE: A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case ME/WE = LOW (when CAS goes LOW) and TR/OE = HIGH.

DRAM-TO-SAM TRANSFER
(READ TRANSFER)

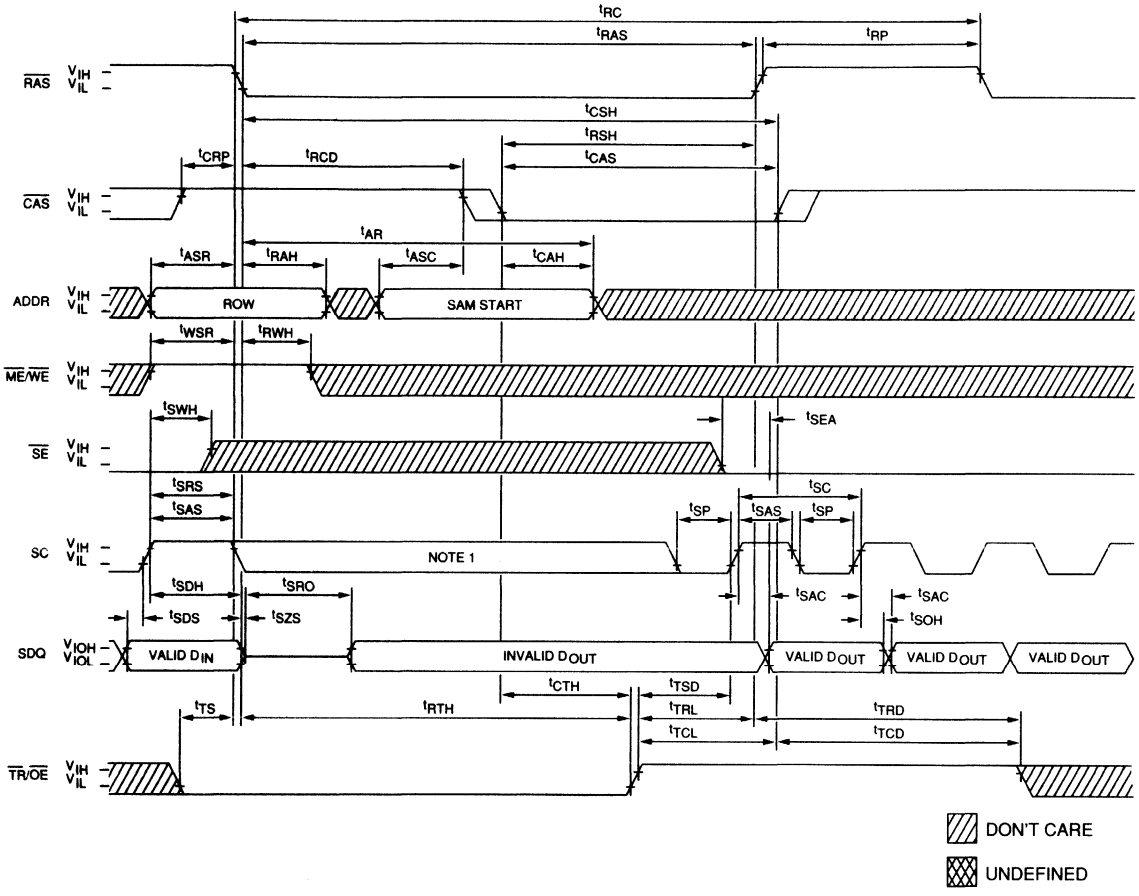
(When part was previously in the SERIAL OUTPUT mode.)



NOTE 1: This $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.

DRAM-TO-SAM TRANSFER
(READ TRANSFER)

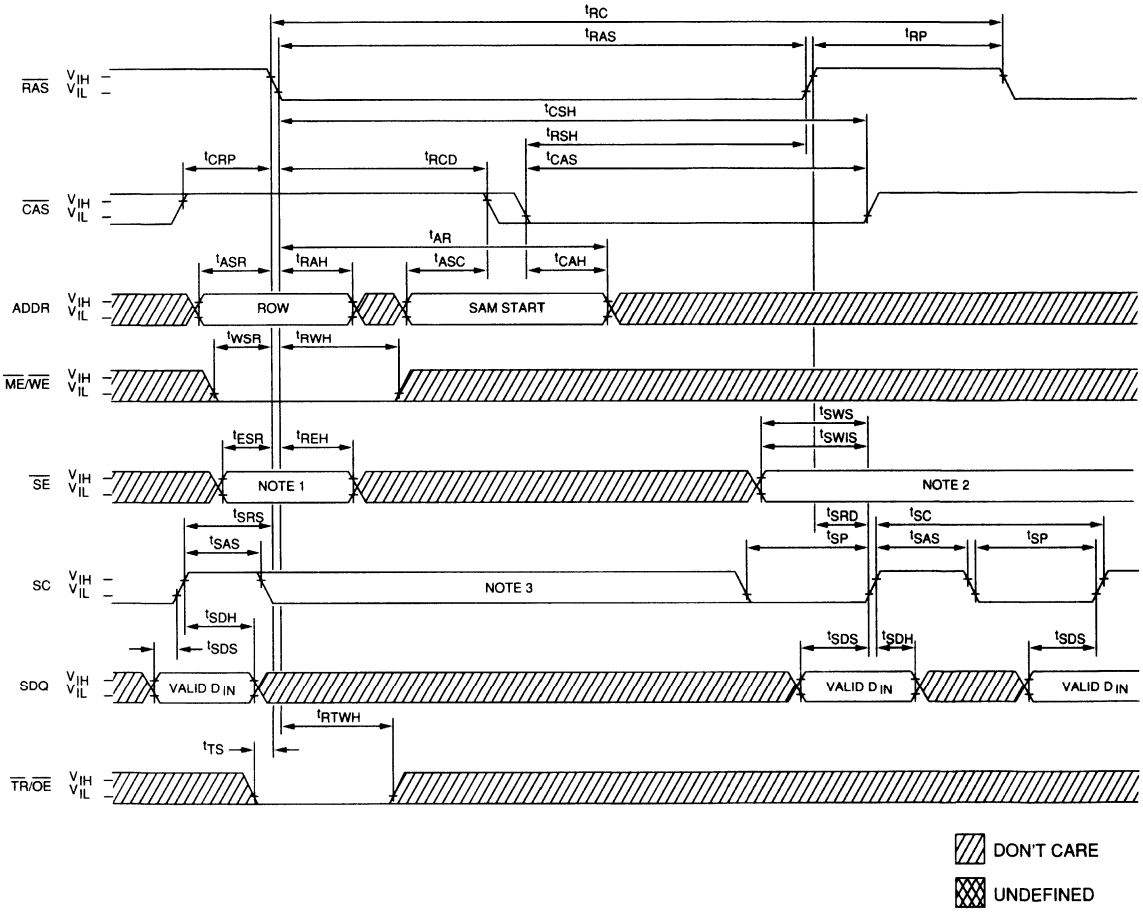
(When part was previously in the SERIAL INPUT mode.)



NOTE 1: There must be no rising edges on the SC input during this time.

SAM-TO-DRAM TRANSFER (WRITE TRANSFER)

(When part was previously in the SERIAL INPUT mode.)

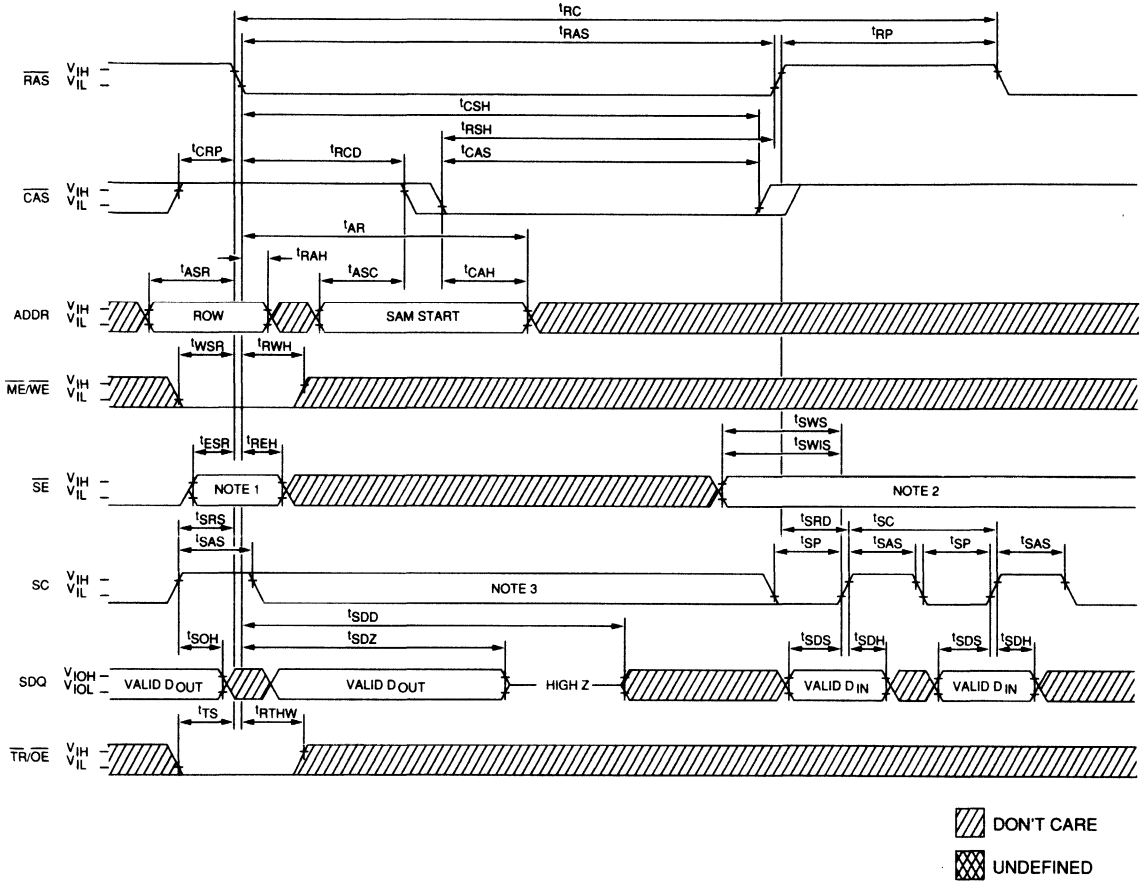


NOTE 1: If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

NOTE 2: $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.

NOTE 3: There must be no rising edges on the SC input during this time.

SAM-TO-DRAM TRANSFER
(WRITE TRANSFER or PSEUDO WRITE TRANFER)
(When part was previously in the SERIAL OUTPUT mode.)

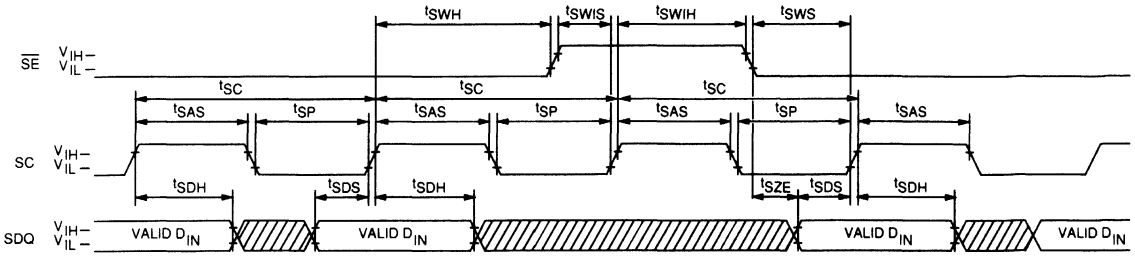


NOTE 1: If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

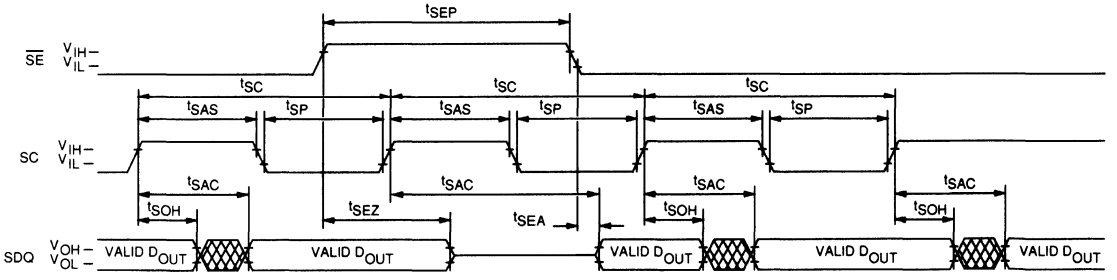
NOTE 2: $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.

NOTE 3: There must be no rising edges on the SC input during this time.

SAM SERIAL INPUT



SAM SERIAL OUTPUT



DON'T CARE

UNDEFINED

VRAM

128K x 8 DRAM with 256 x 8 SAM

FEATURES

- Industry standard pin-out timing, and functions
- High performance CMOS silicon gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512 cycle refresh within 8ms
- Optional FAST PAGE MODE access cycles
- Dual port organization: 128K x 8 DRAM port
  256 x 8 SAM port
- No refresh required for Serial Access Memory
- Low power: 5mW standby; 200mW active, typical
- Fast access times – 80ns random, 25ns serial

SPECIAL FUNCTIONS

- JEDEC Standard Function set
- PERSISTENT MASK WRITE
- SPLIT READ TRANSFER
- Serial Input
- ALTERNATE WRITE TRANSFER
- BLOCK WRITE

OPTIONS / MARKING

OPTIONS	MARKING
• Timing (DRAM, SAM)	
80ns, 25ns	-8
100ns, 30ns	-10
120ns, 35ns	-12
150ns, 40ns	-15

PIN ASSIGNMENT (Top View)

40-Pin DIP 600 MIL

SC	1	40	Vss1
SDQ1	2	39	SDQ8
SDQ2	3	38	SDQ7
SDQ3	4	37	SDQ6
SDQ4	5	36	SDQ5
$\overline{TR/OE}$	6	35	$\overline{SE}$
DQ1	7	34	DQ8
DQ2	8	33	DQ7
DQ3	9	32	DQ6
DQ4	10	31	DQ5
Vcc1	11	30	Vss2
$\overline{ME/WE}$	12	29	DSF
NC	13	28	NC
$\overline{RAS}$	14	27	$\overline{CAS}$
NC	15	26	QSF
A8	16	25	A0
A6	17	24	A1
A5	18	23	A2
A4	19	22	A3
Vcc2	20	21	A7

40-Pin SOJ 400 MIL

SC	1	40	Vcc1
SDQ1	2	39	SDQ8
SDQ2	3	38	SDQ7
SDQ3	4	37	SDQ6
SDQ4	5	36	SDQ5
$\overline{TR/OE}$	6	35	$\overline{SE}$
DQ1	7	34	DQ8
DQ2	8	33	DQ7
DQ3	9	32	DQ6
DQ4	10	31	DQ5
Vcc1	11	30	Vss2
$\overline{ME/WE}$	12	29	DSF
NC	13	28	NC
$\overline{RAS}$	14	27	$\overline{CAS}$
NC	15	26	QSF
A8	16	25	A0
A6	17	24	A1
A5	18	23	A2
A4	19	22	A3
Vcc2	20	21	A7

GENERAL DESCRIPTION

The MT42C8128 is a high speed, dual port CMOS dynamic random access memory (DPDRAM) containing 1,048,576 bits. They can be accessed either by an eight bit wide DRAM port or by a 256 x 8 bit serial access memory (SAM) port. Data can be transferred bidirectionally between the DRAM and the SAM.

Eight 256 bit data registers make up the serial access memory portion of the DPDRAM. Data I/O and internal data transfer is accomplished using three separate bidirectional data paths; the eight bit random access I/O port, the eight internal 256 bit wide paths between the DRAM and the SAM, and the eight bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the DPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the DPDRAM is fully static and does not require any refresh.

The operation and control of the MT42C8128 is compatible with the operation of the MT42C4064 (64Kx4) Video RAM. However, the MT42C8128 offers several additional functions which may be used to increase system performance or ease critical timing requirements. These "special functions" are described in detail in the following section.

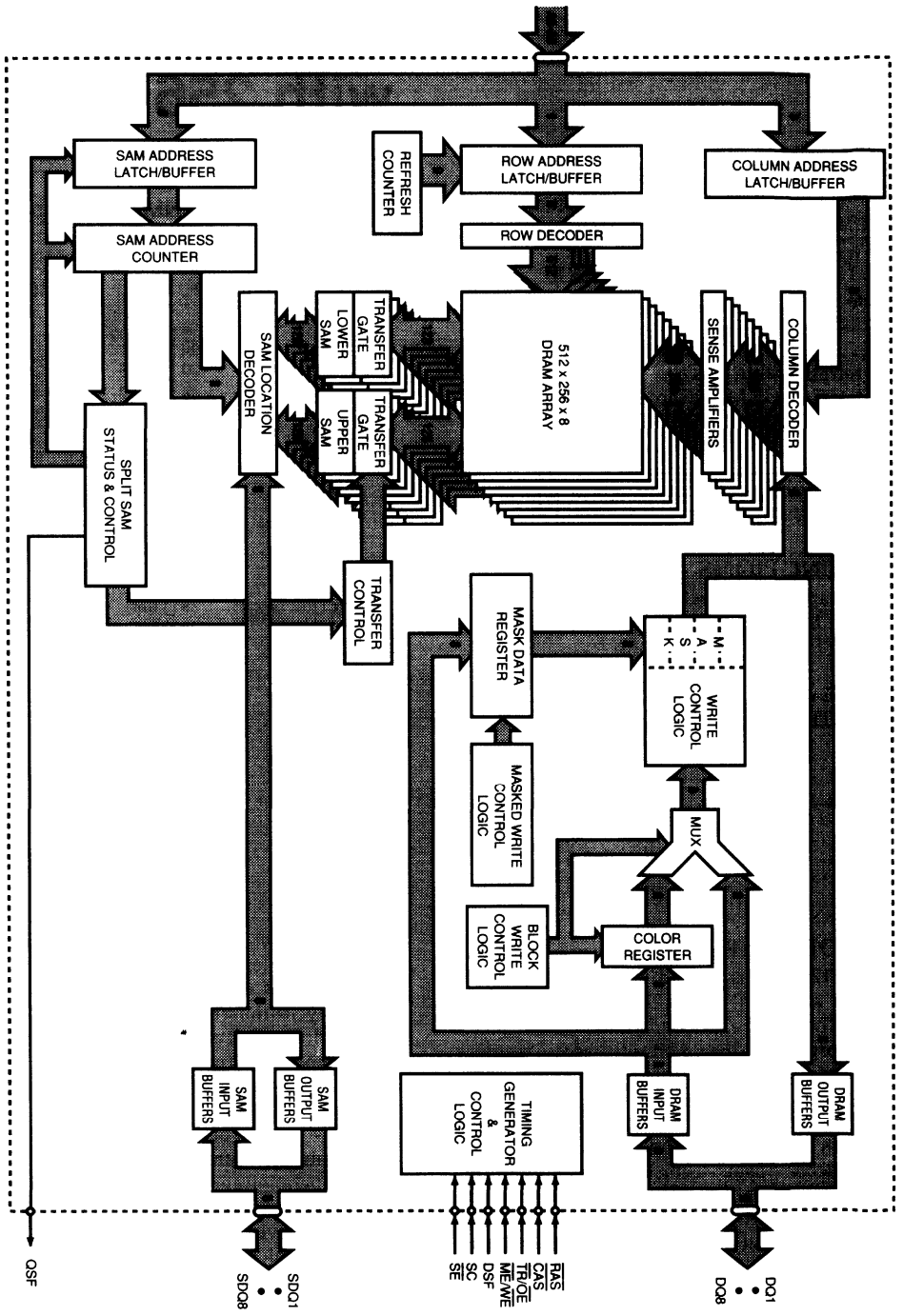


Figure 1
MT42C8128 BLOCK DIAGRAM

PIN DESCRIPTIONS

DIP/SOJ PIN NUMBER(S)	ZIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
1		SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
6		$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a high impedance state.
12		$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$, a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
35		$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a high impedance state. $\overline{SE}$ is also used during a WRITE TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
29		DSF	Input	Special Function Select: DSF is used to indicate which special functions (Block Write, Masked Write vs. Persistent Masked Write, etc.) are used on a particular access cycle.
14		$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 9 row address bits and as a strobe for the $\overline{ME/WE}$, $\overline{TR/OE}$, DSF and DQ inputs.
27		$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the 9 column address bits, enable the DRAM output buffers (along with $\overline{TR/OE}$), and as a strobe for the DSF input.
16, 17, 18 19, 21, 22 23, 24, 25		A0 to A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select 8 bits out of the 128K x 8 available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and the SAM start address (when $\overline{CAS}$ goes LOW).
7, 8, 9, 10, 31 32, 33, 34		DQ1 - DQ8	Input/ Output	DRAM Data I/O inputs for MASK DATA REGISTER and COLOR REGISTER load cycles, and ADDRESS MASK inputs for BLOCK WRITE.
2, 3, 4, 5, 36 37, 38, 39		SDQ1 - SDQ8	Input/ Output	Serial Data I/O: Input, Output, or high impedance.
26		QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed when the Split SAM Transfer mode is being used.
28		NC	–	No Connect - This pin should be either left unconnected or tied to ground.
11, 20		Vcc	Supply	Power Supply: +5 Volts 10%
30, 40		Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C8128 can be divided into three functional blocks (see Figure 1); the DRAM, the transfer circuitry, and the serial access memory (SAM). All of the operations described below are also shown in the AC Timing Diagrams section of this data sheet as well as summarized in the Truth Table.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing transfer operations the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM based memory, the MT42C8128 Video RAM must be refreshed to retain data. All 512 row address combinations must be accessed within 8ms. The MT42C8128 supports $\overline{CAS}$-BEFORE-$\overline{RAS}$, $\overline{RAS}$ ONLY and HIDDEN types of refresh cycles.

For the $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh mode, the row addresses are generated and stored in an internal address counter. The user need not supply any address data and simply must perform 512 $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles within the 8ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for $\overline{RAS}$ ONLY refresh cycles. The DQ I/O pins remain in a high -Z state for both the $\overline{RAS}$ ONLY and $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycles.

HIDDEN refresh cycles are performed by toggling $\overline{RAS}$ (and keeping $\overline{CAS}$ LOW) after a READ or WRITE cycle. This performs $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM portion of the MT42C8128 does not require any refreshing.

DRAM READ AND WRITE CYCLES

The DRAM portion of the DPDRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or "don't care" states for the DRAM are specified for the DPDRAM. These conditions are highlighted in the following discussion. In addition, the DPDRAM has several special functions that can be used when writing to the DRAM.

The 17 address bits that are used to select eight memory bits from the 131,077 x 8 available are latched into the chip using the A0-A8, $\overline{RAS}$, and $\overline{CAS}$ inputs. First, the 9 row address bits are set-up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH to LOW. Next, the 8 column address bits are set-up on the address inputs and clocked in when $\overline{CAS}$ goes from HIGH to LOW.

For single port DRAMs, the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. For the DPDRAM, $(\overline{TR})/\overline{OE}$ is used, when $\overline{RAS}$ goes LOW, to select between DRAM and TRANSFER cycles. $(\overline{TR})/\overline{OE}$ must be HIGH at the $\overline{RAS}$ HIGH to LOW transition for all DRAM operations (except $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh).

If $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ8 port. The $(\overline{TR})/\overline{OE}$ input must transition from HIGH to LOW sometime after $\overline{RAS}$ falls to enable the DRAM output port.

For single port normal DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the DPDRAM, $(\overline{ME})/\overline{WE}$ is used, when $\overline{RAS}$ goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If $(\overline{ME})/\overline{WE}$ is LOW at the $\overline{RAS}$ HIGH to LOW transition, a MASKED WRITE operation is selected. For any DRAM access cycle (READ or WRITE), $(\overline{ME})/\overline{WE}$ must be HIGH at the $\overline{RAS}$ HIGH to LOW transition. If $(\overline{ME})/\overline{WE}$ is LOW when $\overline{CAS}$ goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1-DQ8 data port will be written into the selected memory cells.

The DPDRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, PAGE-MODE READ, PAGE-MODE WRITE, and PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

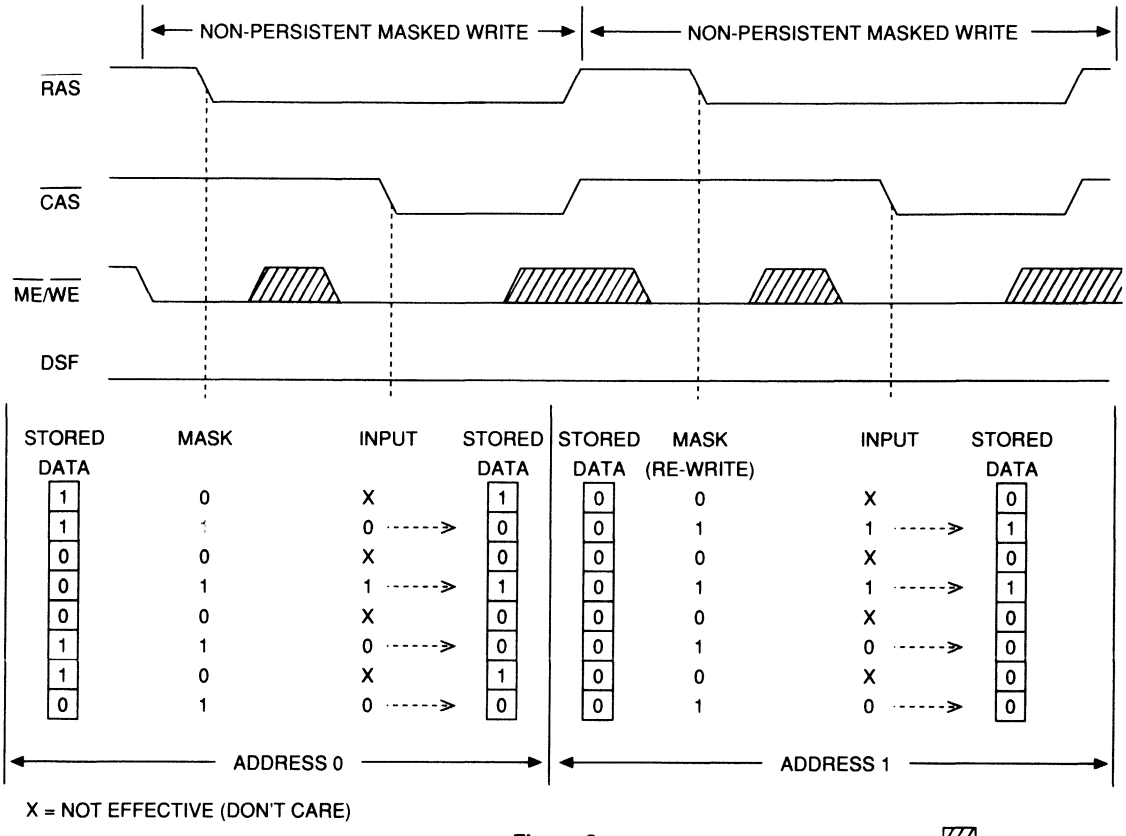


Figure 2
NON-PERSISTENT MASKED WRITE EXAMPLE

NON-PERSISTENT MASKED WRITE

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only certain bits within an eight bit word. The MT42C8128 supports two types of MASKED WRITE cycles, NON-PERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}$/($\overline{WE}$) is LOW and DSF is LOW at the $\overline{RAS}$ HIGH to LOW transition, the data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the four DQ1-DQ8 pins. If a LOW (logic 0) is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. When using NON-PERSISTENT MASKED WRITE, the data present on the DQ inputs is loaded into the mask data register at the falling edge of $\overline{RAS}$. FAST PAGE MODE can be used with NON-PERSISTENT MASKED WRITE to write several column locations. The same mask is used during the entire FAST PAGE $\overline{RAS}$ cycle. An example of NON-PERSISTENT MASKED WRITE cycle is shown in Figure 2.

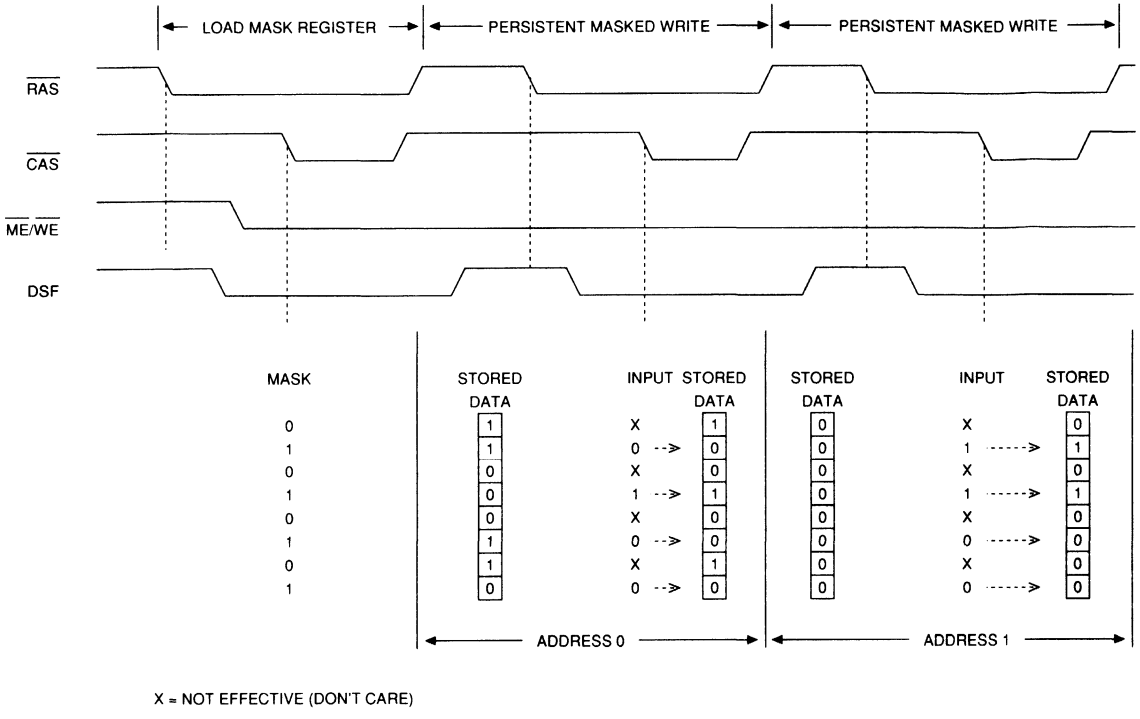


Figure 3
PERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/\overline{WE}$ HIGH and DSF HIGH when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW. Mask data may also be loaded into the mask register by performing a NON-PERSISTENT MASKED WRITE cycle before the PERSISTENT MASKED WRITE cycles.

PERSISTENT MASKED WRITE cycles can then be performed by simply taking $\overline{ME}/(\overline{WE})$ LOW and DSF HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NON-PERSISTENT MASKED WRITE cycle, the data present on the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls. Another PERSISTENT MASKED WRITE cycle can be performed without having to reload the mask data register. Figure 3 shows the LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycle operation. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow controllers that cannot put data out at $\overline{RAS}$ time to perform MASKED WRITES. PERSISTENT MASKED WRITE can be performed during FAST PAGE MODE cycles.

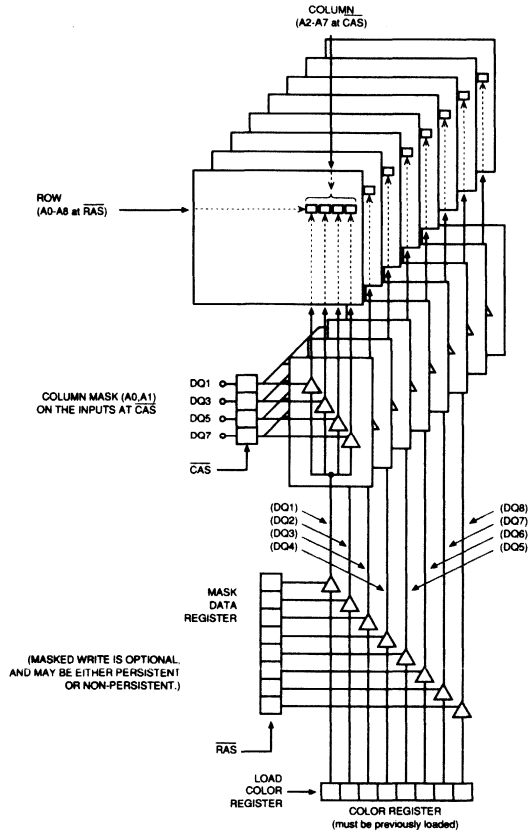


Figure 4
BLOCK WRITE EXAMPLE

BLOCK WRITE

If DSF is LOW when $\overline{CAS}$ goes LOW, the MT42C8128 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to eight adjacent column locations (see Figure 4). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The ROW is addressed as in a normal DRAM WRITE cycle, however when $\overline{CAS}$ goes LOW only the A2-A7 inputs are used. A2-A7 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs (DQ1, 3, 5, and 7) are then used to determine what combination of the eight column locations will be changed. The table on this page illustrates how each of the DQ inputs is used to selectively enable or disable individual column locations within the block. The write enable controls are active HIGH; a logic 1 enables the WRITE funtion and a logic 0 disables the WRITE function.

The contents of the color register will then be written to the column locations enabled. Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

INPUTS	Address Controlled	
	A0	A1
DQ1	0	0
DQ3	1	0
DQ5	0	1
DQ7	1	1

NON-PERSISTENT MASKED BLOCK WRITE

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NON-PERSISTENT MASKED BLOCK WRITE operates exactly like the normal NON-PERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one column location.

Like NON-PERSISTENT MASKED WRITE, the combination of $\overline{ME}/(\overline{WE})$ LOW and DSF LOW when $\overline{CAS}$ goes LOW initiates the NON-PERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the four bit planes can be masked and any combination of the four column locations can be masked.

PERSISTENT MASKED BLOCK WRITE

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF is HIGH when $\overline{CAS}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

LOAD MASK DATA REGISTER

The LOAD MASK DATA REGISTER operation and timing are identical to a normal WRITE cycle except that DSF is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{ME}/(\overline{WE})$, and DSF being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a REGISTER load cycle. DSF is used when $\overline{CAS}$ goes LOW to select the register to be loaded and must be LOW for a LOAD MASK DATA REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of the mask data register will not be changed unless a NON-PERSISTENT MASKED WRITE cycle or a LOAD MASK DATA REGISTER cycle is performed.

The ROW address supplied will be refreshed, but it is not necessary to provide any particular ROW address. The COLUMN address inputs are ignored during a LOAD MASK DATA REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the eight DQ planes.

LOAD COLOR REGISTER

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW then $\overline{RAS}$ goes LOW. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER, and DSF is used to select between NORMAL TRANSFER cycles and SPLIT READ TRANSFER and ALTERNATE WRITE TRANSFER cycles. Each of the TRANSFER cycles available are described below.

READ TRANSFER (DRAM-TO-SAM TRANSFER)

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate the eight 256 bit DRAM rows that are to be tranferred to the eight SAM data registers and the column address bits indicate the start address (or Tap point) of the next serial output cycle from the SAM data registers. To complete the TRANSFER, $\overline{TR}/(\overline{OE})$ is taken HIGH while $\overline{RAS}$ and $\overline{CAS}$ are still LOW. The rising edge of $\overline{TR}/(\overline{OE})$ must occur between the rising edges of successive clocks on the SC input (refer to the AC Timing Diagrams). The 2048 bits of DRAM data are then written into the SAM data registers and the serial shift start address is stored in an internal 8 bit register. If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

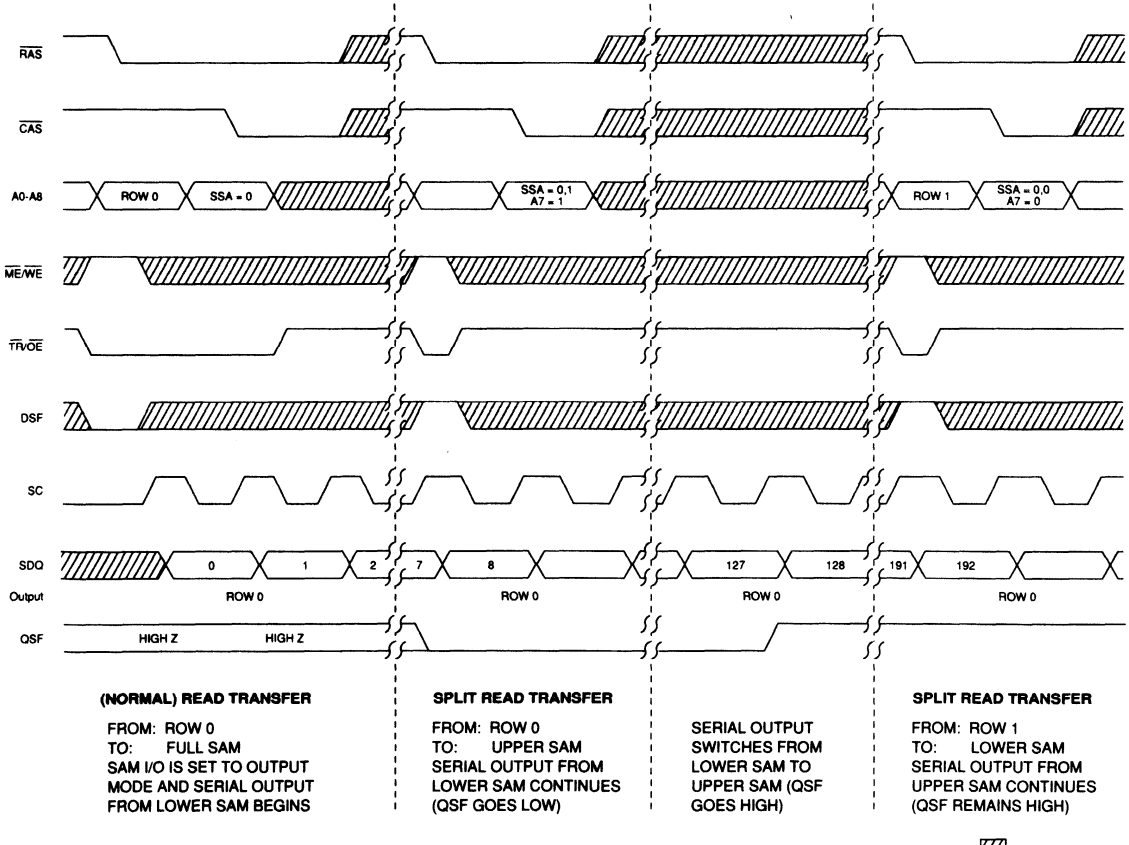


Figure 5
TYPICAL SPLIT READ TRANSFER INITIATION SEQUENCE

SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

The SPLIT READ TRANSFER cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles, the READ TRANSFER cycle had to occur immediately after the last bit of "old data" was clocked out the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data can be transferred to the other half. The transfer can occur at any time while the other half is sending data and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of $\overline{RAS}$ or $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles.

SPLIT TRANSFERS do not change the SAM I/O direction. A normal, or non-split, READ TRANSFER cycle must precede any sequence of SPLIT READ TRANSFER cycles to put the SAM I/O in the output mode and provide a SAM access (which half) reference. Then SPLIT READ TRANSFERS can be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in non-split transfers, the row address is used to specify the DRAM row to be transferred. The most significant column address, A7, is used to select which SAM half accepts the transfer (1=upper half, 0=lower half). The remainder of the column address bits determine the starting address (Tap) for the SAM half selected by A7.

Figure 5 shows a typical SPLIT READ TRANSFER initiation sequence. The normal READ TRANSFER is first performed, followed by a SPLIT READ TRANSFER of the same row to the upper half of the SAM. The purpose of the SPLIT TRANSFER of the same data is to initiate the split SAM operating mode and enable the QSF output. Serial access continues, and when the SAM address counter reaches 128 (A7=1, A0-A6=0) the QSF output goes HIGH. Since the serial access has now switched to the upper SAM, new data can now be transferred to the lower SAM. This sequence of waiting for the state of QSF to change and then transferring new data to the SAM half that is not being accessed can now be repeated. For example, the next step in Figure 5 would be to wait until QSF went LOW (indicateding that row 1 data is shifting out the lower SAM) and then transferring the upper half of row 1 to the upper SAM.

WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the WRITE TRANSFER function is identical to the READ TRANSFER FUNCTION described previously except $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row that the SAM data registers will be written to and the column address (SSA or Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A WRITE TRANSFER does not change the SAM I/O direction.

PSUEDO WRITE TRANSFER (SERIAL INPUT MODE ENABLE)

The PSUEDO WRITE TRANSFER cycle is used to change the direction of SAM port from output to input without performing a WRITE TRANSFER cycle. A PSUEDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the SAM will be ready to accept input data.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the ALTERNATE WRITE TRANSFER is identical to the WRITE TRANSFER except that the DSF pin is taken HIGH, with $(\overline{ME})/\overline{WE}$ LOW, allowing $\overline{SE}$ to be a "don't care." This allows the outputs to be disabled using $\overline{SE}$ during a WRITE TRANSFER cycle.

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE					CAS FALL	A0 - A8[1]		DQ1 - DQ8[2]		REGISTERS	
		CAS	TR/OE	ME/WE	DSF	SE	DSF	RAS	CAS A8-X	RAS	CAS[3]	MASK	COLOR
	DRAM OPERATIONS												
CBR	CAS-BEFORE-RAS REFRESH	0	X	1	X	X	X	—	X	—	X	X	X
ROR	RAS ONLY REFRESH	1	1	X	X	X	—	ROW	—	X	—	X	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	X	0	ROW	COLUMN	X	VALID DATA	X	X
RWNM	NON-PERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	X
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	X	0	ROW	COLUMN	X	VALID DATA	USE	X
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	X	1	ROW	COLUMN (A2 - A7)	X	COLUMN MASK	X	USE
BWNM	NON-PERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	X	1	ROW	COLUMN (A2 - A7)	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASKED REGISTER)	1	1	0	1	X	1	ROW	COLUMN	X	COLUMN	USE	USE
	REGISTER OPERATIONS												
LMR	LOAD MASK REGISTER	1	1	1	1	X	0	ROW[4]	X	X	WRITE MASK	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	X	1	ROW[4]	X	X	COLOR DATA	X	LOAD
	TRANSFER OPERATIONS												
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	X	ROW	SSA[5] (TAP)	X	X	X	X
SRT	SPLIT READ TANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	X	ROW	SSA[5] (TAP)	X	X	X	X
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	X	ROW	SSA[5] (TAP)	X	X	X	X
PWT	PSUEDO WRITE TRANSFER (SERIAL INPUT MODE ENABLE)	1	0	0	0	1	X	ROW[4]	SSA[5] (TAP)	X	X	X	X
AWT	ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	1	X	X	ROW	SSA[5] (TAP)	X	X	X	X

NOTES:
1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
3. On WRITE cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is latched at the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but no particular ROW address is required.
5. SSA = SAM Starting Address or Tap Point. This is the first SAM location that the next SC cycle will access.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V
Operating Temperature, Ta(Ambient) .....0°C to +70°C
Storage Temperature (Ceramic) .....-65°C to +150°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation .....1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(Notes 3, 4, 5) ($0°C \le T_A \le 70°C$, V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts).	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, $0V \le V_{OUT} \le V_{CC}$).	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low voltage (I_{OUT} = 2.5mA)	V_{OL}		0.4	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		5	pF	2
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{ME/WE}$, $\overline{TR/OE}$, SC, $\overline{SE}$, DSF	C_{I2}		7	pF	2
Output Capacitance: DQ, SDQ, QSF	C_O		7	pF	2

CURRENT DRAIN, SAM IN STANDBY

(Notes 2, 3) (0°C ≤ T_A ≤ 70°C, V_{CC} = 5.0V ± 10%)

		MAX					
PARAMETER/CONDITION	**SYMBOL**	**-8**	**-10**	**-12**	**-15**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: T_{RC} = $T_{RC(MIN)}$)	I_{CC1}	90	80	70	70	mA	3, 4
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL} $\overline{CAS}$ = CYCLING; T_{PC} = $T_{PC(MIN)}$)	I_{CC2}	70	60	50	50	mA	
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH} after 8 $\overline{RAS}$ cycles min).	I_{CC3}	5	5	5	5	mA	3
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2).	I_{CC4}	1	1	1	1	mA	3,4
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH}).	I_{CC5}	90	80	60	60	mA	25
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling).	I_{CC6}	80	70	60	60	mA	3
SAM/DRAM DATA TRANSFER	I_{CC7}	90	80	75	75	mA	

CURRENT DRAIN, SAM ACTIVE (tsc = MIN)

(Notes 2, 3) (0°C ≤ T_A ≤ 70°C, V_{CC} = 5.0V ± 10%)

		MAX					
PARAMETER/CONDITION	**SYMBOL**	**-8**	**-10**	**-12**	**-15**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: T_{RC} = $T_{RC(MIN)}$)	I_{CC8}	115	110	100	100	mA	3, 4
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL} $\overline{CAS}$ = CYCLING; T_{PC} = $T_{PC(MIN)}$)	I_{CC9}	95	90	85	85	mA	
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH} after 8 $\overline{RAS}$ cycles min).	I_{CC10}	30	30	30	30	mA	3
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2).	I_{CC11}	25	25	25	25	mA	3,4
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH}).	I_{CC12}	115	110	100	100	mA	25
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling).	I_{CC13}	105	100	95	95	mA	3
SAM/DRAM DATA TRANSFER	I_{CC14}	115	110	100	100	mA	

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	160		190		220		260		ns	
READ-MODIFY-WRITE cycle time	^tRWC	215		220		295		330		ns	
PAGE-MODE READ or WRITE cycle time	^tPC	45		55		70		85		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		30		45	ns	15
Access time from $\overline{TR}$)/$\overline{OE}$	^tOE		20		25		30		45	ns	
Access time from column address	^tAA		40		50		60		70	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		50		60		70	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	80	100,000	100	100,000	120	100,000	150	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		25		35		45		ns	
$\overline{RAS}$ precharge time	^tRP	70		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	35	10,000	45	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	15		15		20		25		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	10		10		15		20		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	25	75	25	90	25	105	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		10		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	12		15		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	17	40	20	50	25	60	25	70	ns	18
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	20		20		25		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		85		95		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		70		ns	
Read command set-up time	^tRCS	0		0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	35	0	35	ns	20
Output Disable	^tOD		20		20		35		35	ns	

DRAM TIMING PARAMETERS (Continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command set-up time	^tWCS	0		0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		30		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		85		90		ns	
Write command pulse width	^tWP	15		20		25		30		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		25		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	22
Data-in hold time	^tDH	20		20		25		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		75		90		100		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	110		130		160		185		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	70		80		100		120		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	55		65		75		85		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		40		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ set-up time	^tWSR	0		0		0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	10		10		10		15		ns	
Mask Data to $\overline{RAS}$ set-up time	^tMS	0		0		0		0		ns	
Mask Data to $\overline{RAS}$ hold time	^tMH	10		15		15		20		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data output (DQ1-DQ8) is high impedance.
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ8) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (min), $^tAWD \geq {}^tAWD$ (min) and $^tCWD \geq {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}/\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}/\overline{WE}$ = LOW and $\overline{TR}/\overline{OE}$=HIGH.
25. SAM output timing is measured with a load equivalent to 2 TTL gate and 30pF.
26. TRANSFER command means that $\overline{TR}/\overline{OE}$ is LOW when $\overline{RAS}$ goes LOW.
27. NON-TRANSFER command means that $\overline{TR}/\overline{OE}$ is HIGH when $\overline{RAS}$ goes LOW.

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 17, 25) (0° C ≤ T_A ≤ + 70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
TRANSFER Command to $\overline{RAS}$ Set Up Time	^tTLS	0		0		0		0		ns	26
Transfer Command to $\overline{RAS}$ Hold Time	^tTLH	10	10,000	10	10,000	10	10,000	15	10,000	ns	
TRANSFER Command to $\overline{RAS}$ Hold Time (REAL-TIME READ TRANSFER only)	^tRTH	70	10,000	80	10,000	90	10,000	100	10,000	ns	26
TRANSFER Command to $\overline{CAS}$ Hold Time (REAL-TIME READ TRANSFER only)	^tCTH	20		25		30		35		ns	26
TRANSFER Command to Column Address Hold Time (For REAL-TIME READ TRANSFER only)	^tATH	25		30		35		40		ns	
TRANSFER Command to SC Lead Time	^tTSL	5		5		5		10		ns	26
TRANSFER Command to $\overline{RAS}$ Lead Time	^tTRL	10		10		10		10		ns	26
TRANSFER Command to $\overline{RAS}$ Delay Time	^tTRD	15		15		15		20		ns	26
TRANSFER Command to $\overline{CAS}$ Time	^tTCL	10		10		10		10		ns	26
TRANSFER Command to $\overline{CAS}$ Delay Time	^tTCD	15		15		15		20		ns	26
First SC edge to TRANSFER Command Delay Time	^tTSD	10		10		10		20		ns	26
Serial Output Buffer Turn Off Delay from $\overline{RAS}$	^tSDZ	10	35	10	40	10	50	10	60	ns	
SC to $\overline{RAS}$ Set Up Time	^tSRS	30		35		40		45		ns	
$\overline{RAS}$ to SC Delay Time	^tSRD	20		25		30		35		ns	
Serial Data Input to $\overline{SE}$ Delay Time	^tSZE	0		0		0		0		ns	
$\overline{RAS}$ to SD Buffer Turn On Time	^tSRO	0		0		0		0		ns	
Serial Data Input Delay from $\overline{RAS}$	^tSDD	45		50		55		60		ns	
Serial Data Input to $\overline{RAS}$ Delay Time	^tSZS	0		0		0		0		ns	
Serial Input Mode Enable ($\overline{SE}$) to $\overline{RAS}$ Set Up Time	^tESR	0		0		0		0		ns	
Serial Input Mode Enable ($\overline{SE}$) to $\overline{RAS}$ Hold Time	^tREH	10		10		10		15		ns	
NON-TRANSFER Command to $\overline{RAS}$ Set Up Time	^tYS	0		0		0		0		ns	27
NON-TRANSFER Command to $\overline{RAS}$ Hold Time	^tYH	10		10		10		10		ns	27
DSF to $\overline{RAS}$ Set Up Time	^tFSR	0		0		0		0		ns	
DSF to $\overline{RAS}$ Hold Time	^tRFH	10		15		15		20		ns	
DSF to $\overline{RAS}$ Hold Time	^tFHR	60		65		70		75		ns	
DSF to $\overline{CAS}$ Set-up Time	^tFSC	0		0		0		0		ns	
DSF to $\overline{CAS}$ Hold Time	^tCFH	15		20		20		25		ns	
SC to QSF Delay Time	^tSQD		25		30		35		40	ns	
SPLIT TRANSFER Set Up Time	^tSTS	30		35		40		45		ns	
SPLIT TRANSFER Hold Time	^tSTH	30		35		40		45		ns	
$\overline{TR/OE}$ to QSF Delay Time	^tTQD		25		30		35		40	ns	
$\overline{CAS}$ to QSF Delay Time	^tCQD		35		40		45		50	ns	

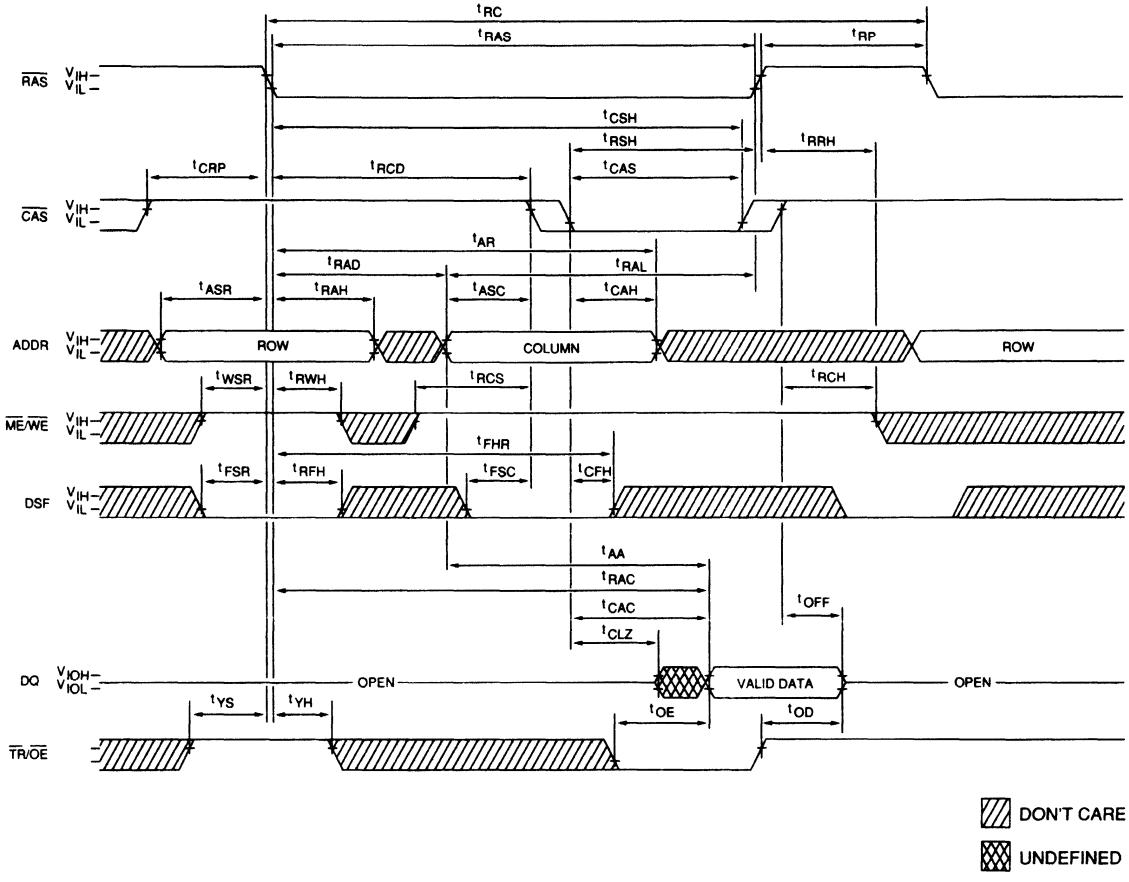
SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 17, 25) (0° C ≤ T_A ≤ + 70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial Clock Cycle Time	^tSC	25		30		35		40		ns	
Access Time from SC	^tSAC		25		30		35		40	ns	
SC Precharge Time (SC Low Time)	^tSP	10		10		12		15		ns	
SC Pulse Width (SC High Time)	^tSAS	10		10		12		15		ns	
Access Time from $\overline{SE}$	^tSEA		20		25		30		40	ns	
$\overline{SE}$ Precharge Time	^tSEP	15		15		15		20		ns	
$\overline{SE}$ Pulse Width	^tSE	15		15		15		20		ns	
Serial Data Out Hold Time after SC High	^tSOH	5		10		10		10		ns	
Serial Output Buffer Turn Off Delay from $\overline{SE}$	^tSEZ	0	15	0	15	0	25	0	30	ns	
Serial Data in Set Up Time	^tSDS	0		0		0		0		ns	
Serial Data in Hold Time	^tSDH	20		20		20		25			
SERIAL INPUT (Write) Enable Set Up Time	^tSWS	0		0		0		0		ns	
SERIAL INPUT (Write) Enable Hold Time	^tSWH	25		30		35		45		ns	
SERIAL INPUT (Write) Disable Set Up Time	^tSWIS	0		0		0		0		ns	
SERIAL INPUT (Write) Disable Hold Time	^tSWIH	25		30		35		45		ns	

DRAM READ CYCLE

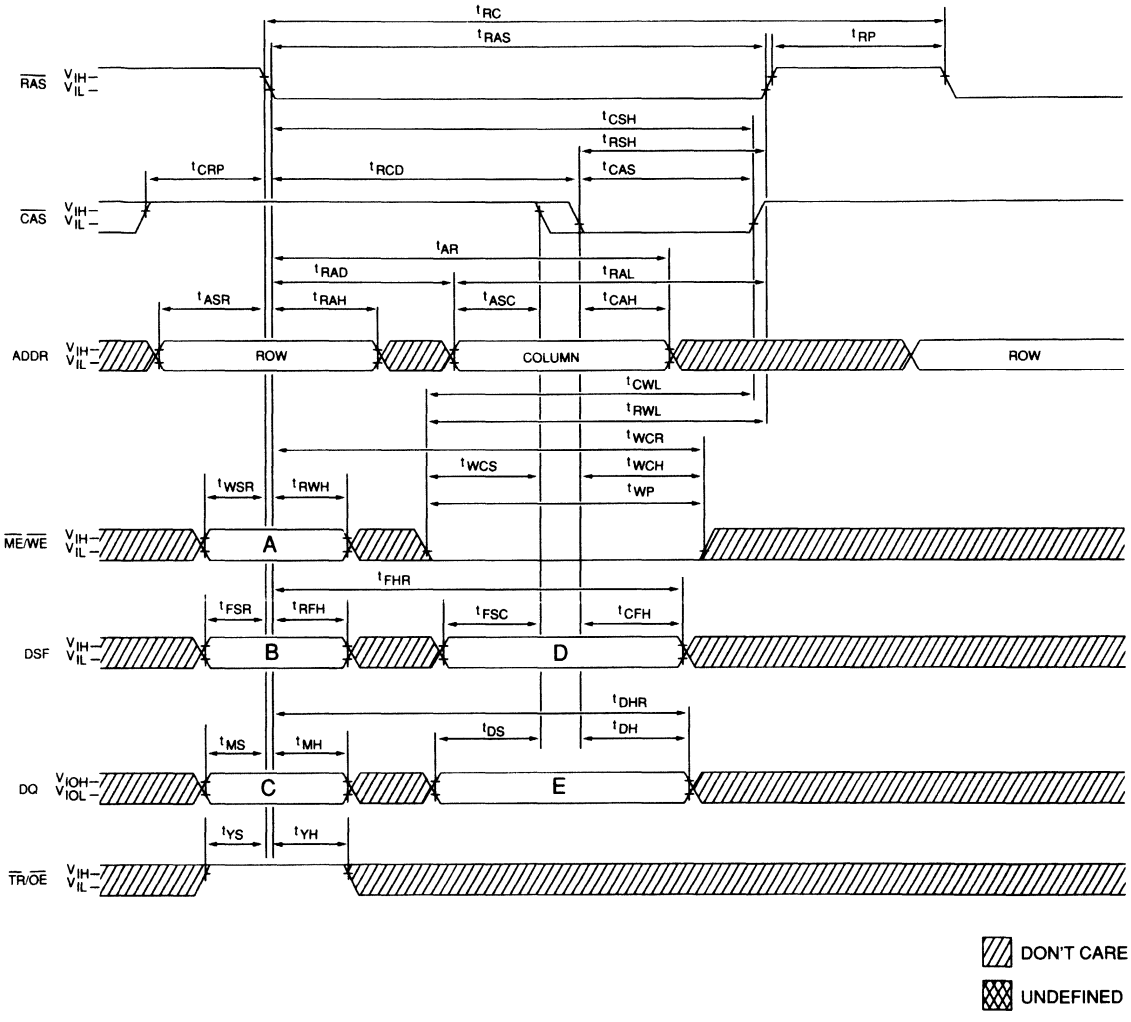


WRITE CYCLE FUNCTION TABLE

LOGIC STATES					FUNCTION
RAS Falling Edge			CAS Falling Edge		
A ME/WE	B DSF	C DQ (Input)	D DSF	E DQ (Input)	
1	0	X	0	DRAM Data	Normal DRAM WRITE (or READ)
0	0	Write Mask	0	DRAM Data (Masked)	Non-Persistent (Load and Use) Masked Write to DRAM
0	1	X	0	DRAM Data (Masked)	Persistent (Use Register) Masked Write to DRAM
1	0	X	1	Column Mask	Block Write to DRAM (No Data Mask)
0	0	Write Mask	1	Column Mask	Non-Persistent (Load and Use) Masked Block Write to DRAM
0	1	X	1	Column Mask	Persistent (Use Register) Masked Block Write to DRAM
1	1	X	0	Write Mask	Load Mask Data Register
1	1	X	1	Color Data	Load Color Register

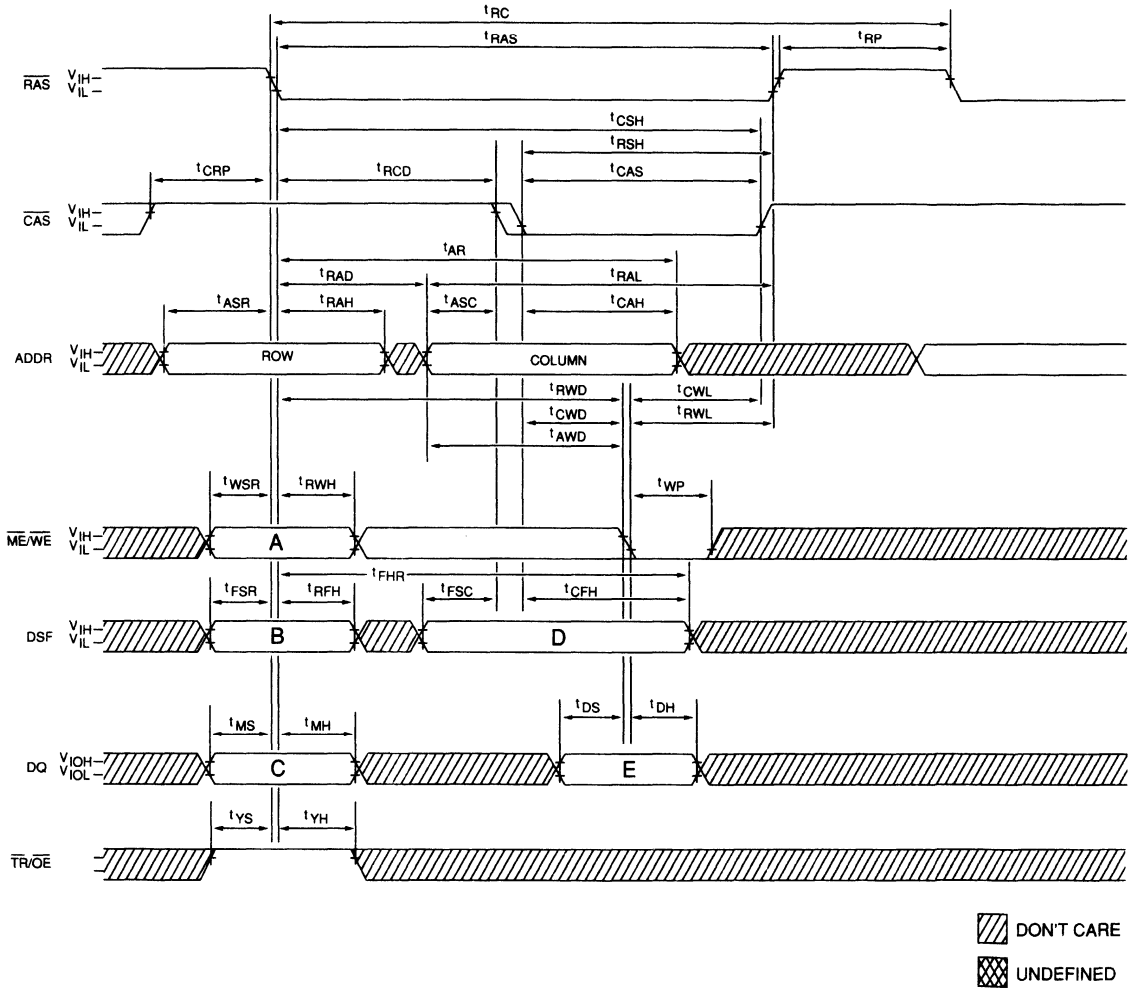
NOTE: Refer to this function table to determine the logic states of A, B, C, D, and E for the WRITE cycle timing diagrams on the following pages.

DRAM EARLY-WRITE CYCLE



NOTE: The Logic states of "A", "B", "C", "D", and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

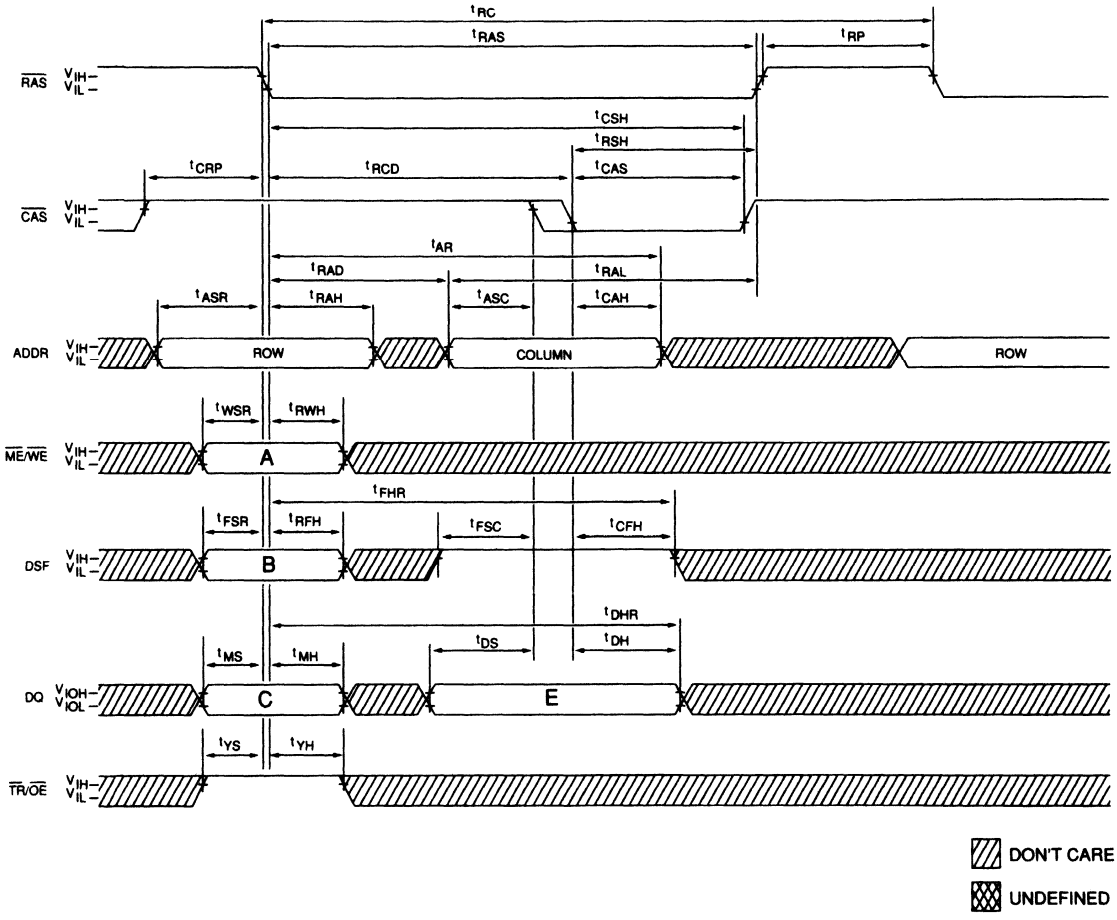
DRAM LATE-WRITE CYCLE



NOTE 1: The Logic states of "A", "B", "C", "D", and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

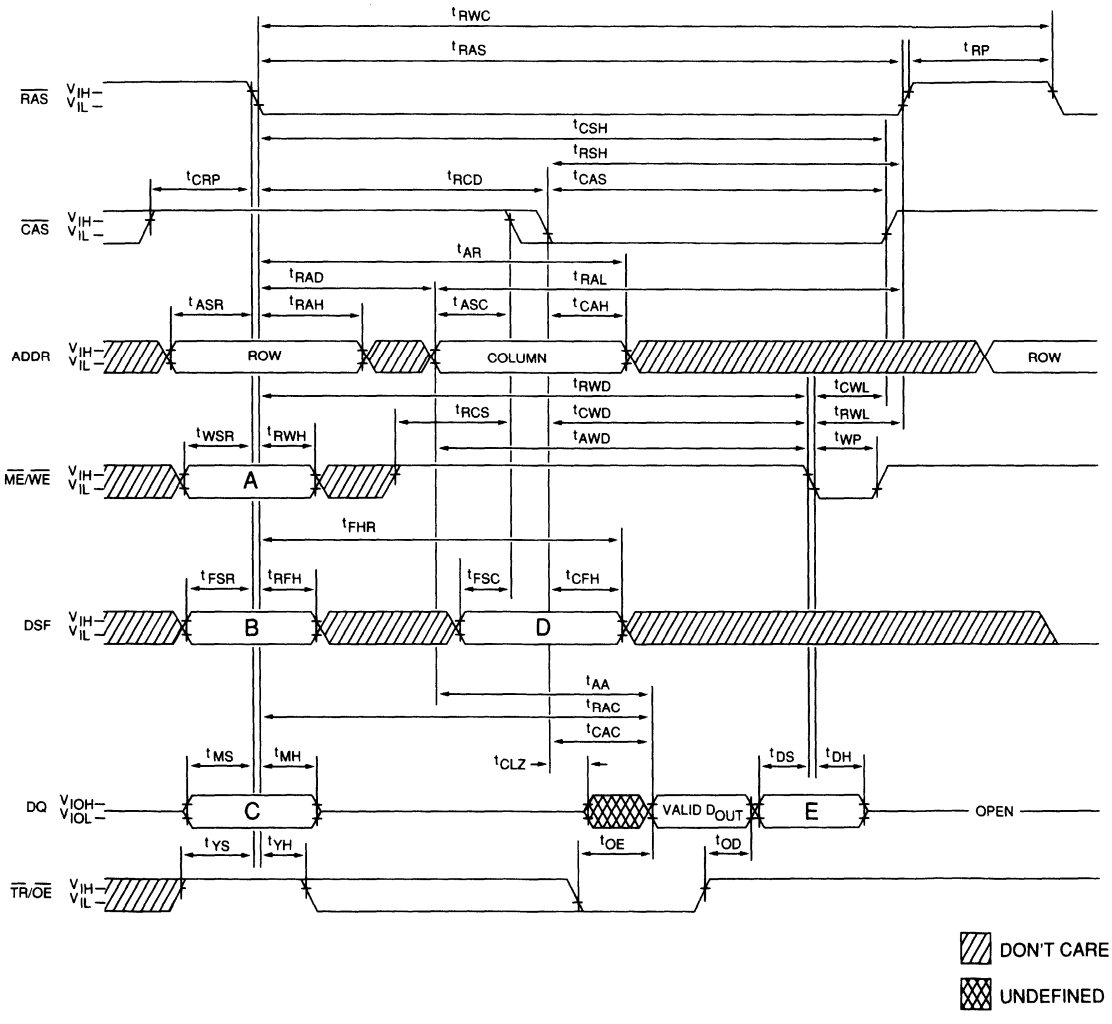
NOTE 2: The Column Mask data for a BLOCK WRITE cycle must be valid at the falling edge of $\overline{CAS}$, regardless of the level of $\overline{ME}/\overline{WE}$. See the BLOCK WRITE cycle timing diagram.

DRAM BLOCK-WRITE CYCLE



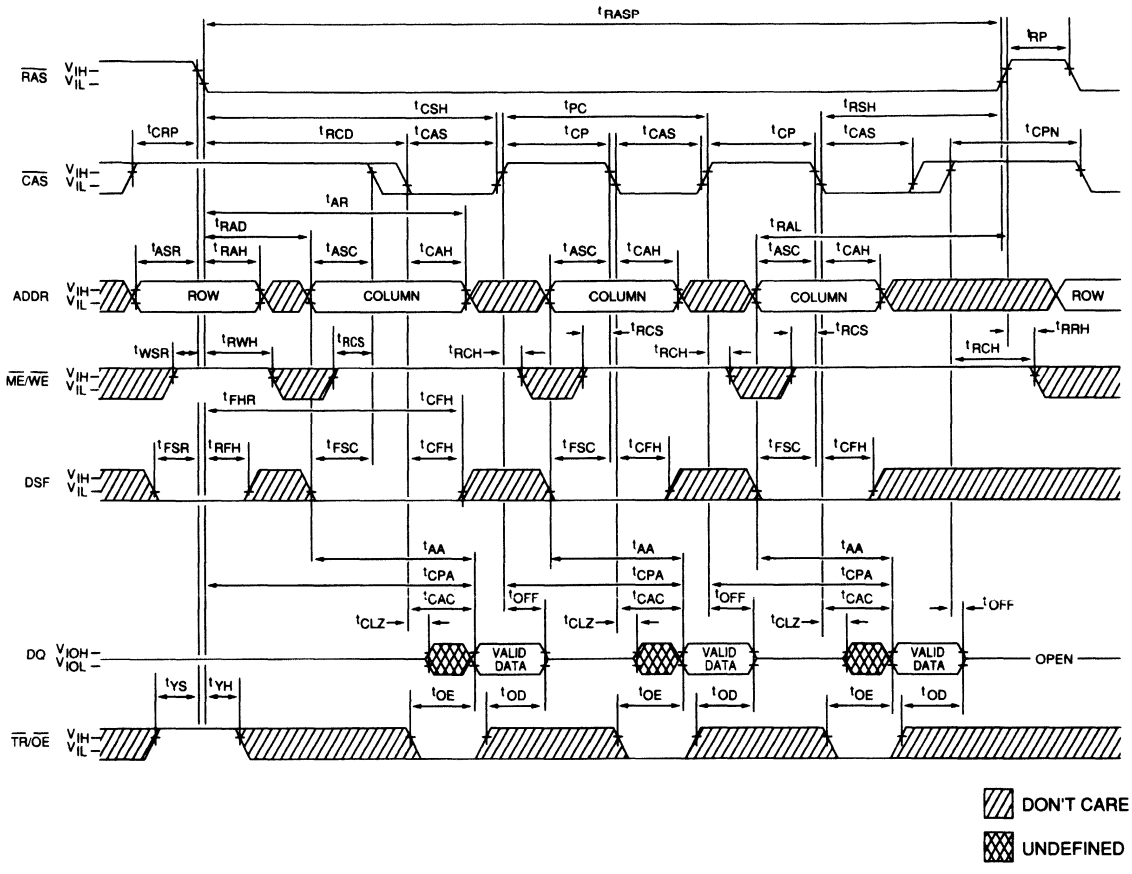
NOTE: The Logic states of "A", "B", "C", and "E" determine the type of BLOCK WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



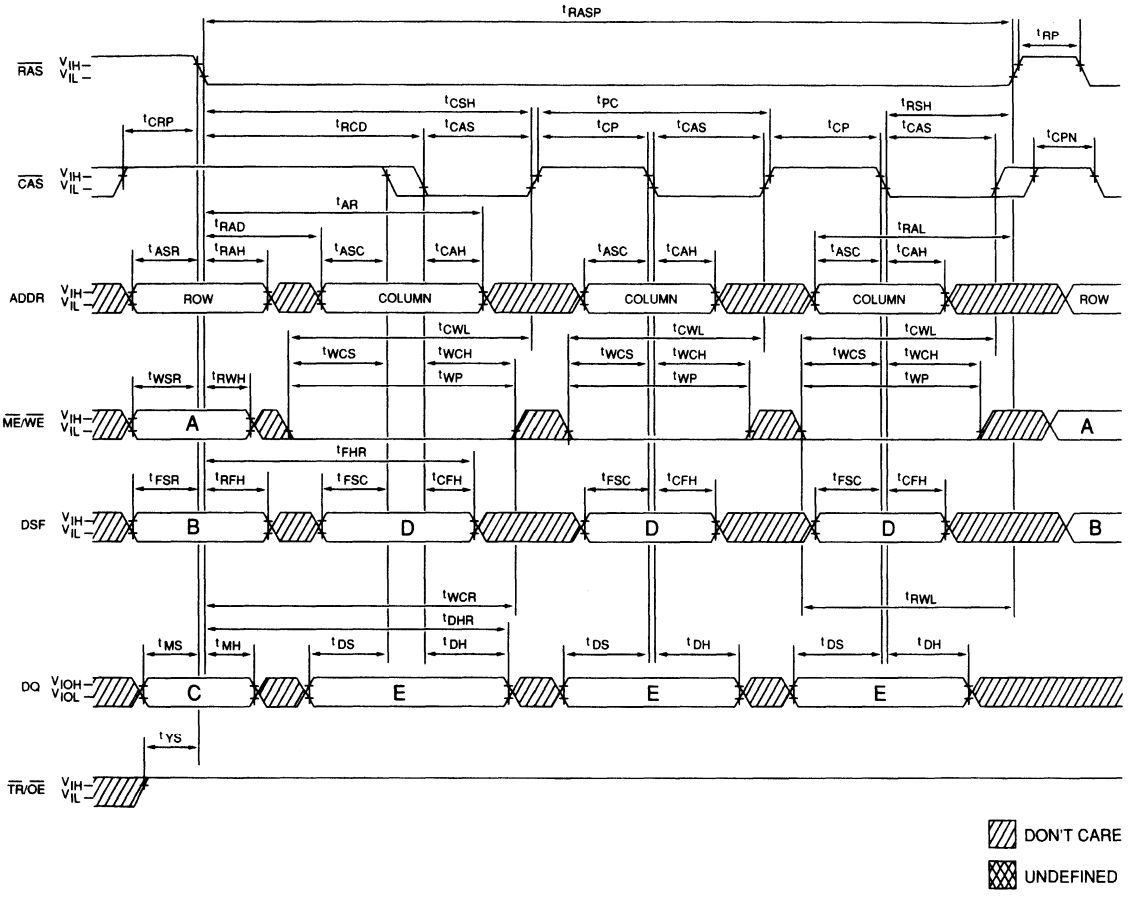
NOTE: The Logic states of "A", "B", "C", "D", and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM PAGE-MODE READ CYCLE



NOTE: WRITE cycles or READ-MODIFY-WRITE cycles can be mixed with READ cycles while in PAGE-MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.

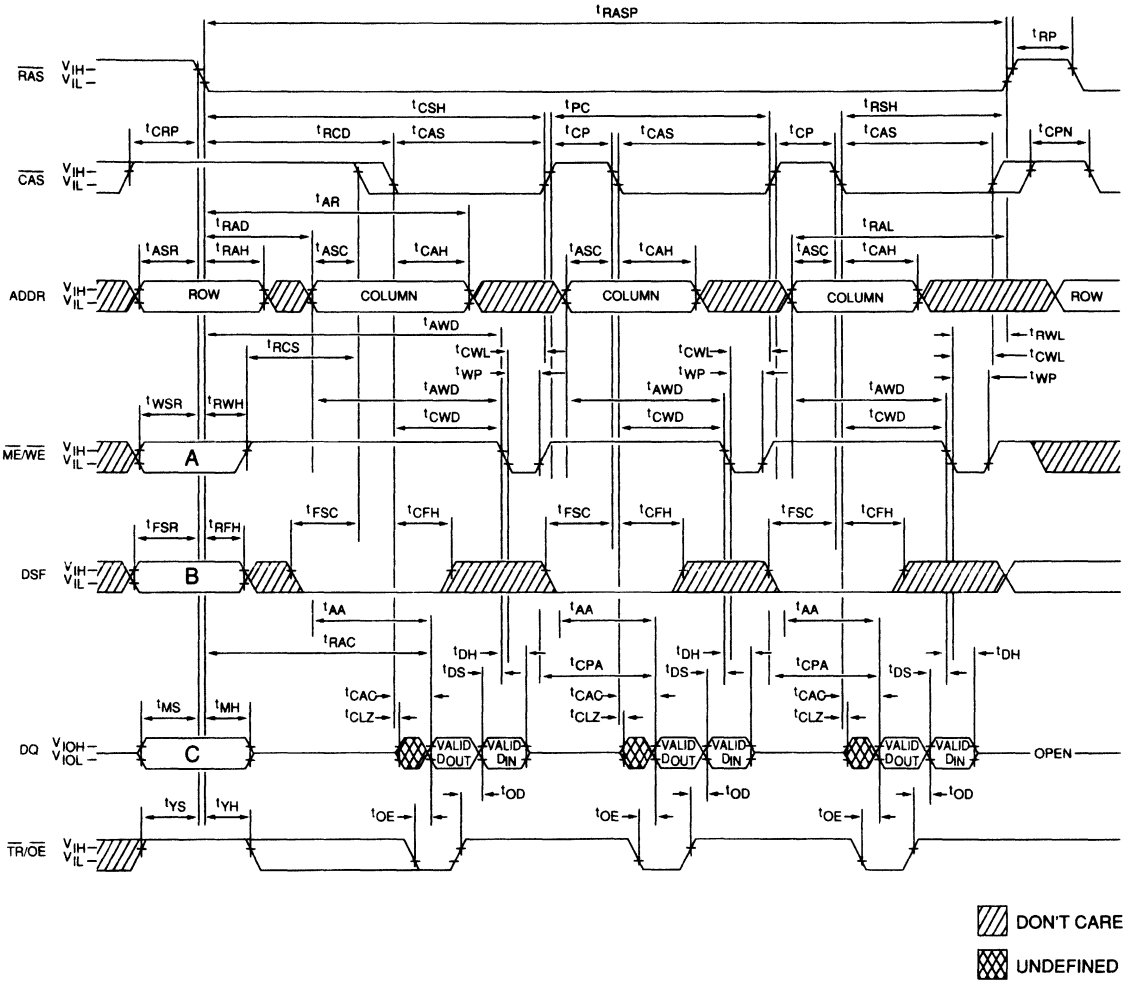
DRAM PAGE-MODE EARLY-WRITE CYCLE



NOTE 1: READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in PAGE-MODE.

NOTE 2: The Logic states of "A", "B", "C", "D", and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

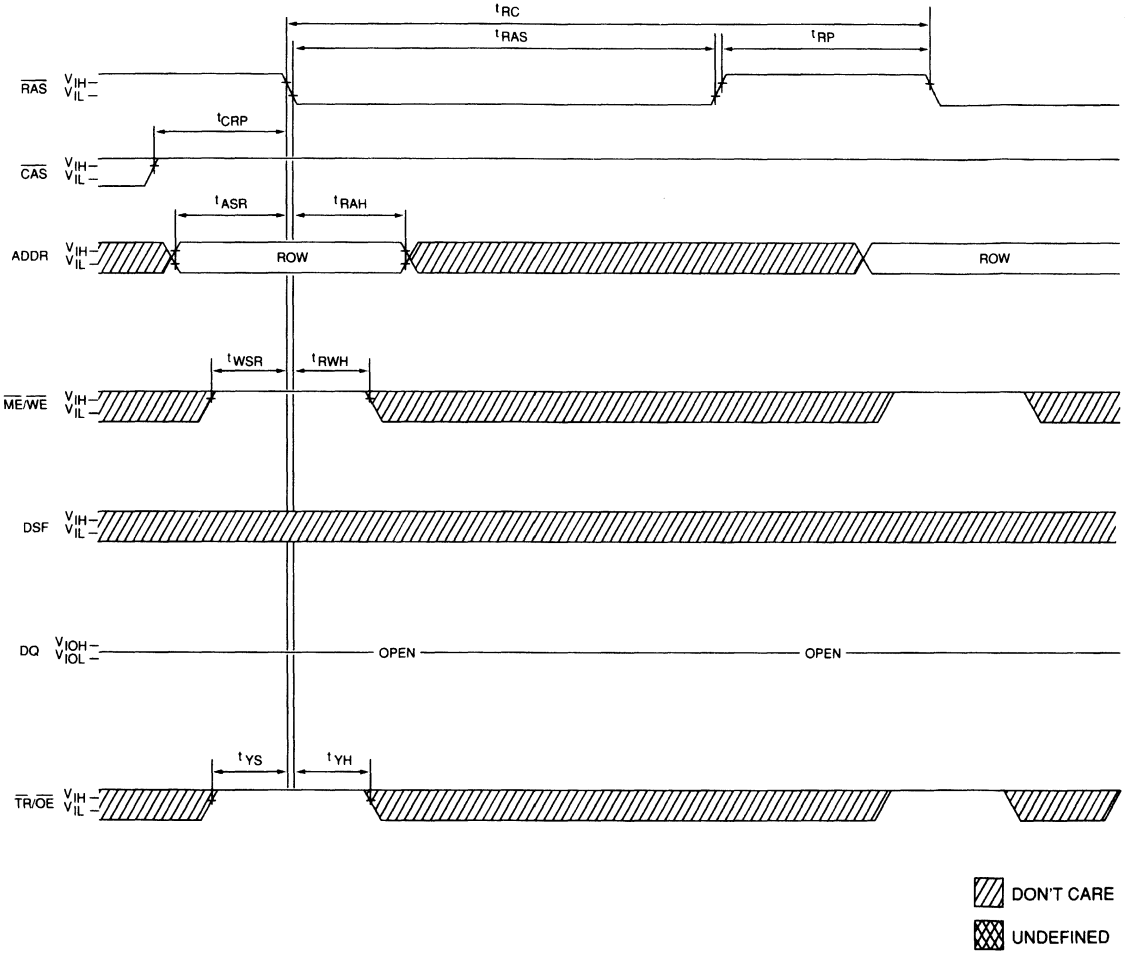
DRAM PAGE-MODE READ-WRITE CYCLE
(PAGE-MODE READ-MODIFY-WRITE CYCLE)



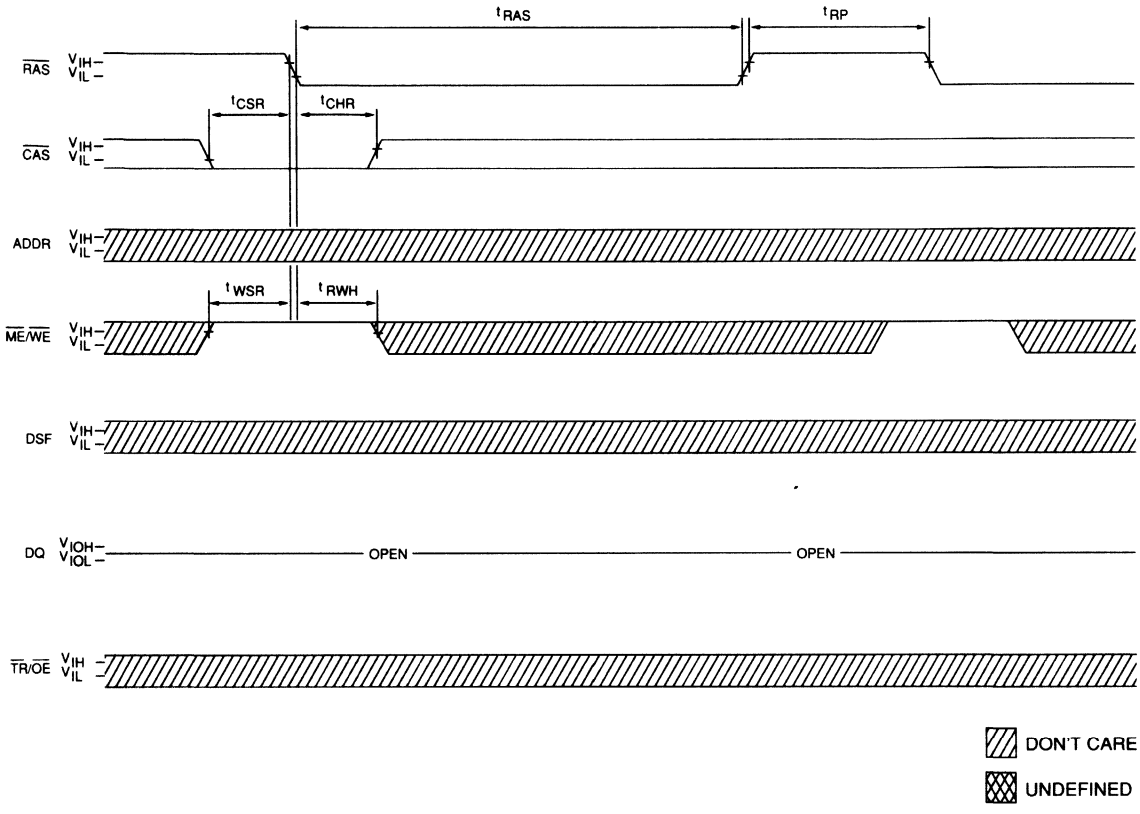
NOTE 1: READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in PAGE-MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.

NOTE 2: The Logic states of "A", "B" and "C" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

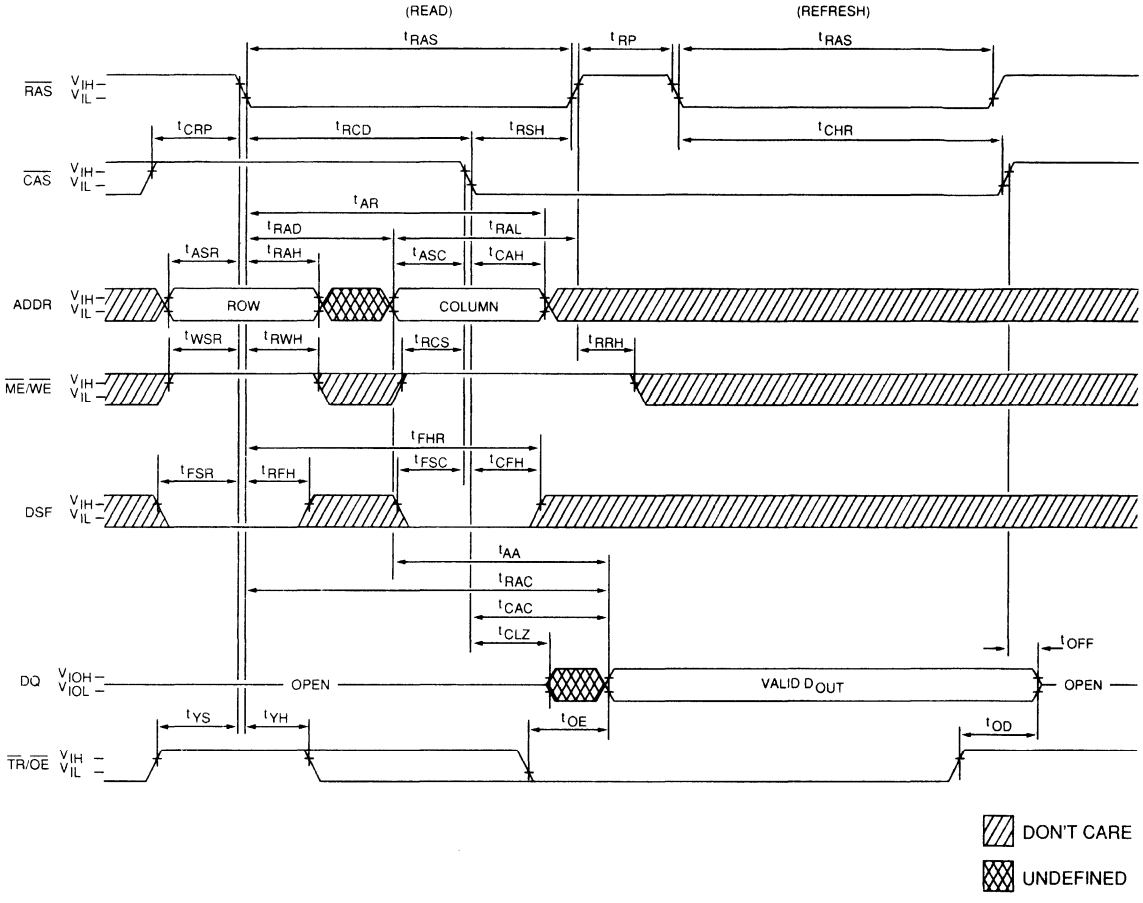
DRAM $\overline{RAS}$ ONLY REFRESH CYCLE
(ADDR = A0-A8)



CAS-BEFORE-RAS REFRESH CYCLE



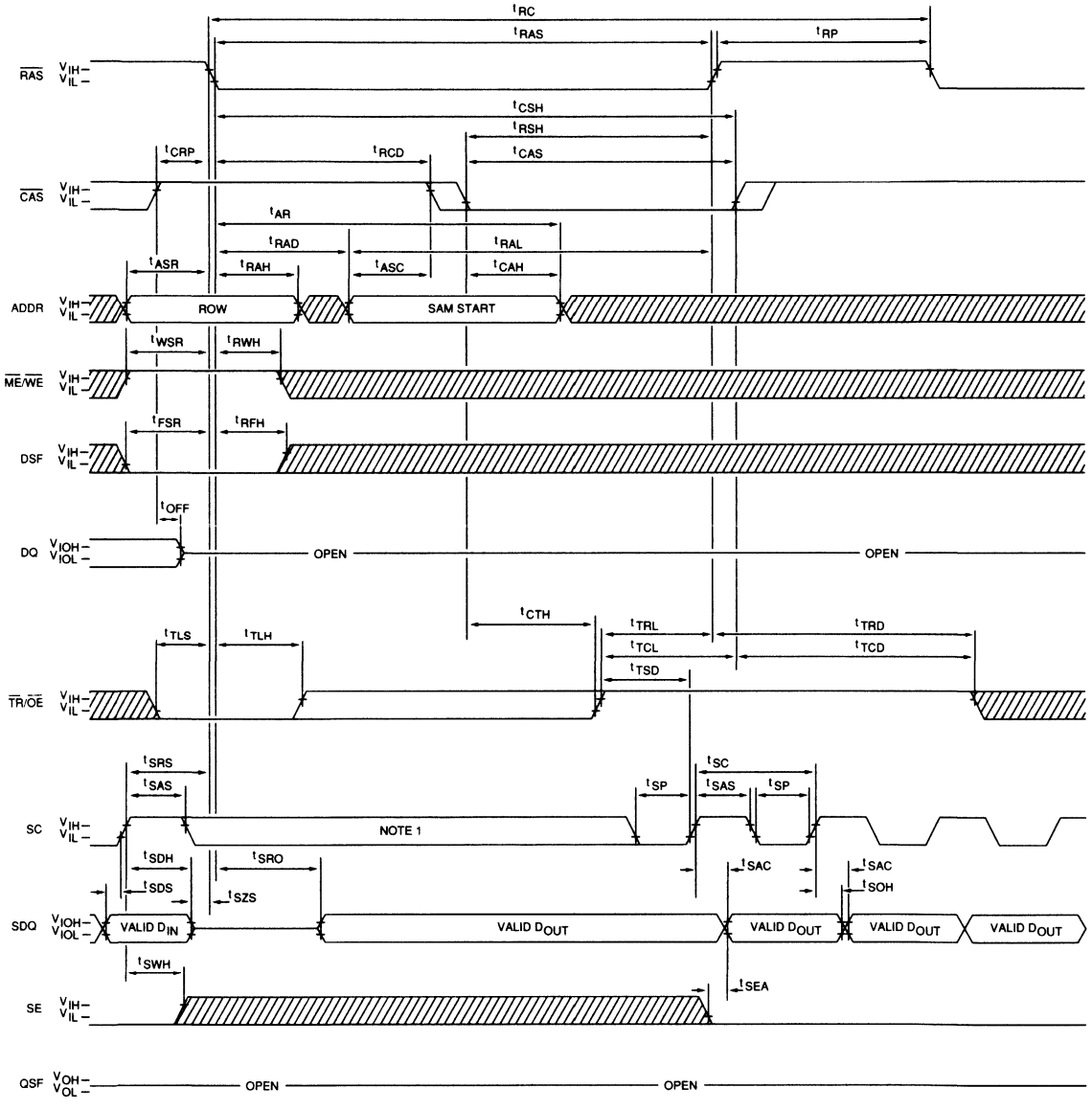
DRAM HIDDEN REFRESH CYCLE



NOTE: A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH.

READ TRANSFER
(DRAM-TO-SAM TRANSFER)

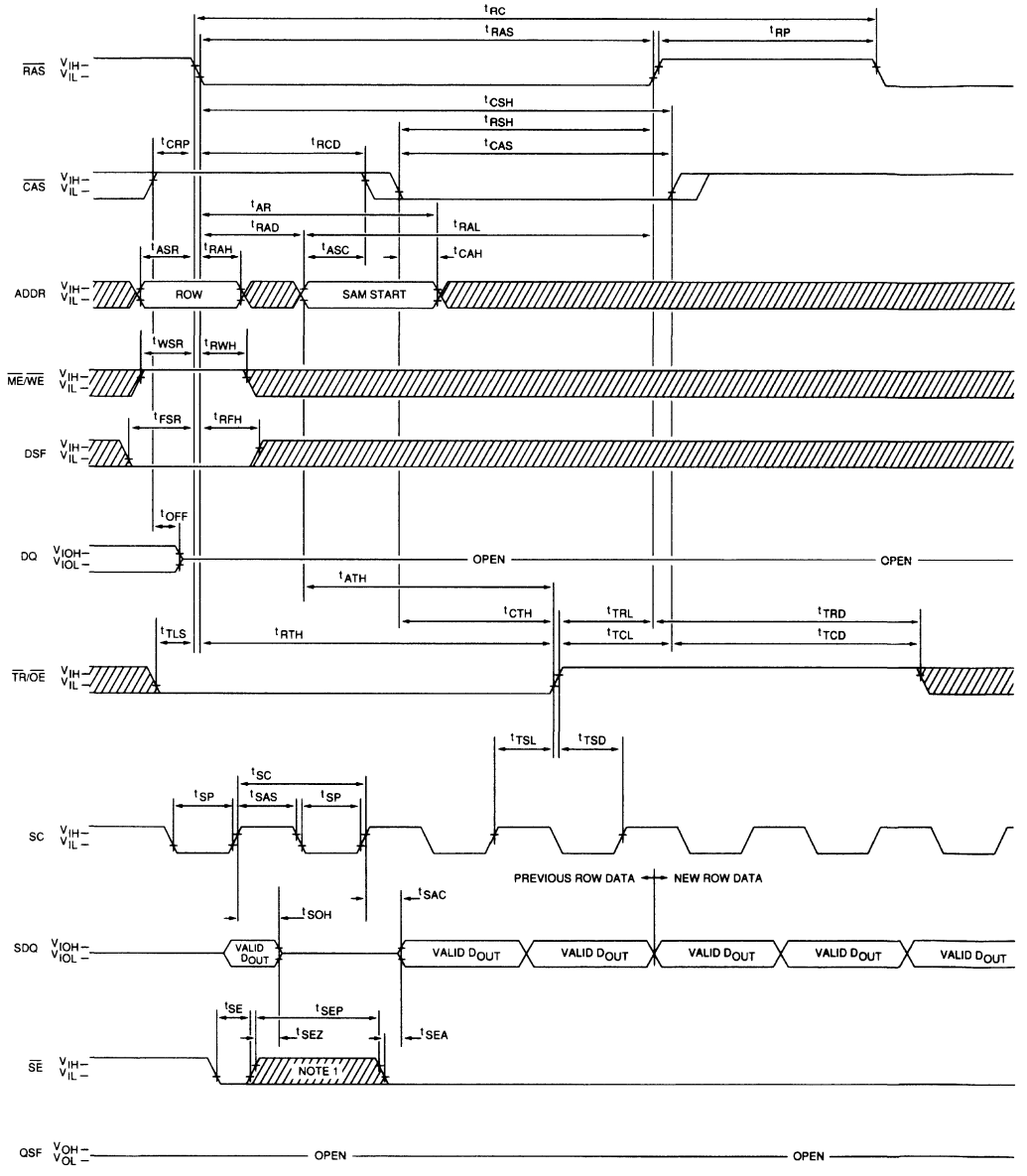
(When part was previously in the SERIAL INPUT mode.)



NOTE 1: There must be no rising edges on the SC input during this time period.

REAL-TIME READ TRANSFER (DRAM-TO-SAM TRANSFER)

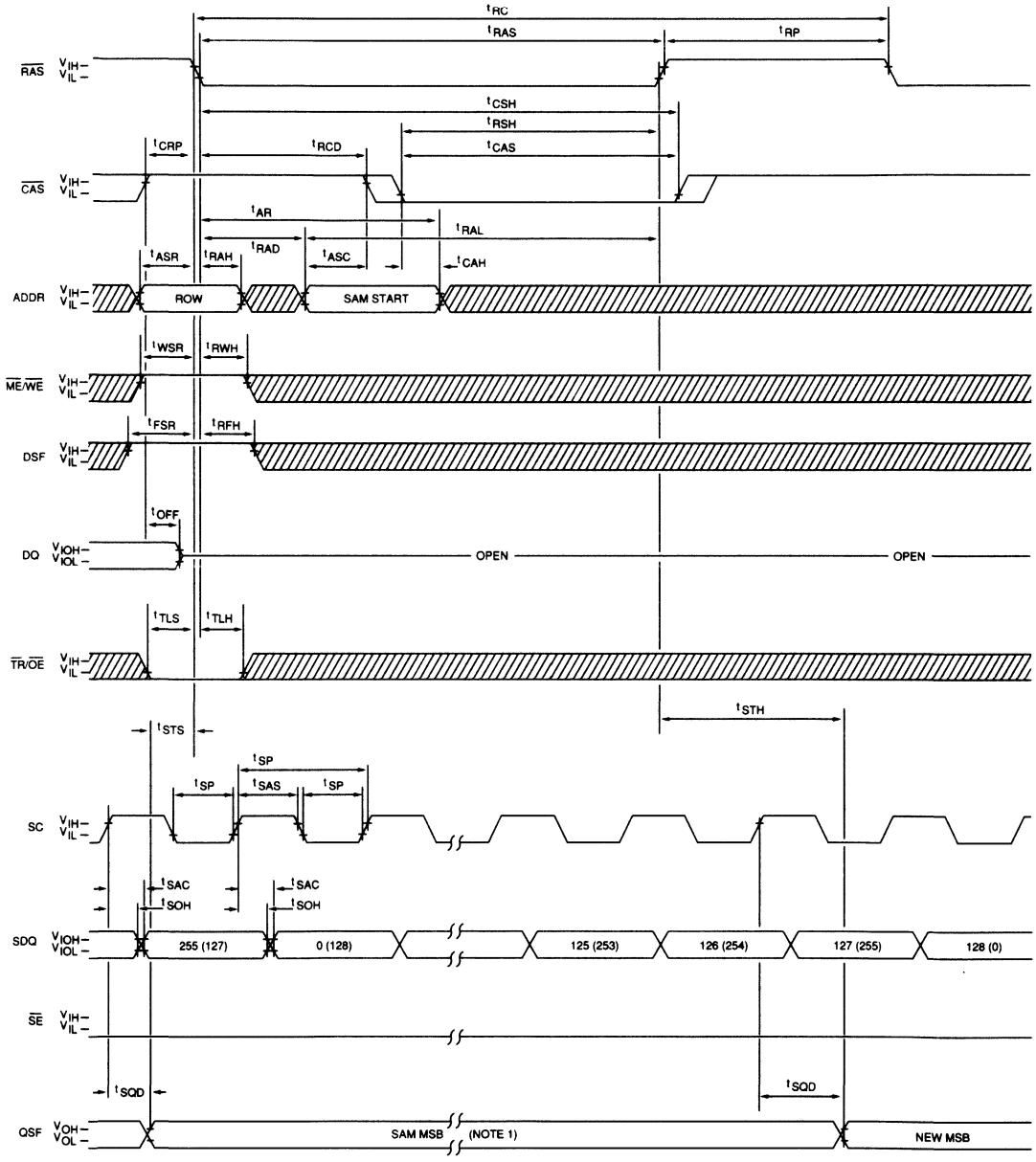
(When part was previously in the SERIAL OUTPUT mode.)



NOTE 1: The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.

DON'T CARE
UNDEFINED

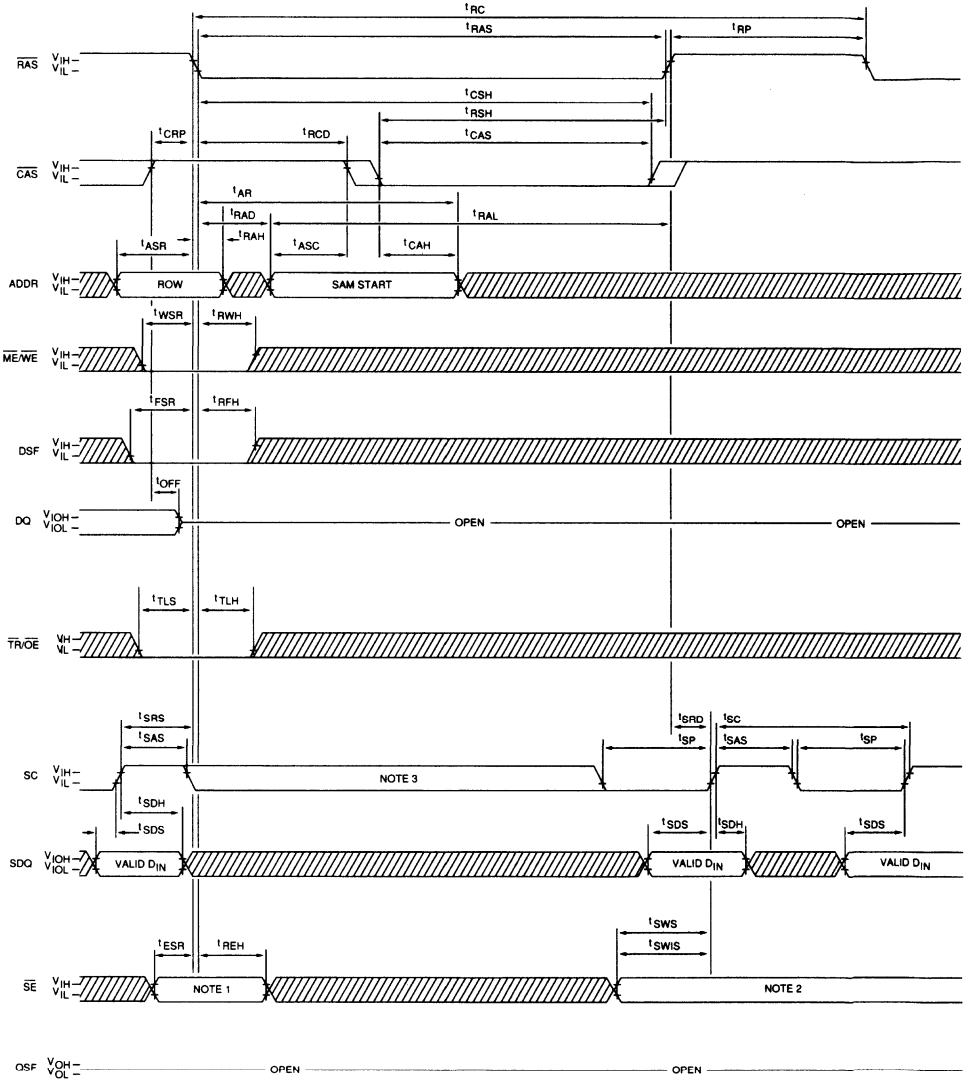
SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE 1: QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)

(When part was previously in the SERIAL INPUT mode.)



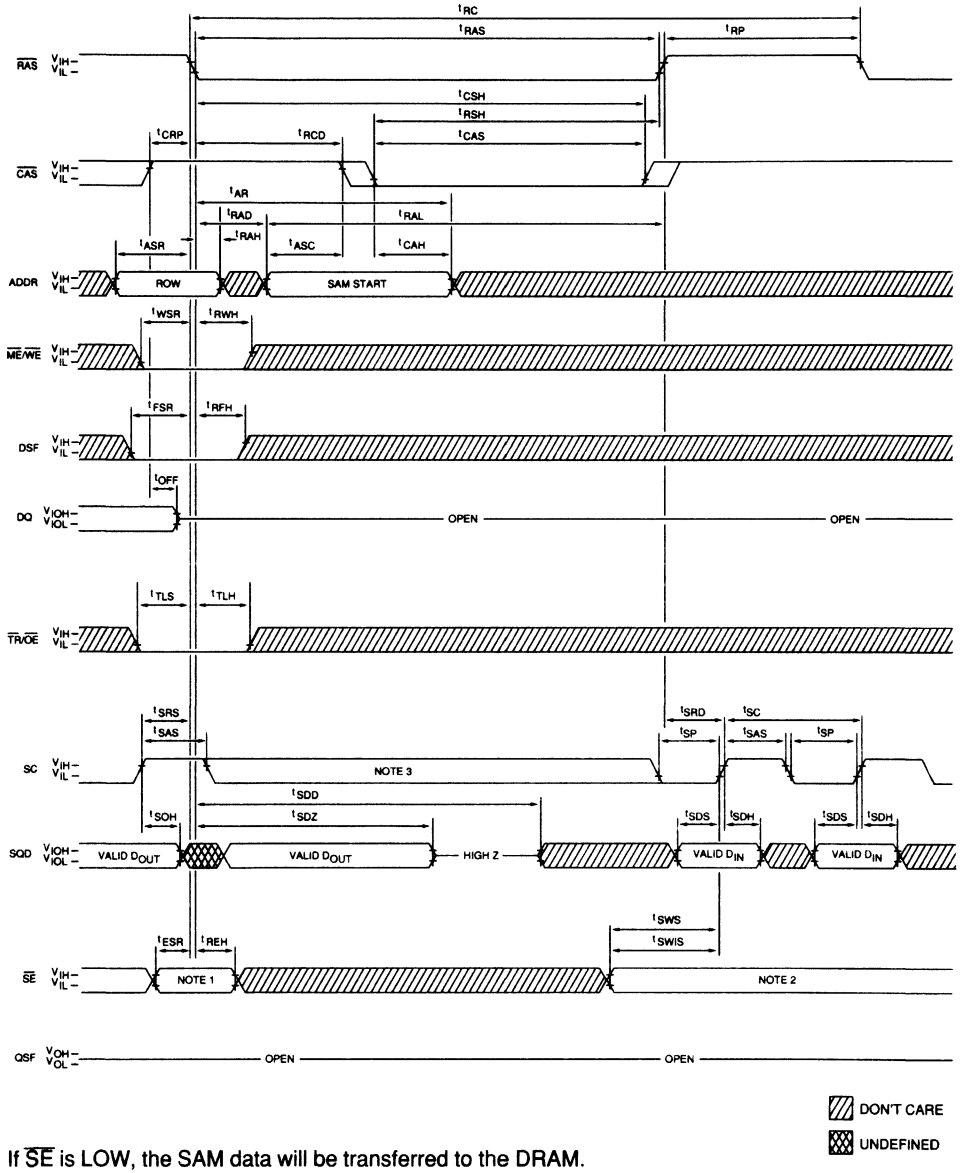
NOTE 1: If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

NOTE 2: $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.

NOTE 3: There must be no rising edges on the SC input during this time period.

WRITE TRANSFER and PSEUDO WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode.)

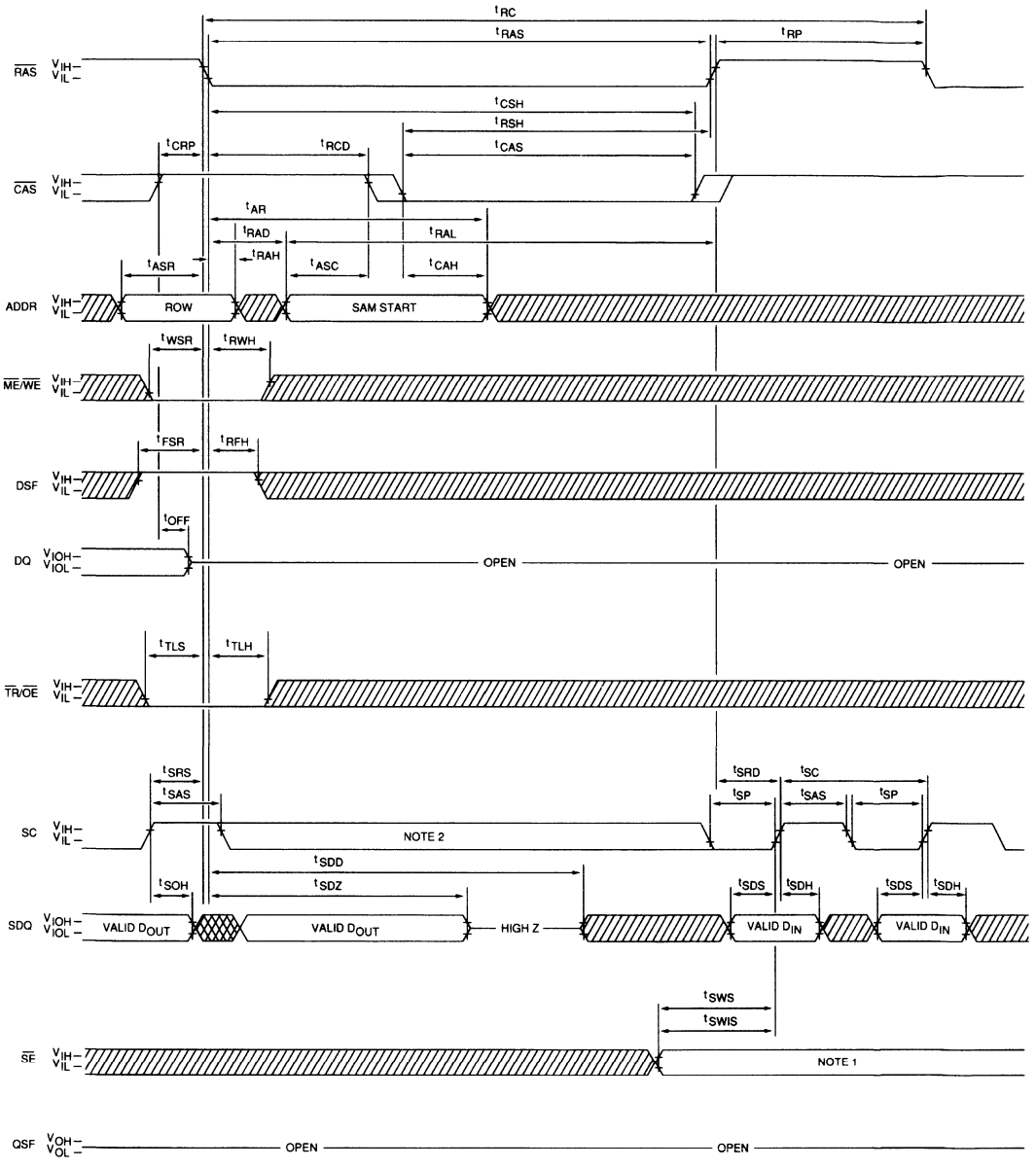


NOTE 1: If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

NOTE 2: $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.

NOTE 3: There must be no rising edges on the SC input during this time period.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)



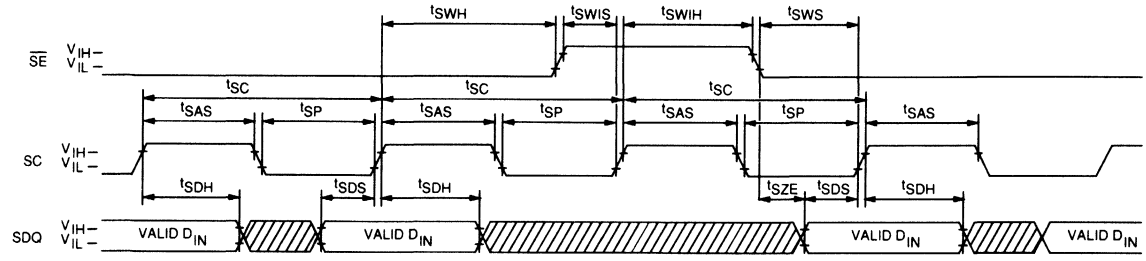
NOTE 1: $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.

NOTE 2: There must be no rising edges on the SC input during this time period.

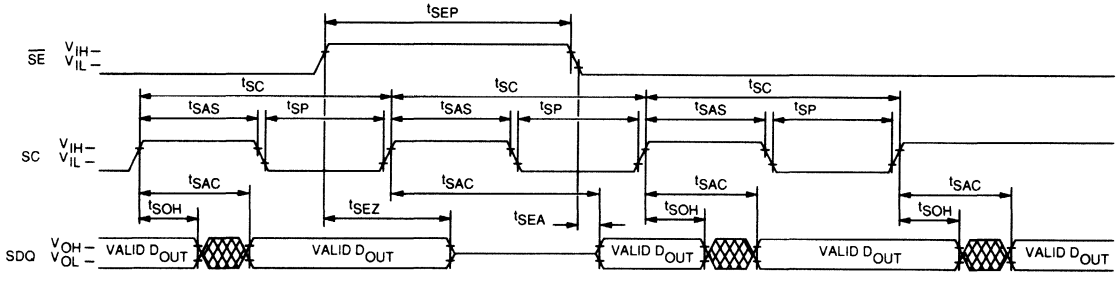
DON'T CARE

UNDEFINED

SAM SERIAL INPUT



SAM SERIAL OUTPUT



DON'T CARE

UNDEFINED

VRAM

256K x 4 DRAM with 512 x 4 SAM

FEATURES

- Industry standard pin-out, timing and functions
- High performance CMOS silicon gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 512 cycle refresh within 8ms
- Optional FAST PAGE MODE access cycles
- Dual port organization: 256K x 4 DRAM port
  512 x 4 SAM port
- No refresh required for Serial Access Memory
- Low power: 5mW standby; 200mW active, typical
- Fast access times – 80ns random, 25ns serial

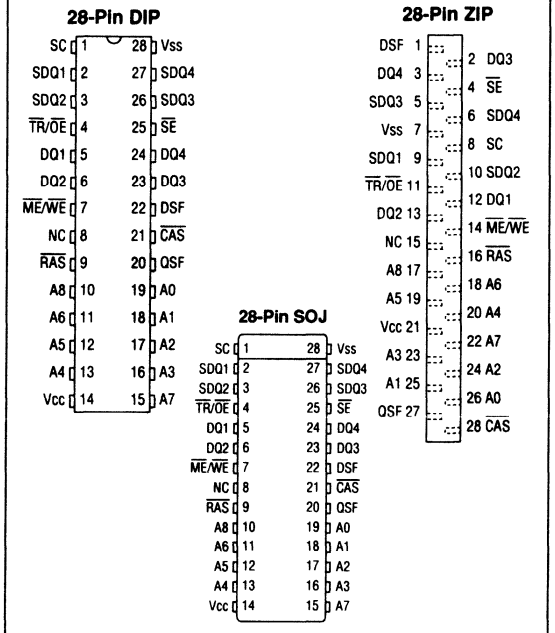
SPECIAL FUNCTIONS

- JEDEC Standard Function set
- PERSISTENT MASK WRITE
- SPLIT READ TRANSFER
- ALTERNATE WRITE TRANSFER
- BLOCK WRITE

OPTIONS / MARKING

OPTIONS	MARKING
• Timing (DRAM, SAM)	
80ns, 25ns	-8
100ns, 30ns	-10
120ns, 35ns	-12
150ns, 40ns	-15

PIN ASSIGNMENT (Top View)



GENERAL DESCRIPTION

The MT42C4256 is a high speed, dual port CMOS dynamic random access memory (DPDRAM) containing 1,048,576 bits. They can be accessed either by a four bit wide DRAM port or by a 512 x 4 bit serial access memory (SAM) port. Data can be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the DPDRAM is functionally identical to the MT4C4256 (256K x 4) bit DRAM. Four 512 bit data registers make up the serial access memory portion of the DPDRAM. Data I/O and internal data transfer is accomplished using three separate bidirectional data paths; the four bit random access I/O port, the four internal 512 bit wide paths between the DRAM and the SAM, and the four bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the DPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the DPDRAM is fully static and does not require any refresh.

The operation and control of the MT42C4256 is compatible with (and can be identical to) the operation of the MT42C4064 (64Kx4) Video RAM. However, the MT42C4256 offers several additional functions which may be used to increase system performance or ease critical timing requirements. These "special functions" are described in detail in the following section.

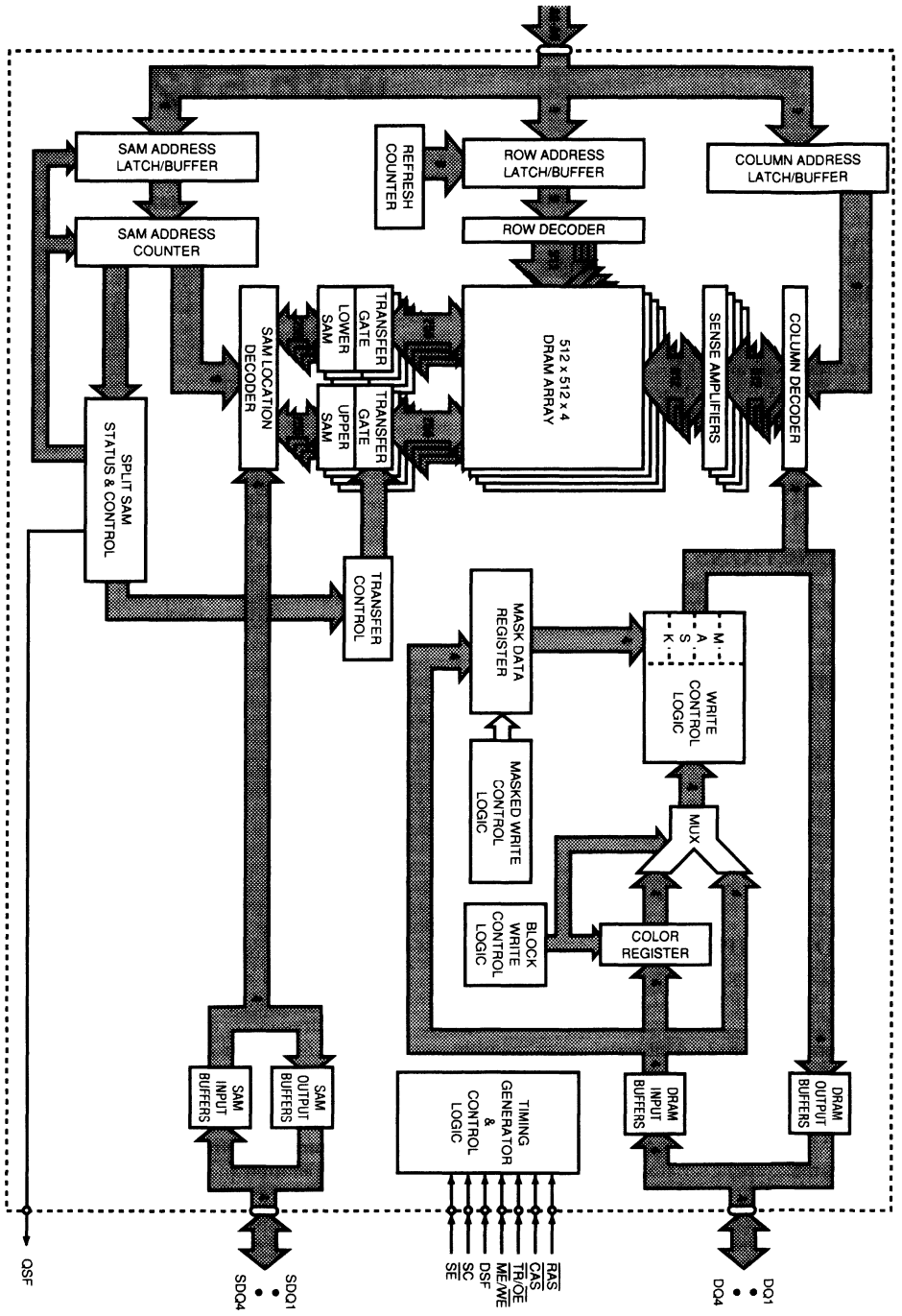


Figure 1
MT42C4256 BLOCK DIAGRAM

PIN DESCRIPTIONS

DIP/SOJ PIN NUMBER(S)	ZIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
1	8	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
4	11	$\overline{TR/OE}$	Input	Transfer Enable: Enables an internal TRANSFER operation at $\overline{RAS}$ (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after $\overline{RAS}$ goes LOW ($\overline{CAS}$ must also be LOW), otherwise the output buffers are in a high impedance state.
7	14	$\overline{ME/WE}$	Input	Mask Enable: If $\overline{ME/WE}$ is LOW at the falling edge of $\overline{RAS}$ a MASKED WRITE cycle is performed, or Write Enable: $\overline{ME/WE}$ is also used to select a READ ($\overline{ME/WE}$ = H) or WRITE ($\overline{ME/WE}$ = L) cycle when accessing the DRAM. This includes a READ TRANSFER ($\overline{ME/WE}$ = H) or WRITE TRANSFER ($\overline{ME/WE}$ = L).
25	4	$\overline{SE}$	Input	Serial Port Enable: $\overline{SE}$ enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a high impedance state. $\overline{SE}$ is also used during a WRITE TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
22	1	DSF	Input	Special Function Select: DSF is used to indicate which special functions (Block Write, Masked Write vs. Persistent Masked Write, etc.) are used on a particular access cycle.
9	16	$\overline{RAS}$	Input	Row Address Strobe: $\overline{RAS}$ is used to clock in the 9 Row address bits and as a strobe for the $\overline{ME/WE}$, $\overline{TR/OE}$, DSF, and DQ inputs.
21	28	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock in the 9 column address bits, enable the DRAM output buffers (along with $\overline{TR/OE}$), and as a strobe for the DSF input.
19, 18, 17, 16, 13, 12, 11, 15, 10	26, 25, 24, 23, 20, 19, 18, 22, 17	A0 to A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select 4 bits out of the 256K x 4 available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when $\overline{RAS}$ goes LOW) and the SAM start address (when $\overline{CAS}$ goes LOW).
5, 6, 23, 24	12, 13, 2, 3	DQ1 - DQ4	Input/ Output	DRAM Data I/O inputs for MASK DATA REGISTER and COLOR REGISTER load cycles, and ADDRESS MASK inputs for BLOCK WRITE.
2, 3, 26, 27	9, 10, 5, 6	SDQ1 - SDQ4	Input/ Output	Serial Data I/O: Input, Output, or high impedance.
20	27	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed when the Split SAM Transfer mode is being used.
8	15	NC	–	No Connect - This pin should be either left unconnected or tied to ground.
14	21	Vcc	Supply	Power Supply: +5 Volts ±10%
28	7	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C4256 can be divided into three functional blocks (see Figure 1); the DRAM, the transfer circuitry, and the serial access memory (SAM). All of the operations described below are also shown in the AC Timing Diagrams section of this data sheet as well as summarized in the Truth Table.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing transfer operations the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$.*

DRAM OPERATION

DRAM REFRESH

Like any DRAM based memory, the MT42C4256 Video RAM must be refreshed to retain data. All 512 row address combinations must be accessed within 8ms. The MT42C4256 supports $\overline{CAS}$-BEFORE-$\overline{RAS}$, $\overline{RAS}$ ONLY and HIDDEN types of refresh cycles.

For the $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh mode, the row addresses are generated and stored in an internal address counter. The user need not supply any address data and simply must perform 512 $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycles within the 8ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for $\overline{RAS}$ ONLY refresh cycles. The DQ I/O pins remain in a high -Z state for both the $\overline{RAS}$ ONLY and $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycles.

HIDDEN refresh cycles are performed by toggling $\overline{RAS}$ (and keeping $\overline{CAS}$ LOW) after a READ or WRITE cycle. This performs $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM portion of the MT42C4256 does not require any refreshing.

DRAM READ AND WRITE CYCLES

The DRAM portion of the DPDRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or "don't care" states for the DRAM are specified for the DPDRAM. These conditions are highlighted in the following discussion. In addition, the DPDRAM has several special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select four memory bits from the 262,144 x 4 available are latched into the chip using the A0-A8, $\overline{RAS}$ and $\overline{CAS}$ inputs. First, the 9 row address bits are set-up on the address inputs and clocked into the part when $\overline{RAS}$ transitions from HIGH to LOW. Next, the 9 column address bits are set-up on the address inputs and clocked in when $\overline{CAS}$ goes from HIGH to LOW.

For single port DRAMS, the $\overline{OE}$ pin is a "don't care" when $\overline{RAS}$ goes LOW. For the DPDRAM, $(\overline{TR})/\overline{OE}$ is used, when $\overline{RAS}$ goes LOW, to select between DRAM and TRANSFER cycles. $(\overline{TR})/\overline{OE}$ must be HIGH at the $\overline{RAS}$ HIGH to LOW transition for all DRAM operations (except $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh).

If $(\overline{ME})/\overline{WE}$ is HIGH when $\overline{CAS}$ goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ4 port. The $(\overline{TR})/\overline{OE}$ input must transition from HIGH to LOW sometime after $\overline{RAS}$ falls to enable the DRAM output port.

For single port normal DRAMs, $\overline{WE}$ is a "don't care" when $\overline{RAS}$ goes LOW. For the DPDRAM, $(\overline{ME})/\overline{WE}$ is used, when $\overline{RAS}$ goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If $(\overline{ME})/\overline{WE}$ is LOW at the $\overline{RAS}$ HIGH to LOW transition, a MASKED WRITE operation is selected. For any DRAM access cycle (READ or WRITE), $(\overline{ME})/\overline{WE}$ must be HIGH at the $\overline{RAS}$ HIGH to LOW transition. If $(\overline{ME})/\overline{WE}$ is LOW when $\overline{CAS}$ goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1-DQ4 data port will be written into the selected memory cells.

The DPDRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, PAGE-MODE READ, PAGE-MODE WRITE, and PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

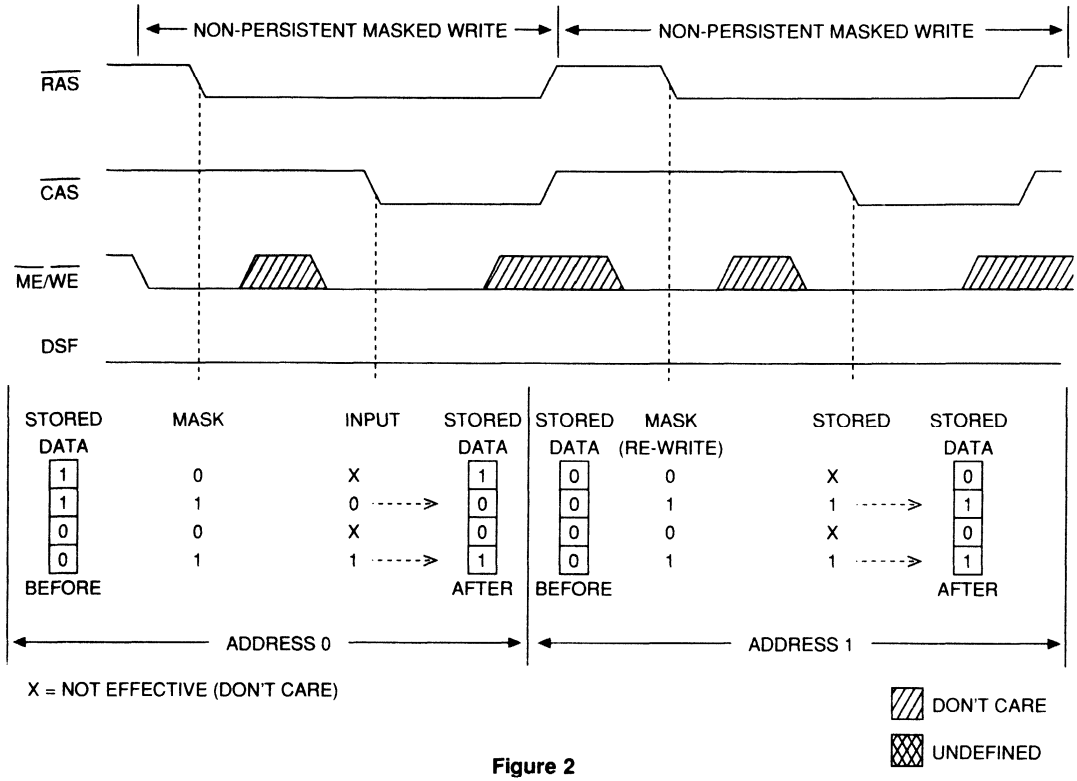


Figure 2
NON-PERSISTENT MASKED WRITE EXAMPLE

NON-PERSISTENT MASKED WRITE

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only certain bits within a four bit word. The MT42C4256 supports two types of MASKED WRITE cycles, NON-PERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}$/($\overline{WE}$) is LOW and DSF is LOW at the $\overline{RAS}$ HIGH to LOW transition, the data (mask data) present on the DQ1-DQ4 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the four DQ1-DQ4 pins. If a LOW (logic 0) is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that $\overline{CAS}$ is still HIGH. When $\overline{CAS}$ goes LOW, the bits present on the DQ1-DQ4 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. When using NON-PERSISTENT MASKED WRITE, the data present on the DQ inputs is loaded into the mask data register at the falling edge of $\overline{RAS}$. FAST PAGE MODE can be used with NON-PERSISTENT MASKED WRITE to write several column locations. The same mask is used during the entire FAST PAGE $\overline{RAS}$ cycle. An example of NON-PERSISTENT MASKED WRITE cycle is shown in Figure 2.

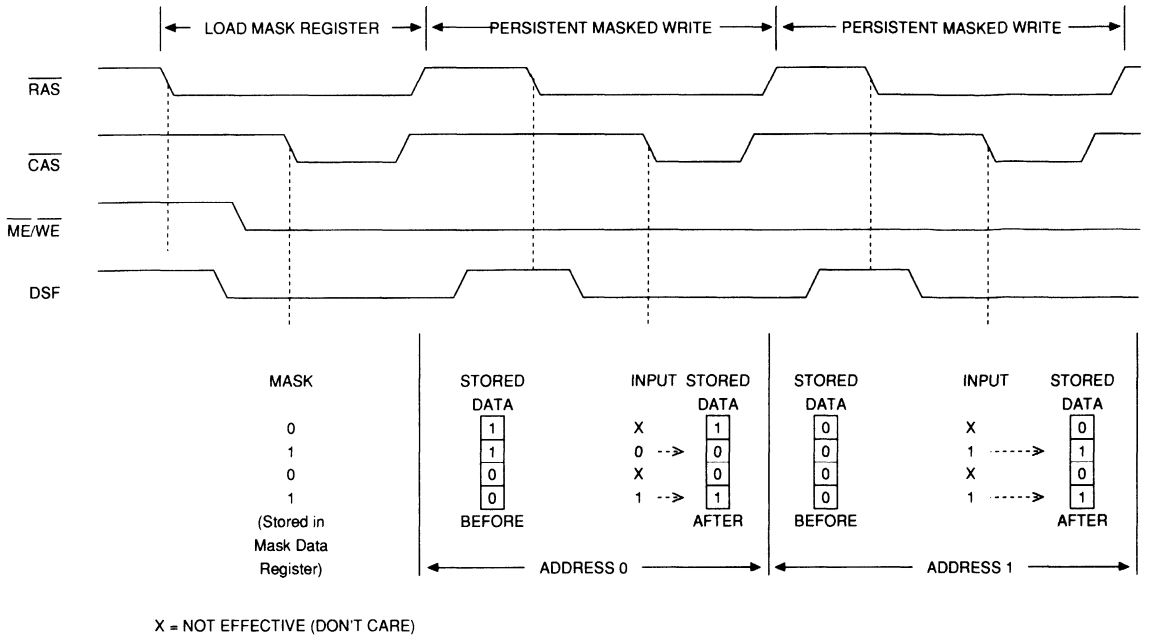


Figure 3
PERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{ME}/\overline{WE}$ HIGH and DSF HIGH when $\overline{RAS}$ goes LOW. The mask data is loaded into the internal register when $\overline{CAS}$ goes LOW. Mask data may also be loaded into the mask register by performing a NON-PERSISTENT MASKED WRITE cycle before the PERSISTENT MASKED WRITE cycles.

PERSISTENT MASKED WRITE cycles can then be performed by simply taking $\overline{ME}/(\overline{WE})$ LOW and DSF HIGH when $\overline{RAS}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NON-PERSISTENT MASKED WRITE cycle, the data present on the DQ inputs is not loaded into the mask register when $\overline{RAS}$ falls. Another PERSISTENT MASKED WRITE cycle can be performed without having to reload the mask data register. Figure 3 shows the LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycle operation. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow controllers that cannot put data out at $\overline{RAS}$ time to perform MASKED WRITES. PERSISTENT MASKED WRITE can be performed during FAST PAGE MODE cycles.

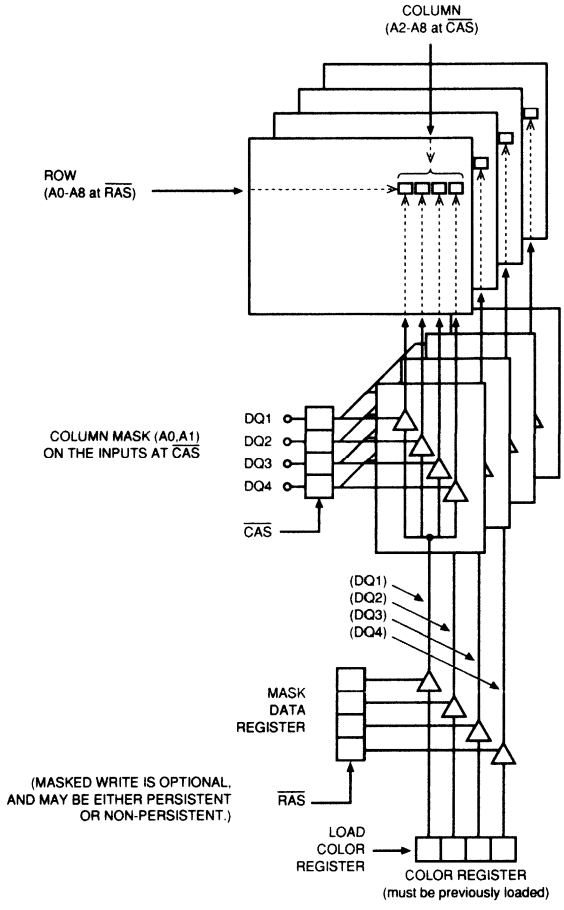


Figure 4
BLOCK WRITE EXAMPLE

BLOCK WRITE

If DSF is LOW when $\overline{CAS}$ goes LOW, the MT42C4256 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 4). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The ROW is addressed as in a normal DRAM WRITE cycle, however when $\overline{CAS}$ goes LOW only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs are then used to determine what combination of the four column locations will be changed. DQ1 acts as a write enable for column location A0=0, A1=0; DQ2 controls column location A0=1, A1=0; DQ3 controls A0=0, A1=1; and DQ4 controls A0=1, A1=1. The write enable controls are active HIGH; a logic 1 enables and a logic 0 disables the WRITE function.

The contents of the color register will then be written to the column locations enabled. Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

NON-PERSISTENT MASKED BLOCK WRITE

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NON-PERSISTENT MASKED BLOCK WRITE operates exactly like the normal NON-PERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one column location.

Like NON-PERSISTENT MASKED WRITE, the combination of $\overline{ME}/(\overline{WE})$ LOW and DSF LOW when $\overline{CAS}$ goes LOW initiates the NON-PERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the four bit planes can be masked and any combination of the four column locations can be masked.

PERSISTENT MASKED BLOCK WRITE

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF is HIGH when $\overline{CAS}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

LOAD MASK DATA REGISTER

The LOAD MASK DATA REGISTER operation and timing are identical to a normal WRITE cycle except that DSF is HIGH when $\overline{RAS}$ goes LOW. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{ME}/(\overline{WE})$, and DSF being HIGH when $\overline{RAS}$ goes LOW indicates the cycle is a REGISTER load cycle. DSF is used when $\overline{CAS}$ goes LOW to select the register to be loaded and must be LOW for a LOAD MASK DATA REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless a NON-PERSISTENT MASKED WRITE cycle or a LOAD MASK DATA REGISTER cycle is performed.

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK DATA REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the four DQ planes.

LOAD COLOR REGISTER

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when $\overline{CAS}$ goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW then $\overline{RAS}$ goes LOW. The state of $(\overline{ME})/\overline{WE}$ when $\overline{RAS}$ goes LOW indicates the direction of the TRANSFER, and DSF is used to select between NORMAL TRANSFER, SPLIT READ TRANSFER, and ALTERNATE WRITE TRANSFER cycles. Each of the TRANSFER cycles available are described below.

READ TRANSFER (DRAM-TO-SAM TRANSFER)

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when $\overline{RAS}$ goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate the four 512 bit DRAM rows that are to be tranferred to the four SAM data registers and the column address bits indicate the start address (or Tap point) of the next serial output cycle from the SAM data registers. To complete the TRANSFER, $\overline{TR}/(\overline{OE})$ is taken HIGH while $\overline{RAS}$ and $\overline{CAS}$ are still LOW. The rising edge of $\overline{TR}/(\overline{OE})$ must occur between the rising edges of successive clocks on the SC input (refer to the AC Timing Diagrams). The 2048 bits of DRAM data are then written into the SAM data registers and the serial shift start address is stored in an internal 9 bit register. If $\overline{SE}$ is LOW, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. $\overline{SE}$ enables the serial outputs and may be either HIGH or LOW during this operation. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

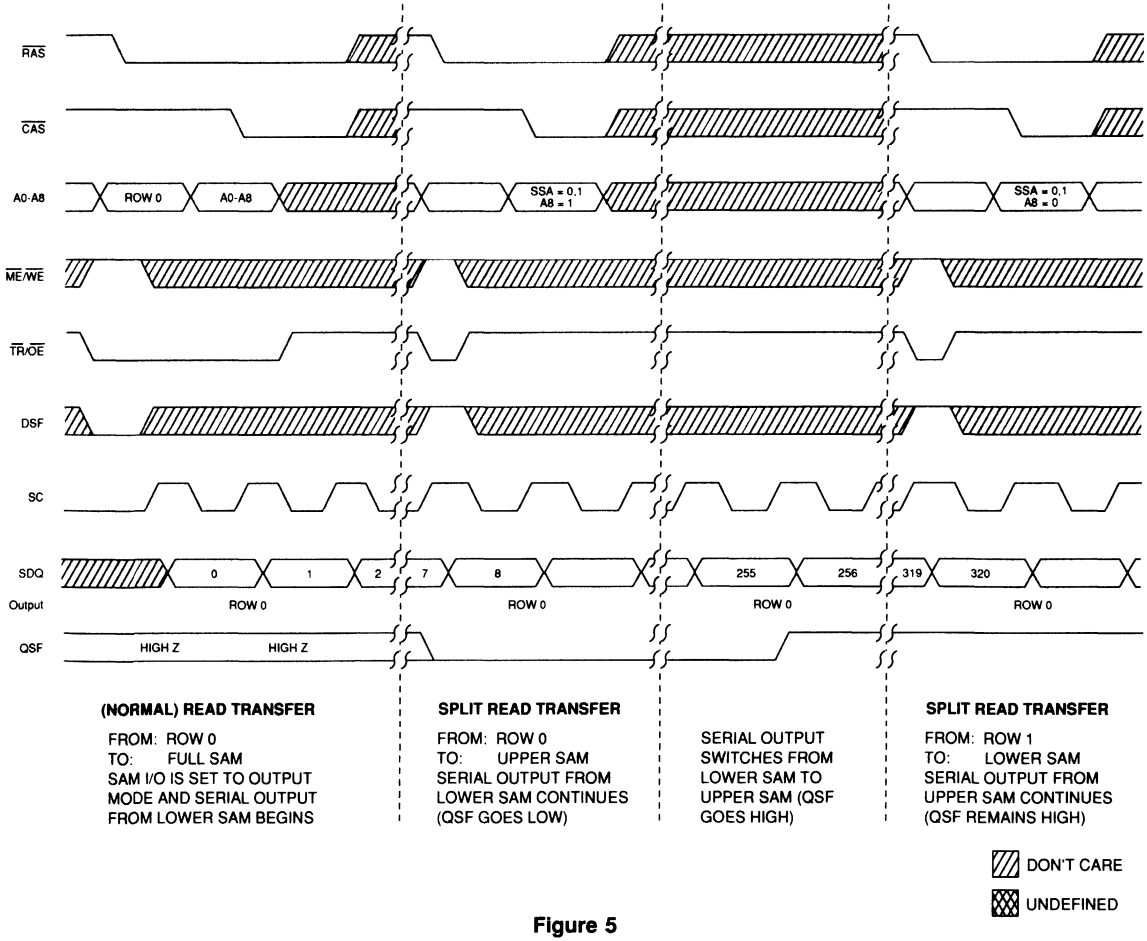


Figure 5
TYPICAL SPLIT READ TRANSFER INITIATION SEQUENCE

SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

The SPLIT READ TRANSFER cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles, the READ TRANSFER cycle had to occur immediately after the last bit of "old data" was clocked out the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data can be transferred to the other half. The transfer can occur at any time while the other half is sending data and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of $\overline{RAS}$ or $\overline{CAS}$. The transfer timing is generated internally for SPLIT TRANSFER cycles.

SPLIT TRANSFERS do not change the SAM I/O direction. A normal, or non-split, READ TRANSFER cycle must precede any sequence of SPLIT READ TRANSFER cycles to put the SAM I/O in the output mode and provide a SAM access (which half) reference. Then SPLIT READ TRANSFERS can be initiated by taking DSF HIGH when $\overline{RAS}$ goes LOW during the TRANSFER cycle. As in non-split transfers, the row address is used to specify the DRAM row to be transferred. The most significant column address, A8, is used to select which SAM half accepts the transfer (1=upper half, 0=lower half). The remainder of the column address bits determine the starting address (Tap) for the SAM half selected by A8.

Figure 5 shows a typical SPLIT READ TRANSFER initiation sequence. The normal READ TRANSFER is first performed, followed by a SPLIT READ TRANSFER of the same row to the upper half of the SAM. The purpose of the SPLIT TRANSFER of the same data is to initiate the split SAM operating mode and enable the QSF output. Serial access continues, and when the SAM address counter reaches 256 (A8=1, A0-A7=0) the QSF output goes HIGH. Since the serial access has now switched to the upper SAM, new data can now be transferred to the lower SAM. This sequence of waiting for the state of QSF to change and then transferring new data to the SAM half that is not being accessed can now be repeated. For example, the next step in Figure 5 would be to wait until QSF went LOW (indicating that row 1 data is shifting out the lower SAM) and then transferring the upper half of row 1 to the upper SAM.

WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the WRITE TRANSFER function is identical to the READ TRANSFER FUNCTION described previously except $(\overline{ME})/\overline{WE}$ and $\overline{SE}$ must be LOW when $\overline{RAS}$ goes LOW. The row address indicates the DRAM row that the SAM data registers will be written to and the column address (SSA or Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A WRITE TRANSFER does not change the SAM I/O direction.

PSEUDO WRITE TRANSFER (SERIAL INPUT MODE ENABLE)

The PSEUDO WRITE TRANSFER cycle is used to change the direction of SAM port from output to input without performing a WRITE TRANSFER cycle. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with $\overline{SE}$ held HIGH instead of LOW. The DRAM data will not be disturbed and the SAM will be ready to accept input data.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the ALTERNATE WRITE TRANSFER is identical to the WRITE TRANSFER except that the DSF pin is taken HIGH, with $(\overline{ME})/\overline{WE}$ LOW, allowing $\overline{SE}$ to be a "don't care." This allows the outputs to be disabled using $\overline{SE}$ during a WRITE TRANSFER cycle.

TRUTH TABLE

CODE	FUNCTION	RAS FALLING EDGE					CAS FALL	A0 - A8[1]		DQ1 - DQ4[2]		REGISTERS	
		CAS	TR/OE	ME/WE	DSF	SE	DSF	RAS	CAS	RAS	CAS[3]	MASK	COLOR
	DRAM OPERATIONS												
CBR	CAS-BEFORE-RAS REFRESH	0	X	1	X	X	X	—	X	—	X	X	X
ROR	RAS ONLY REFRESH	1	1	X	X	X	—	ROW	—	X	—	X	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	X	0	ROW	COLUMN	X	VALID DATA	X	X
RWNM	NON-PERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	X	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	X
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	X	0	ROW	COLUMN	X	VALID DATA	USE	X
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	X	1	ROW	COLUMN (A2 - A8)	X	COLUMN MASK	X	USE
BWNM	NON-PERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	X	1	ROW	COLUMN (A2 - A8)	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASKED REGISTER)	1	1	0	1	X	1	ROW	COLUMN	X	COLUMN	USE	USE
	REGISTER OPERATIONS												
LMR	LOAD MASK REGISTER	1	1	1	1	X	0	ROW[4]	X	X	WRITE MASK	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	X	1	ROW[4]	X	X	COLOR DATA	X	LOAD
	TRANSFER OPERATIONS												
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	X	ROW	SSA[5] (TAP)	X	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	X	ROW	SSA[5] (TAP)	X	X	X	X
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	X	ROW	SSA[5] (TAP)	X	X	X	X
PWT	PSEUDO WRITE TRANSFER (SERIAL INPUT MODE ENABLE)	1	0	0	0	1	X	ROW[4]	SSA[5] (TAP)	X	X	X	X
AWT	ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	1	X	X	ROW	SSA[5] (TAP)	X	X	X	X

NOTES: 1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
2. These columns show what must be present on the DQ1-DQ4 inputs when RAS falls and when CAS falls.
3. On WRITE cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is latched at the falling edge of CAS or TR/OE, whichever is later.
4. The ROW that is addressed will be refreshed, but no particular ROW address is required.
5. SSA = SAM Starting Address or Tap Point. This is the first SAM location that the next SC cycle will access.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V
Operating Temperature, Ta(Ambient) .....0°C to +70°C
Storage Temperature (Ceramic) .....-65°C to +150°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation .....1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	$V_{CC}+1$	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(Notes 3, 4, 5) ($0°C \le T_A \le 70°C$, V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (any input ($0V \le V_{IN} \le V_{CC}$), all other pins not under test = 0 volts).	I_L	-10	10	µA	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, $0V \le V_{OUT} \le V_{CC}$).	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A_0-A_8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{ME/WE}$, $\overline{TR/OE}$, SC, $\overline{SE}$, DSF	C_{I2}		7	pF	2
Output Capacitance: DQ, SDQ, QSF	C_O		7	pF	2

CURRENT DRAIN, SAM IN STANDBY

(Notes 2, 3) (0°C ≤ T_A ≤ 70°C, V_{CC} = 5.0V ± 10%)

		MAX					
PARAMETER/CONDITION	**SYMBOL**	**-8**	**-10**	**-12**	**-15**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: T_{RC} = $T_{RC(MIN)}$)	I_{CC1}	90	80	70	70	mA	3, 4
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL} $\overline{CAS}$ = CYCLING; T_{PC} = $T_{PC(MIN)}$)	I_{CC2}	70	60	50	50	mA	
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH} after 8 $\overline{RAS}$ cycles min).	I_{CC3}	5	5	5	5	mA	3
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2).	I_{CC4}	1	1	1	1	mA	3,4
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH}).	I_{CC5}	90	80	60	60	mA	25
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling).	I_{CC6}	80	70	60	60	mA	3
SAM/DRAM DATA TRANSFER	I_{CC7}	90	80	75	75	mA	

CURRENT DRAIN, SAM ACTIVE (tsc = MIN)

(Notes 2, 3) (0°C ≤ T_A ≤ 70°C, V_{CC} = 5.0V ± 10%)

		MAX					
PARAMETER/CONDITION	**SYMBOL**	**-8**	**-10**	**-12**	**-15**	**UNITS**	**NOTES**
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: T_{RC} = $T_{RC(MIN)}$)	I_{CC8}	115	110	100	100	mA	3, 4
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL} $\overline{CAS}$ = CYCLING; T_{PC} = $T_{PC(MIN)}$)	I_{CC9}	95	90	85	85	mA	
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{IH} after 8 $\overline{RAS}$ cycles min).	I_{CC10}	30	30	30	30	mA	3
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at V_{CC}-0.2V or V_{SS} + 0.2).	I_{CC11}	25	25	25	25	mA	3,4
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$=Cycling; $\overline{CAS}$=V_{IH}).	I_{CC12}	115	110	100	100	mA	25
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$=Cycling).	I_{CC13}	105	100	95	95	mA	3
SAM/DRAM DATA TRANSFER	I_{CC14}	115	110	100	100	mA	

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	160		190		220		260		ns	
READ-MODIFY-WRITE cycle time	^tRWC	215		220		295		330		ns	
PAGE-MODE READ or WRITE cycle time	^tPC	45		55		70		85		ns	
Access time from $\overline{RAS}$	^tRAC		80		100		120		150	ns	14
Access time from $\overline{CAS}$	^tCAC		20		25		30		45	ns	15
Access time from $\overline{TR}$/$\overline{OE}$	^tOE		20		25		30		45	ns	
Access time from column address	^tAA		40		50		60		70	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		50		60		70	ns	
$\overline{RAS}$ pulse width	^tRAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	80	100,000	100	100,000	120	100,000	150	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	25		25		35		45		ns	
$\overline{RAS}$ precharge time	^tRP	70		80		90		100		ns	
$\overline{CAS}$ pulse width	^tCAS	20	10,000	25	10,000	30	10,000	45	10,000	ns	
$\overline{CAS}$ hold time	^tCSH	80		100		120		150		ns	
$\overline{CAS}$ precharge time	^tCPN	15		15		20		25		ns	16
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	10		10		15		20		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	60	20	75	25	90	25	105	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		10		10		ns	
Row address set-up time	^tASR	0		0		0		0		ns	
Row address hold time	^tRAH	12		15		15		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	17	40	20	50	25	60	25	70	ns	18
Column address set-up time	^tASC	0		0		0		0		ns	
Column address hold time	^tCAH	20		20		25		25		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	60		70		85		95		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	40		50		60		70		ns	
Read command set-up time	^tRCS	0		0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		0		ns	19
$\overline{CAS}$ to output in low-Z	^tCLZ	0		0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	35	0	35	ns	20
Output Disable	^tOD		20		20		35		35	ns	

DRAM TIMING PARAMETERS (Continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command set-up time	^tWCS	0		0		0		0		ns	21
Write command hold time	^tWCH	15		20		25		30		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	60		75		85		90		ns	
Write command pulse width	^tWP	15		20		25		30		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	25		25		30		35		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	25		25		30		35		ns	
Data-in set-up time	^tDS	0		0		0		0		ns	22
Data-in hold time	^tDH	20		20		25		25		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	60		70		90		100		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	110		130		160		185		ns	21
Column address to $\overline{WE}$ delay time	^tAWD	70		80		100		120		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	55		65		75		85		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	3	50	3	50	ns	9, 10
Refresh Period (512 cycles)	^tREF		8		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge time	^tRPC	0		0		0		0		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCSR	10		10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	^tCHR	30		30		30		40		ns	5
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ set-up time	^tWSR	0		0		0		0		ns	
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ hold time	^tRWH	10		10		10		15		ns	
Mask Data to $\overline{RAS}$ set-up time	^tMS	0		0		0		0		ns	
Mask Data to $\overline{RAS}$ hold time	^tMH	10		15		15		20		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. The 8 $\overline{RAS}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, DRAM data output (DQ1-DQ4) is high impedance.
12. If $\overline{CAS}$ = V_{IL}, DRAM data output (DQ1-DQ4) may contain data from the last valid READ cycle.
13. DRAM output timing measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (max).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (max) limit ensures that ^tRAC (max) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (max) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (max) limit ensures that ^tRCD (max) can be met. ^tRAD (max) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (max) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (min), the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (min), $^tAWD \ge {}^tAWD$ (min) and $^tCWD \ge {}^tCWD$ (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}/\overline{WE}$ leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if $\overline{TR}/\overline{OE}$ is LOW then taken HIGH, DQ goes open.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}/\overline{WE}$ = LOW and $\overline{TR}/\overline{OE}$=HIGH.
25. SAM output timing is measured with a load equivalent to 2 TTL gate and 50pF.
26. TRANSFER command means that $\overline{TR}/\overline{OE}$ is LOW when $\overline{RAS}$ goes LOW.
27. NON-TRANSFER command means that $\overline{TR}/\overline{OE}$ is HIGH when $\overline{RAS}$ goes LOW.

TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 17, 25) (0° C ≤ T_A ≤ + 70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
TRANSFER Command to $\overline{RAS}$ Set Up Time	^tTLS	0		0		0		0		ns	26
Transfer Command to $\overline{RAS}$ Hold Time	^tTLH	10	10,000	10	10,000	10	10,000	15	10,000	ns	
TRANSFER Command to $\overline{RAS}$ Hold Time (REAL-TIME READ TRANSFER only)	^tRTH	70	10,000	80	10,000	90	10,000	100	10,000	ns	26
TRANSFER Command to $\overline{CAS}$ Hold Time (REAL-TIME READ TRANSFER only)	^tCTH	20		25		30		35		ns	26
TRANFER Command to Column Address Hold Time (For REAL TIME READ TRANSFER only)	^tATH	25		30		35		40		ns	
TRANSFER Command to SC Lead Time	^tTSL	5		5		5		10		ns	26
TRANSFER Command to $\overline{RAS}$ Lead Time	^tTRL	10		10		10		10		ns	26
TRANSFER Command to $\overline{RAS}$ Delay Time	^tTRD	15		15		15		20		ns	26
TRANSFER Command to $\overline{CAS}$ Time	^tTCL	10		10		10		10		ns	26
TRANSFER Command to $\overline{CAS}$ Delay Time	^tTCD	15		15		15		20		ns	26
First SC edge to TRANSFER Command Delay Time	^tTSD	10		10		10		20		ns	26
Serial Output Buffer Turn Off Delay from $\overline{RAS}$	^tSDZ	10	35	10	40	10	50	10	60	ns	
SC to $\overline{RAS}$ Set Up Time	^tSRS	30		35		40		45		ns	
$\overline{RAS}$ to SC Delay Time	^tSRD	20		25		30		35		ns	
Serial Data Input to $\overline{SE}$ Delay Time	^tSZE	0		0		0		0		ns	
$\overline{RAS}$ to SD Buffer Turn On Time	^tSRO	0		0		0		0		ns	
Serial Data Input Delay from $\overline{RAS}$	^tSDD	45		50		55		60		ns	
Serial Data Input to $\overline{RAS}$ Delay Time	^tSZS	0		0		0		0		ns	
Serial Input Mode Enable ($\overline{SE}$) to $\overline{RAS}$ Set Up Time	^tESR	0		0		0		0		ns	
Serial Input Mode Enable ($\overline{SE}$) to $\overline{RAS}$ Hold Time	^tREH	10		10		10		15		ns	
NON-TRANSFER Command to $\overline{RAS}$ Set Up Time	^tYS	0		0		0		0		ns	27
NON-TRANSFER Command to $\overline{RAS}$ Hold Time	^tYH	10		10		10		10		ns	27
DSF to $\overline{RAS}$ Set Up Time	^tFSR	0		0		0		0		ns	
DSF to $\overline{RAS}$ Hold Time	^tRFH	10		15		15		20		ns	
DSF to $\overline{RAS}$ Hold Time	^tFHR	60		65		70		75		ns	
DSF to $\overline{CAS}$ Set-up Time	^tFSC	0		0		0		0		ns	
DSF to $\overline{CAS}$ Hold Time	^tCFH	15		20		20		25		ns	
SC to QSF Delay Time	^tSQD		25		30		35		40	ns	
SPLIT TRANSFER Set Up Time	^tSTS	30		35		40		45		ns	
SPLIT TRANSFER Hold Time	^tSTH	30		35		40		45		ns	
$\overline{TR/OE}$ to QSF Delay Time	^tTQD		25		30		35		40	ns	
$\overline{CAS}$ to QSF Delay Time	^tCQD		35		40		45		50	ns	

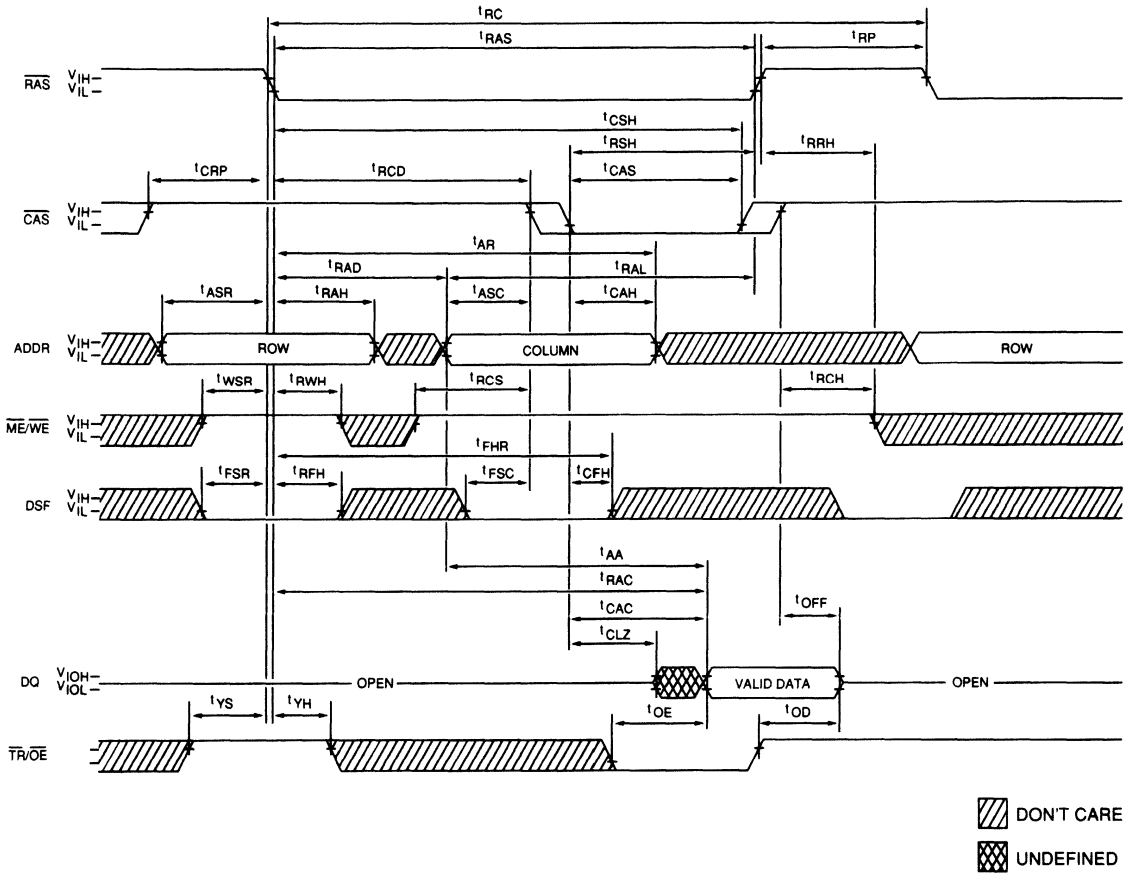
SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 3, 4, 5, 17, 25) (0° C ≤ T_A ≤ + 70°C, Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Serial Clock Cycle Time	^tSC	25		30		35		40		ns	
Access Time from SC	^tSAC		25		30		35		40	ns	
SC Precharge Time (SC Low Time)	^tSP	10		10		12		15		ns	
SC Pulse Width (SC High Time)	^tSAS	10		10		12		15		ns	
Access Time from $\overline{SE}$	^tSEA		20		25		30		40	ns	
$\overline{SE}$ Precharge Time	^tSEP	15		15		15		20		ns	
$\overline{SE}$ Pulse Width	^tSE	15		15		15		20		ns	
Serial Data Out Hold Time after SC High	^tSOH	5		10		10		10		ns	
Serial Output Buffer Turn Off Delay from $\overline{SE}$	^tSEZ	0	15	0	15	0	25	0	30	ns	
Serial Data in Set Up Time	^tSDS	0		0		0		0		ns	
Serial Data in Hold Time	^tSDH	20		20		20		25			
SERIAL INPUT (Write) Enable Set Up Time	^tSWS	0		0		0		0		ns	
SERIAL INPUT (Write) Enable Hold Time	^tSWH	25		30		35		45		ns	
SERIAL INPUT (Write) Disable Set Up Time	^tSWIS	0		0		0		0		ns	
SERIAL INPUT (Write) Disable Hold Time	^tSWIH	25		30		35		45		ns	

DRAM READ CYCLE

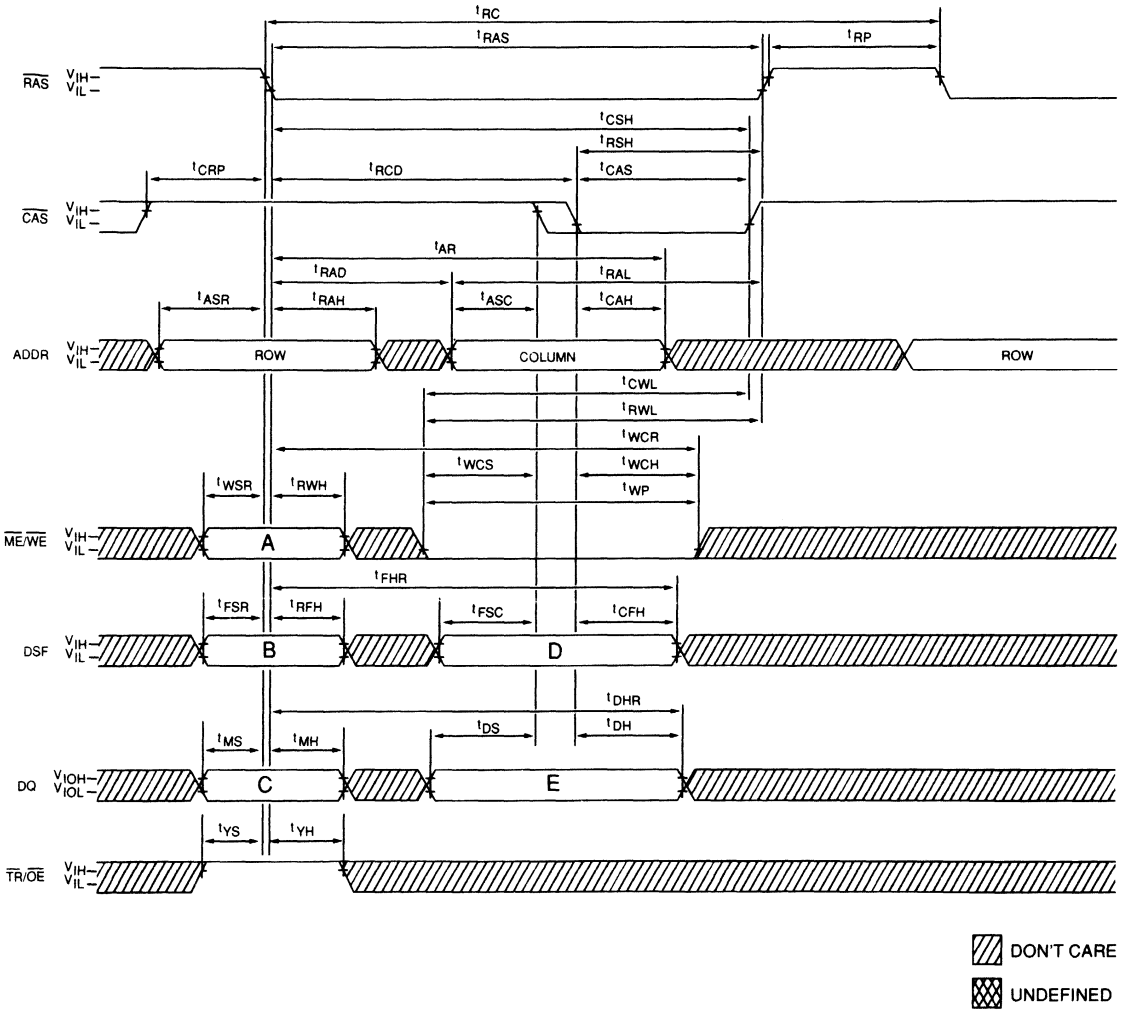


WRITE CYCLE FUNCTION TABLE

LOGIC STATES					FUNCTION
$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge		
A $\overline{ME}/\overline{WE}$	B DSF	C DQ (Input)	D DSF	E DQ (Input)	
1	0	X	0	DRAM Data	Normal DRAM WRITE (or READ)
0	0	Write Mask	0	DRAM Data (Masked)	Non-Persistent (Load and Use) Masked Write to DRAM
0	1	X	0	DRAM Data (Masked)	Persistent (Use Register) Masked Write to DRAM
1	0	X	1	Column Mask	Block Write to DRAM (No Data Mask)
0	0	Write Mask	1	Column Mask	Non-Persistent (Load and Use) Masked Block Write to DRAM
0	1	X	1	Column Mask	Persistent (Use Register) Masked Block Write to DRAM
1	1	X	0	Write Mask	Load Mask Data Register
1	1	X	1	Color Data	Load Color Register

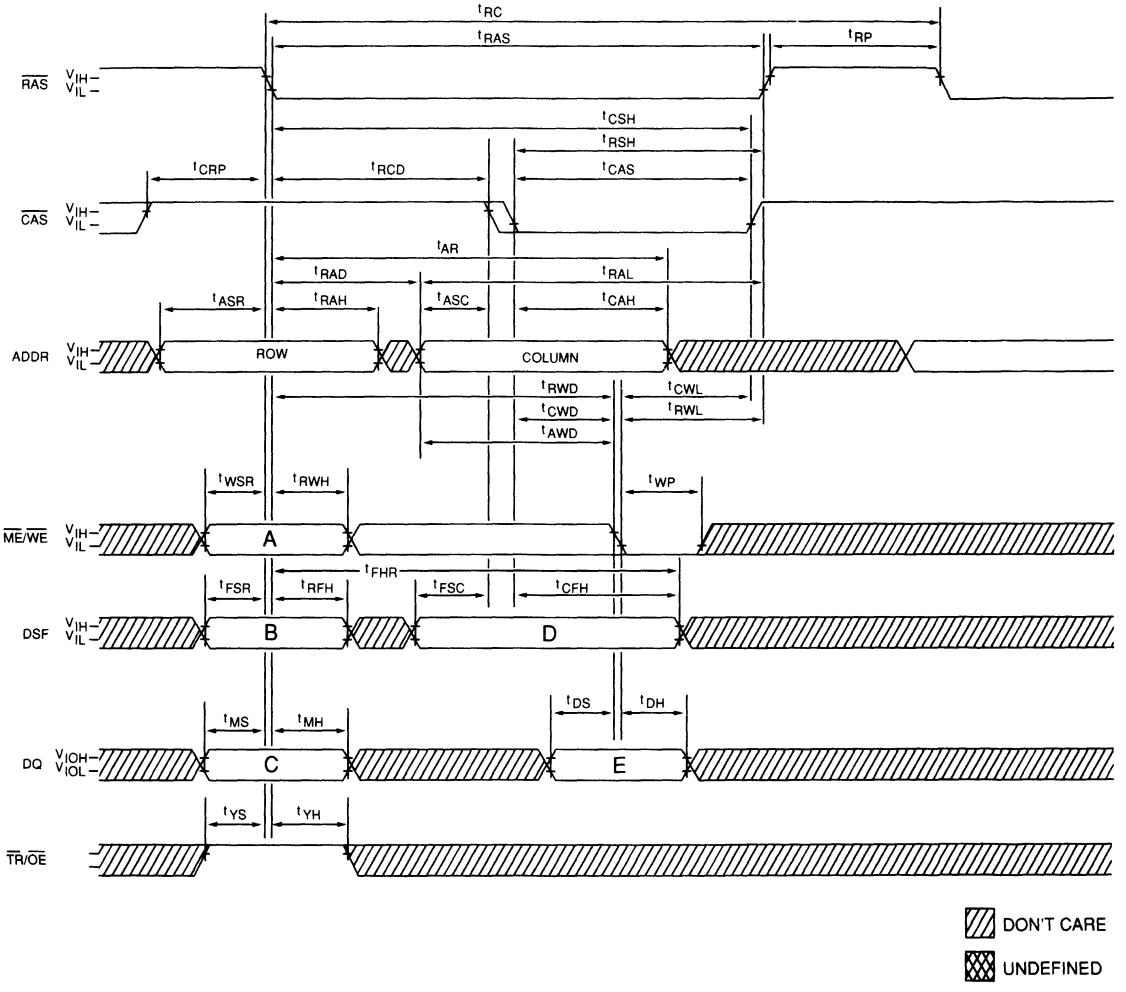
NOTE: Refer to this function table to determine the logic states of A, B, C, D, and E for the WRITE cycle timing diagrams on the following pages.

DRAM EARLY-WRITE CYCLE



NOTE: The Logic states of "A", "B", "C", "D", and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

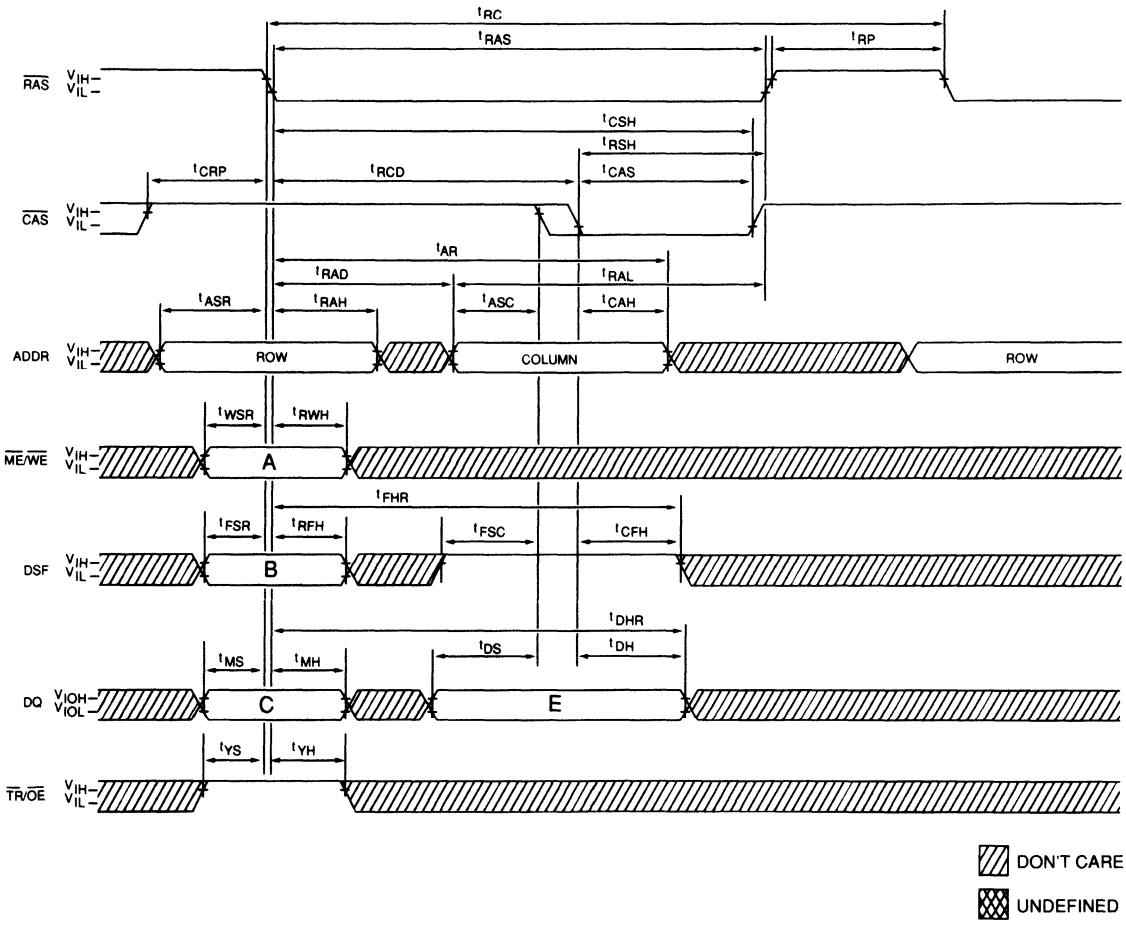
DRAM LATE-WRITE CYCLE



NOTE 1: The Logic states of "A", "B", "C", "D", and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

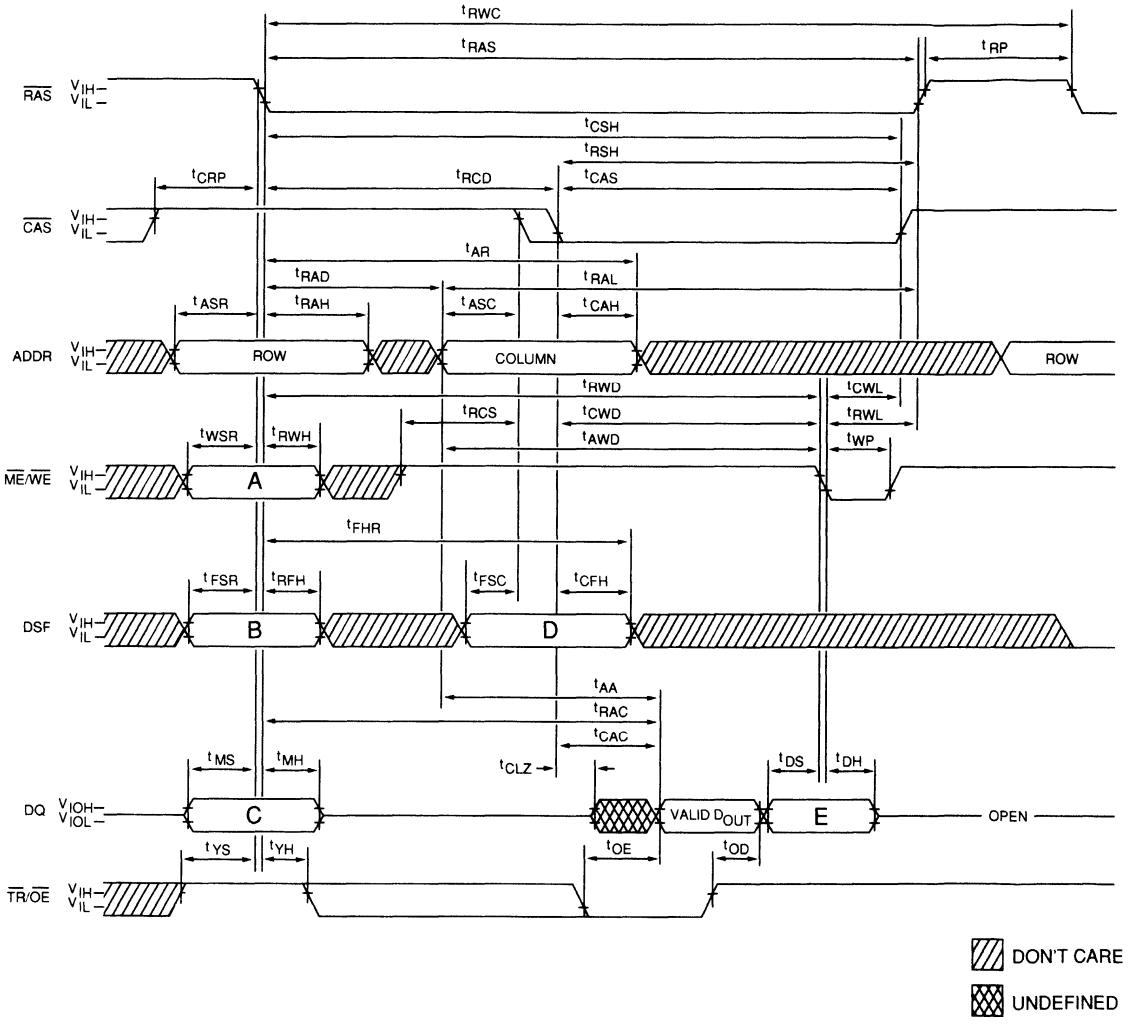
NOTE 2: The Column Mask data for a BLOCK WRITE cycle must be valid at the falling edge of $\overline{CAS}$, regardless of the level of $\overline{ME}/\overline{WE}$. See the BLOCK WRITE cycle timing diagram.

DRAM BLOCK-WRITE CYCLE



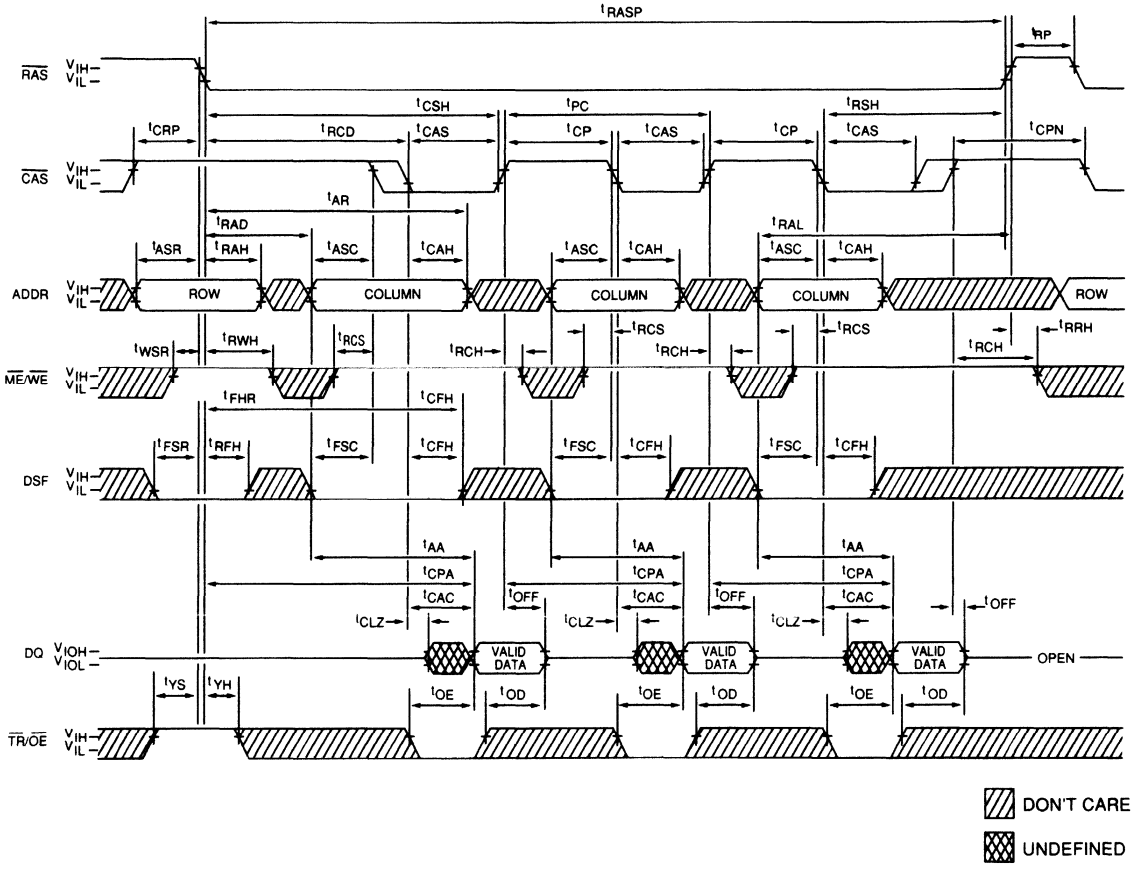
NOTE: The Logic states of "A", "B", "C", and "E" determine the type of BLOCK WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM READ-WRITE CYCLE
(READ-MODIFY-WRITE CYCLE)



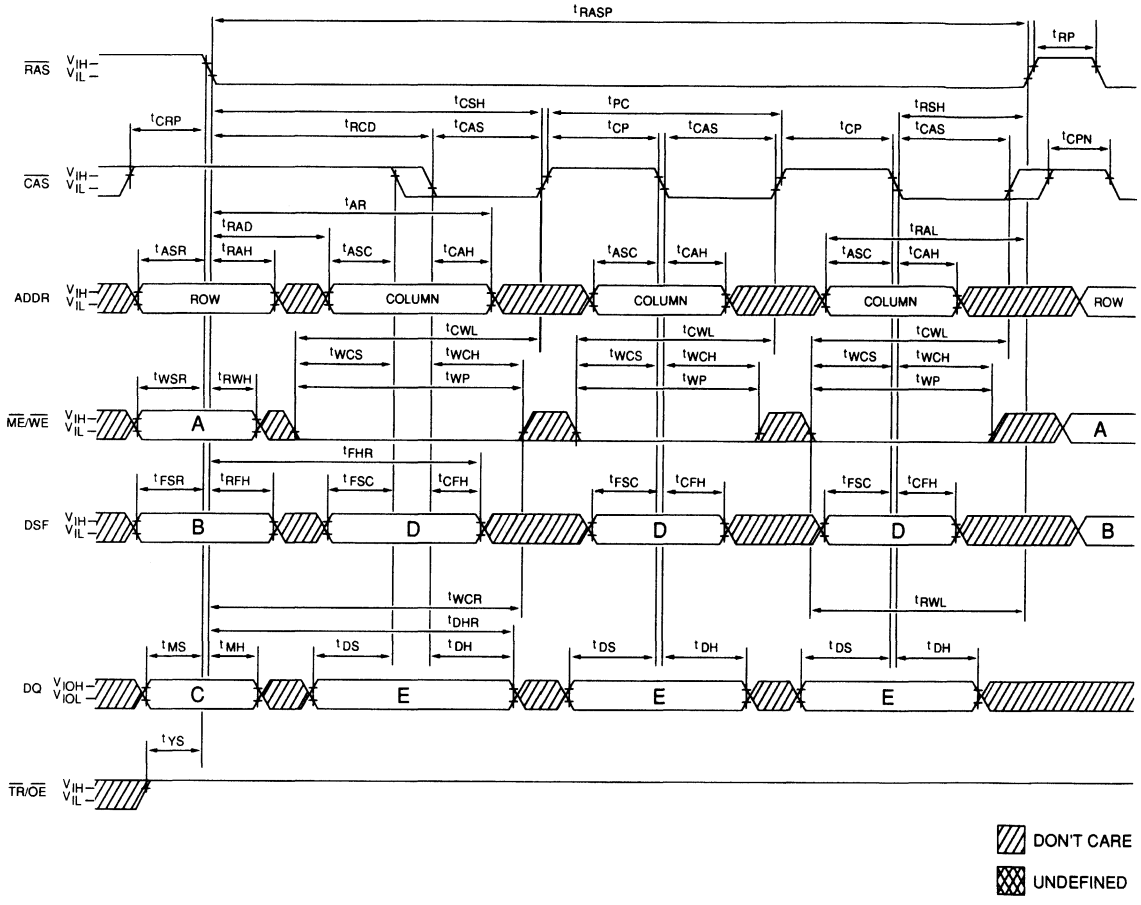
NOTE: The Logic states of "A", "B", "C", "D", and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM PAGE-MODE READ CYCLE



NOTE: WRITE cycles or READ-MODIFY-WRITE cycles can be mixed with READ cycles while in PAGE-MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.

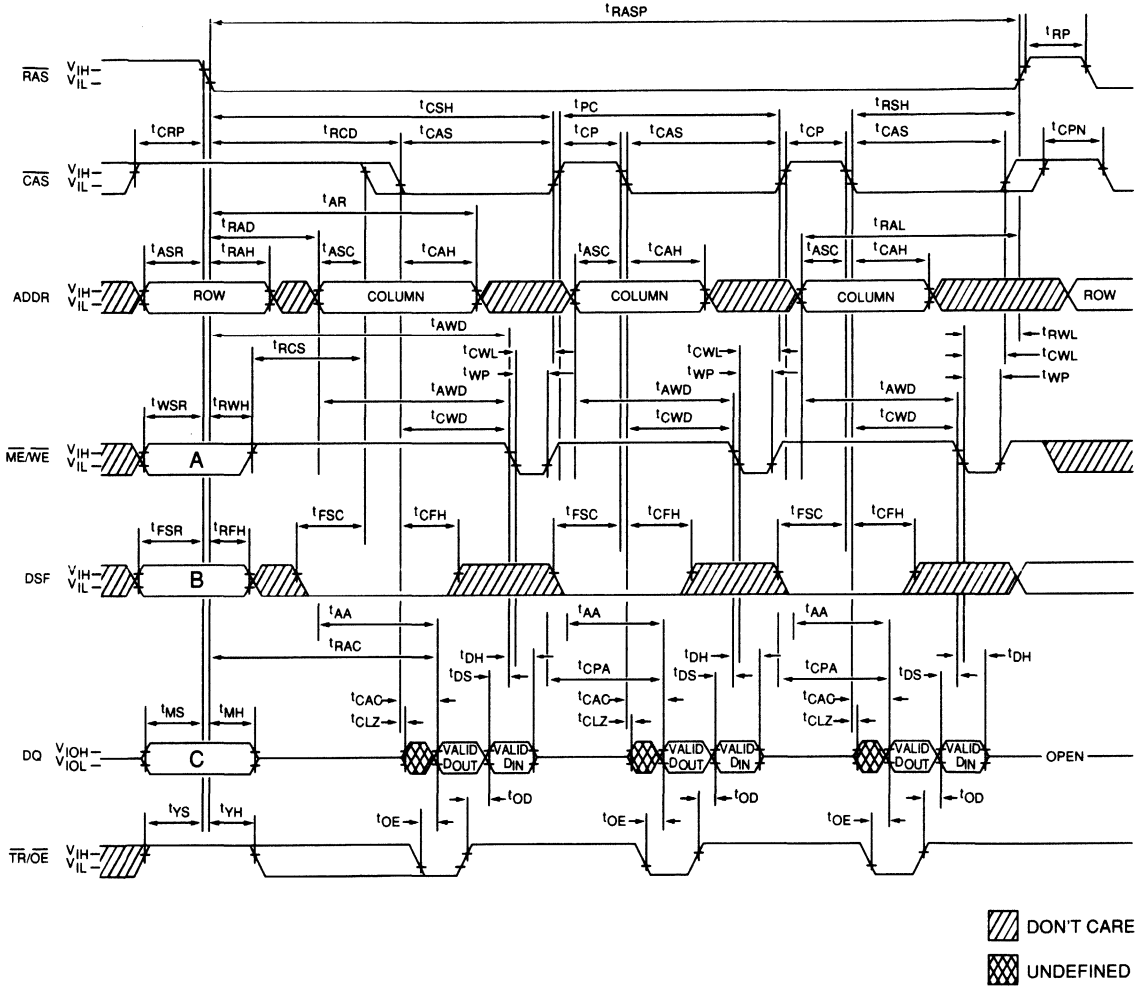
DRAM PAGE-MODE EARLY-WRITE CYCLE



NOTE 1: READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in PAGE-MODE.

NOTE 2: The Logic states of "A", "B", "C", "D", and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

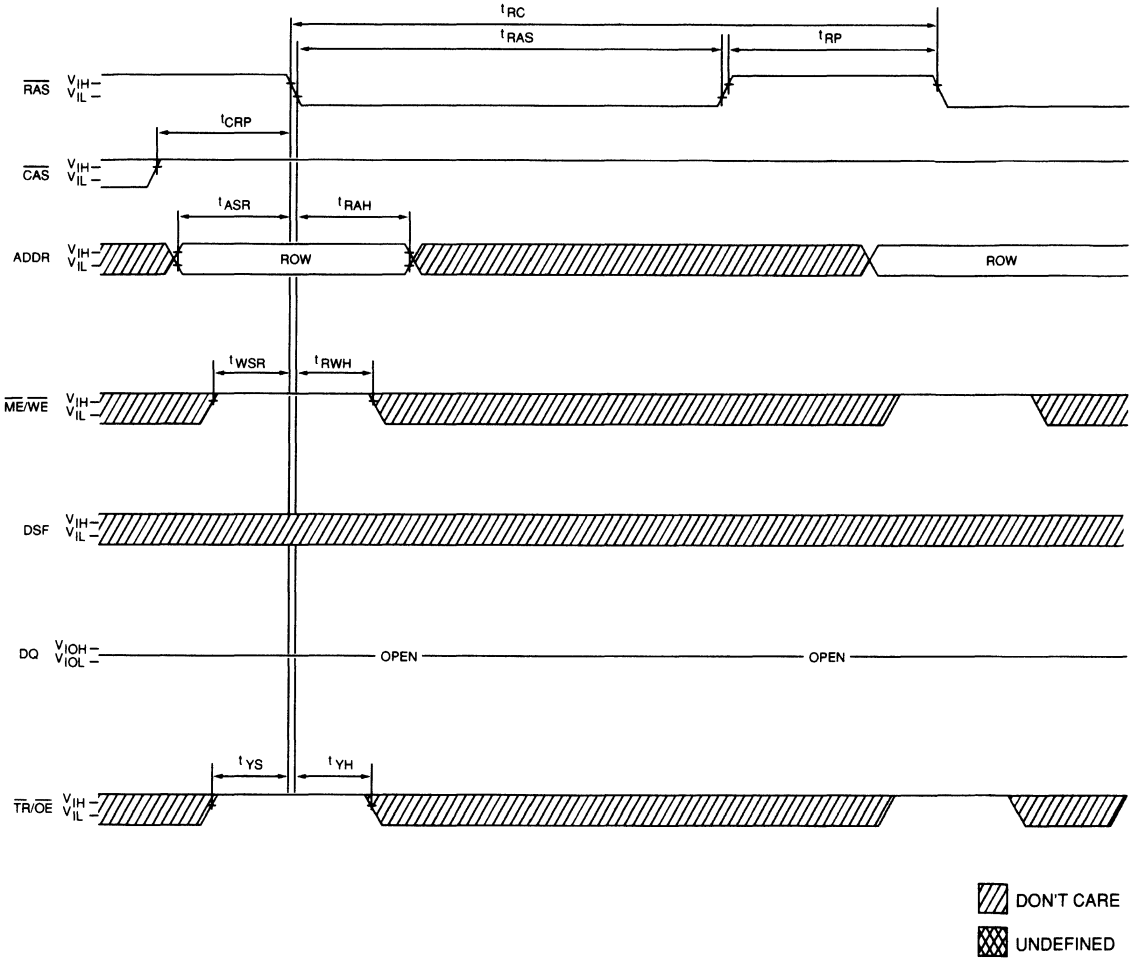
DRAM PAGE-MODE READ-WRITE CYCLE
(PAGE-MODE READ-MODIFY-WRITE CYCLE)



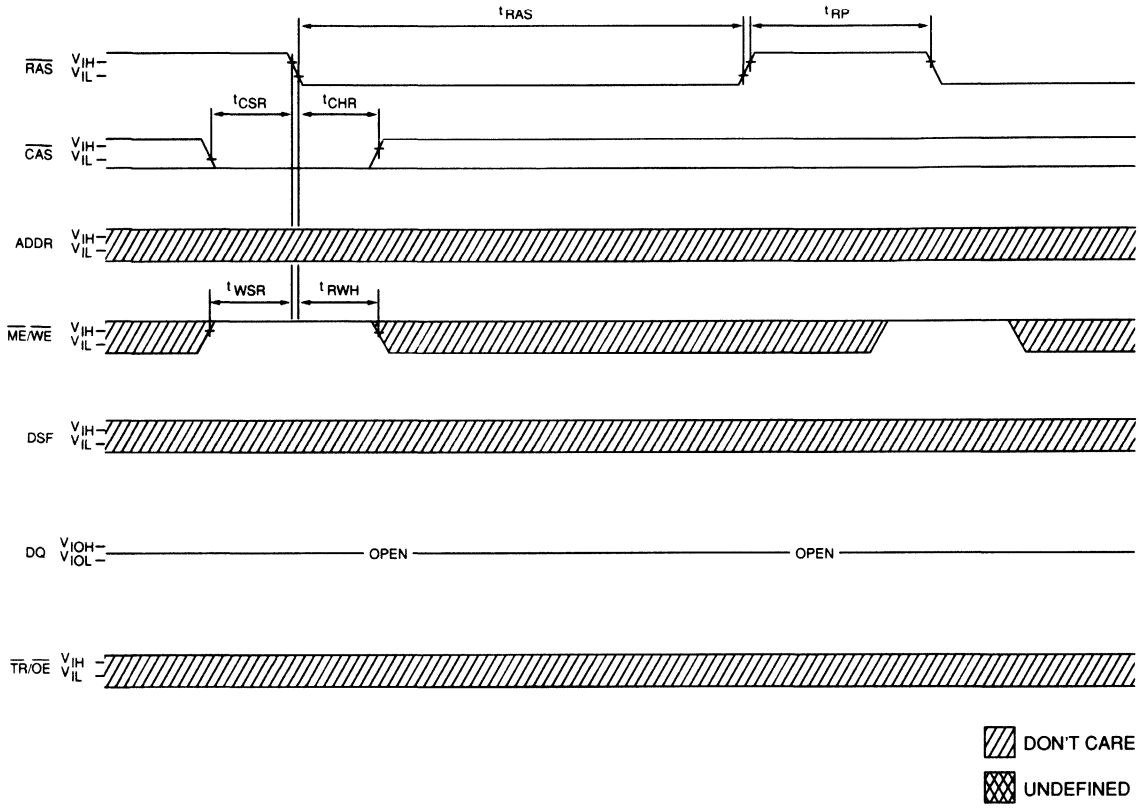
NOTE 1: READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in PAGE-MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.

NOTE 2: The Logic states of "A", "B" and "C" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

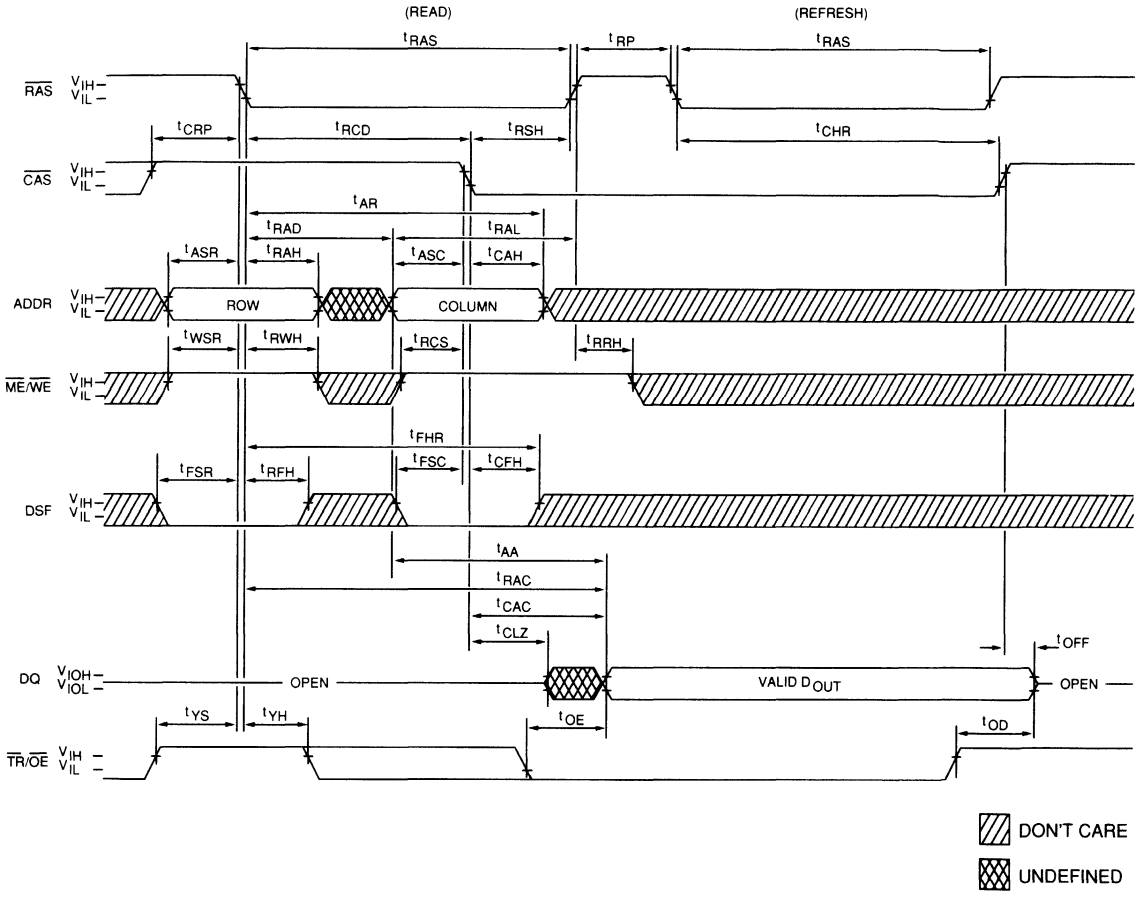
DRAM $\overline{RAS}$ ONLY REFRESH CYCLE
(ADDR = A0-A8)



CAS-BEFORE-RAS REFRESH CYCLE



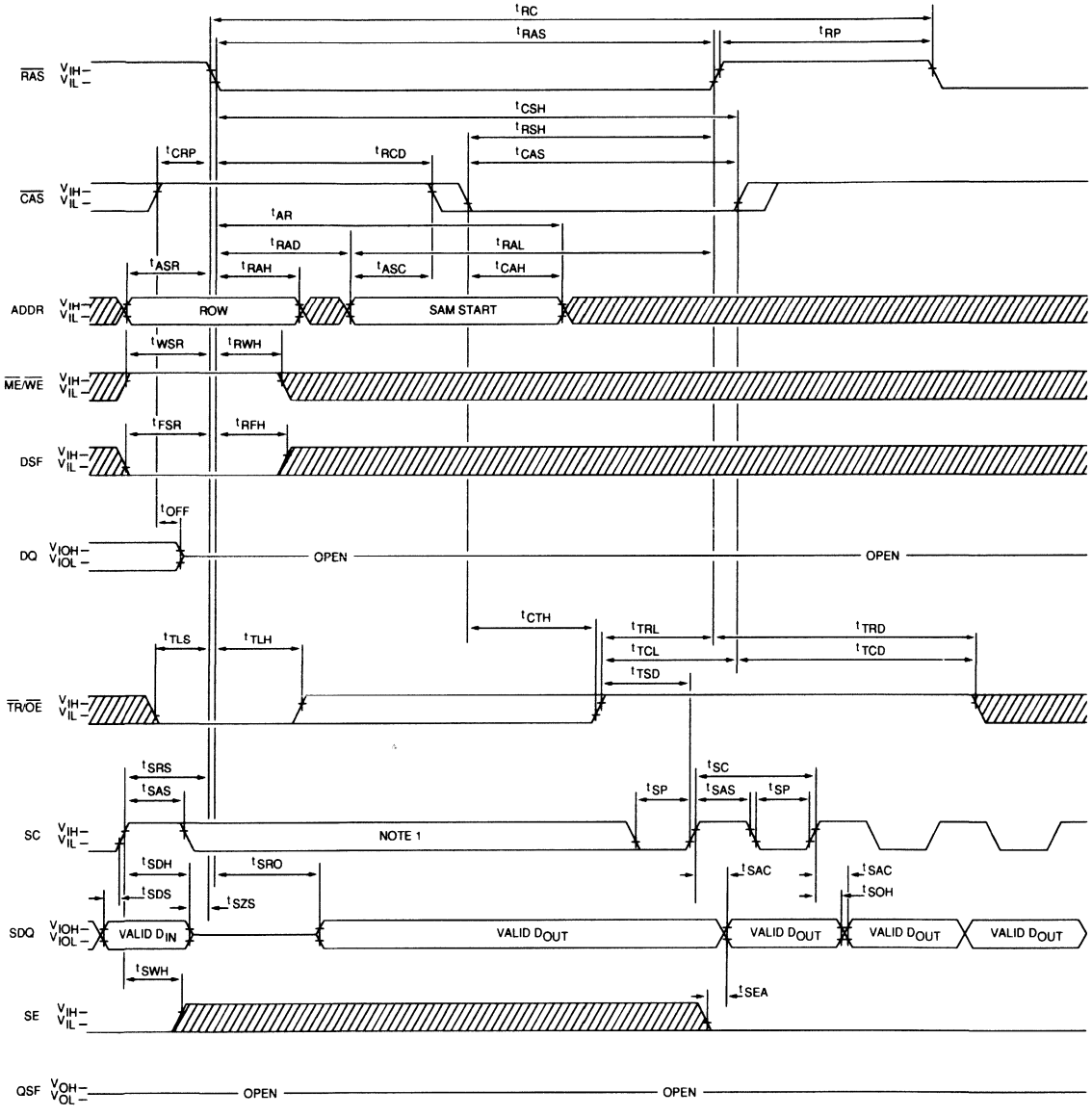
DRAM HIDDEN REFRESH CYCLE



NOTE: A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{ME}/\overline{WE}$ = LOW (when $\overline{CAS}$ goes LOW) and $\overline{TR}/\overline{OE}$ = HIGH.

READ TRANSFER
(DRAM-TO-SAM TRANSFER)

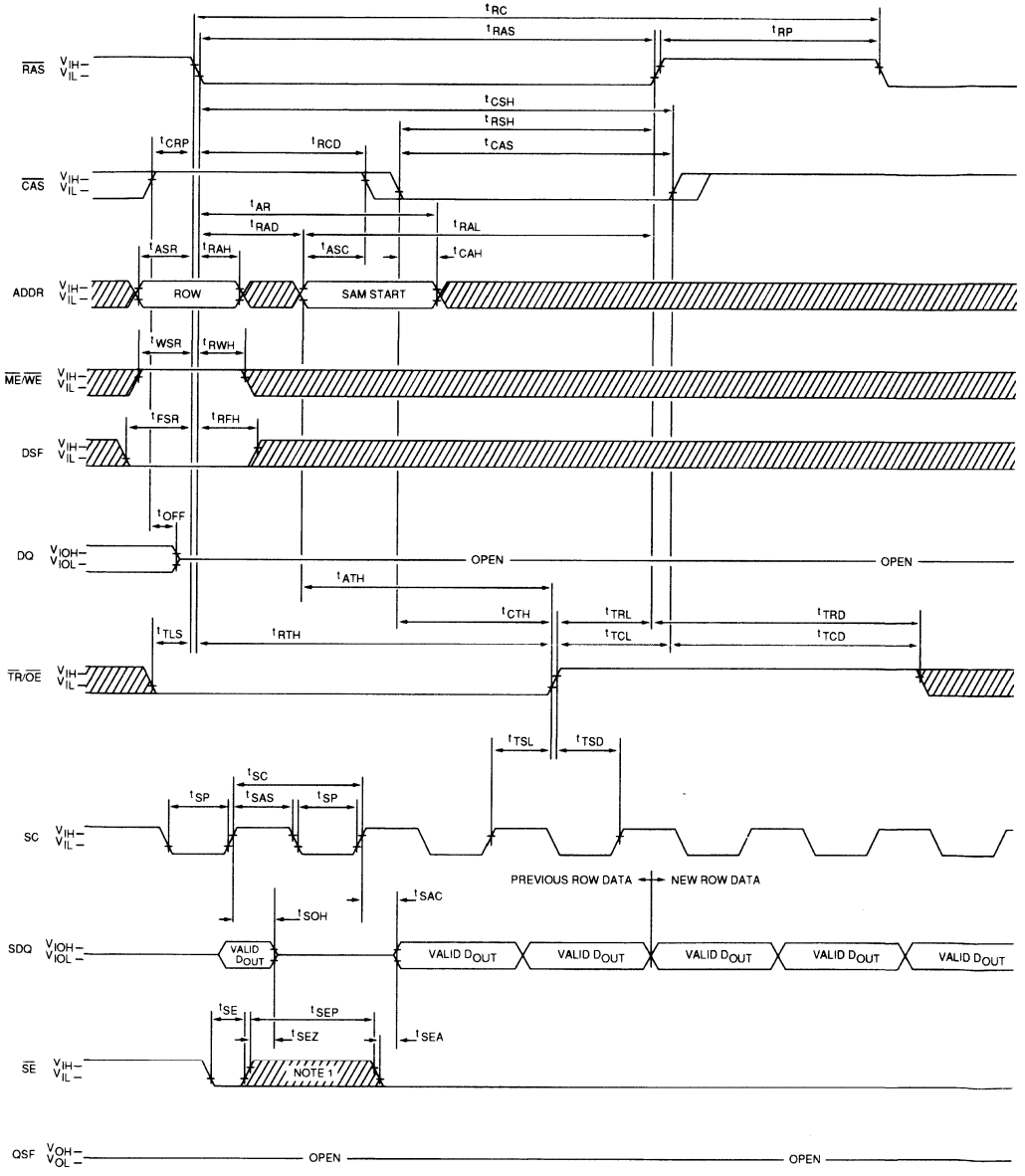
(When part was previously in the SERIAL INPUT mode.)



NOTE 1: There must be no rising edges on the SC input during this time period.

REAL-TIME READ TRANSFER
(DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode.)

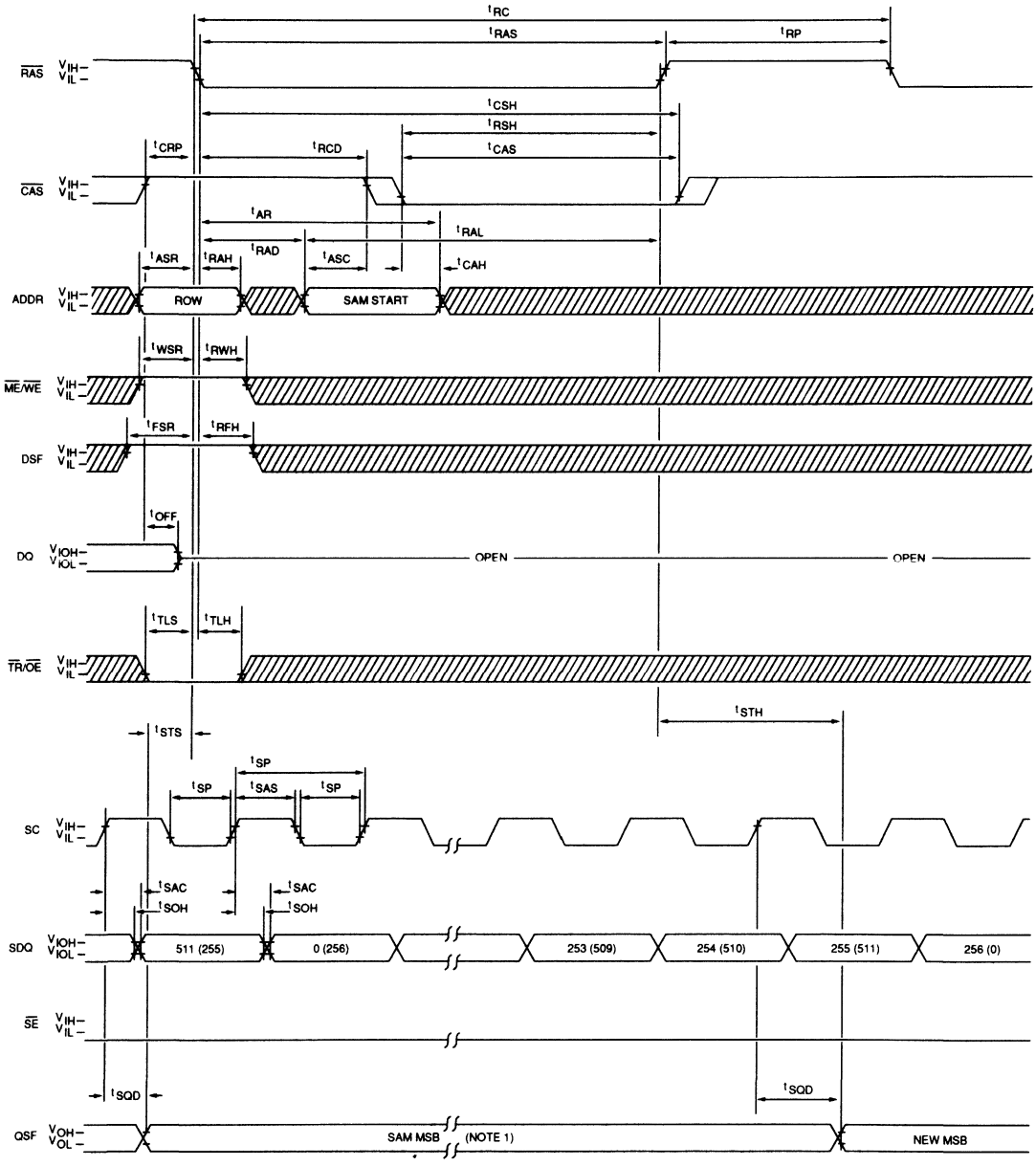


NOTE 1: The $\overline{SE}$ pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.

DON'T CARE

UNDEFINED

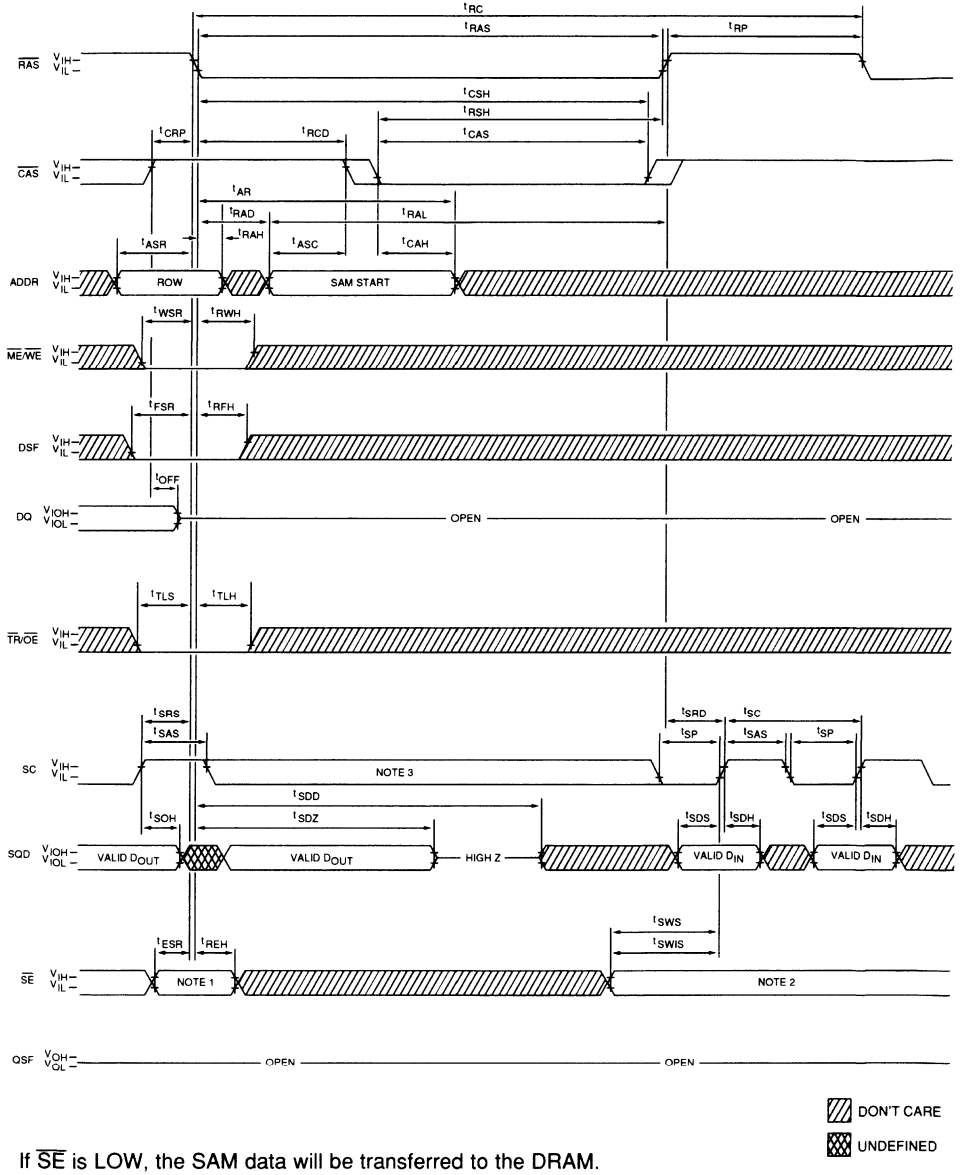
SPLIT READ TRANSFER
(SPLIT DRAM-TO-SAM TRANSFER)



NOTE 1: QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

WRITE TRANSFER and PSEUDO WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode.)



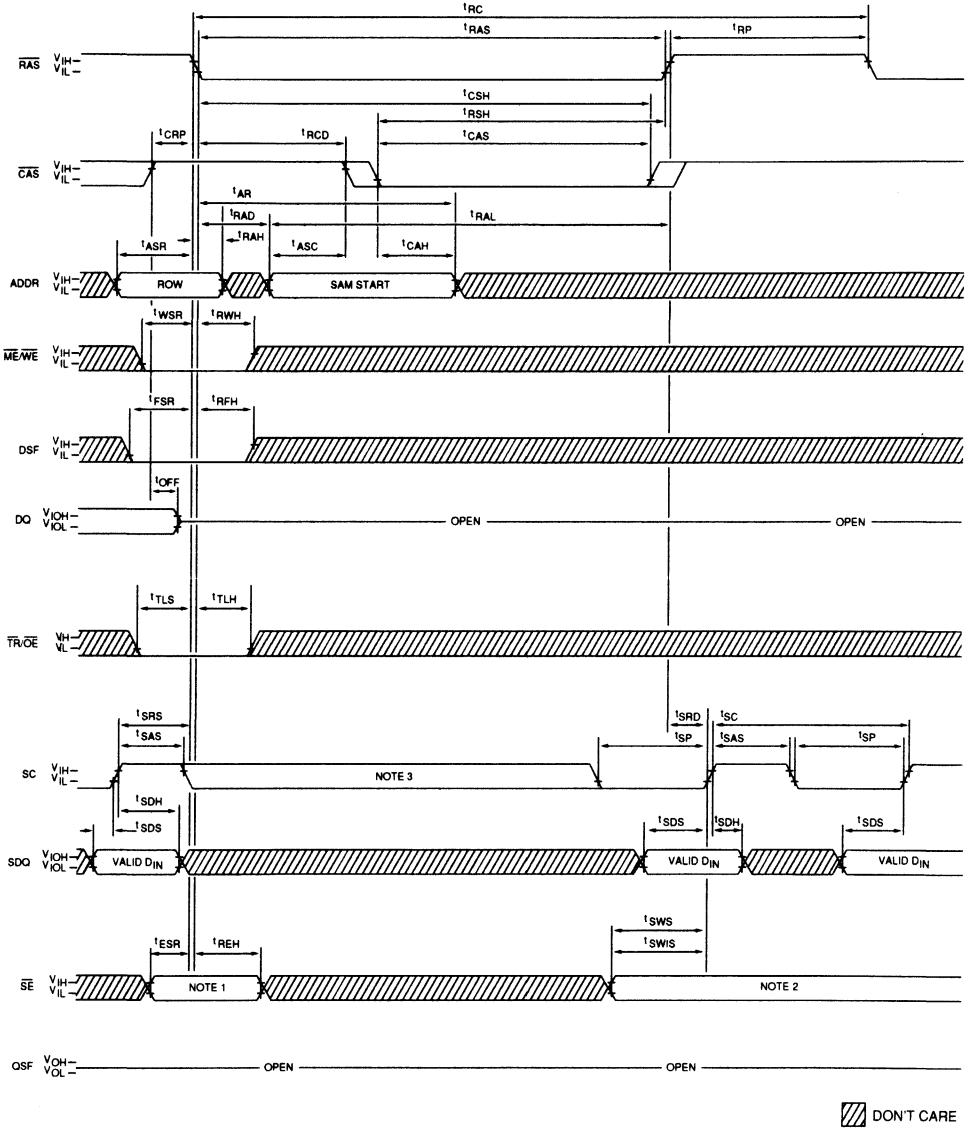
NOTE 1: If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

NOTE 2: $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.

NOTE 3: There must be no rising edges on the SC input during this time period.

WRITE TRANSFER
(SAM-TO-DRAM TRANSFER)

(When part was previously in the SERIAL INPUT mode.)

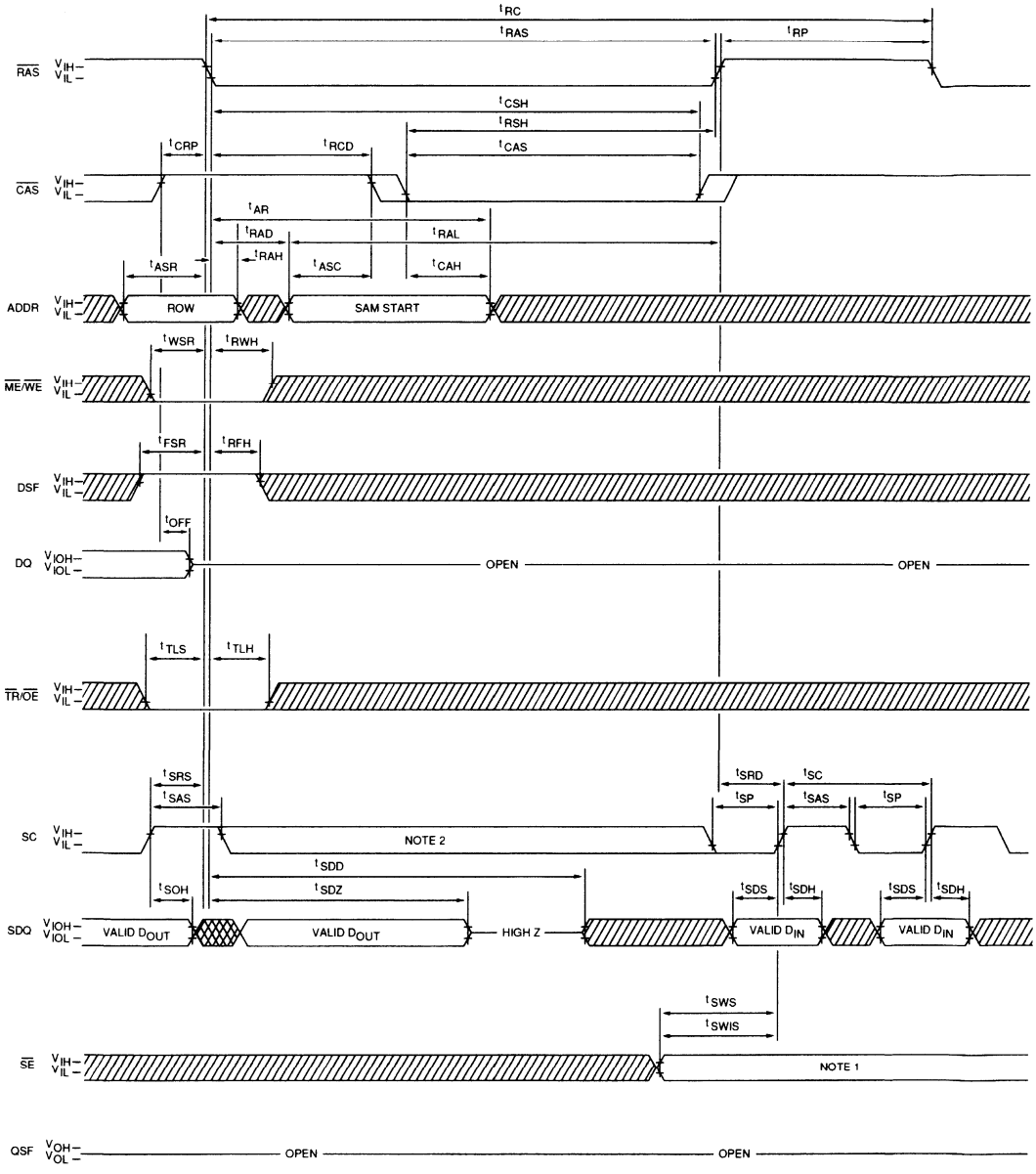


NOTE 1: If $\overline{SE}$ is LOW, the SAM data will be transferred to the DRAM.
If $\overline{SE}$ is HIGH, the SAM data will not be transferred to the DRAM (SERIAL INPUT MODE ENABLE cycle).

NOTE 2: $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.

NOTE 3: There must be no rising edges on the SC input during this time period.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)



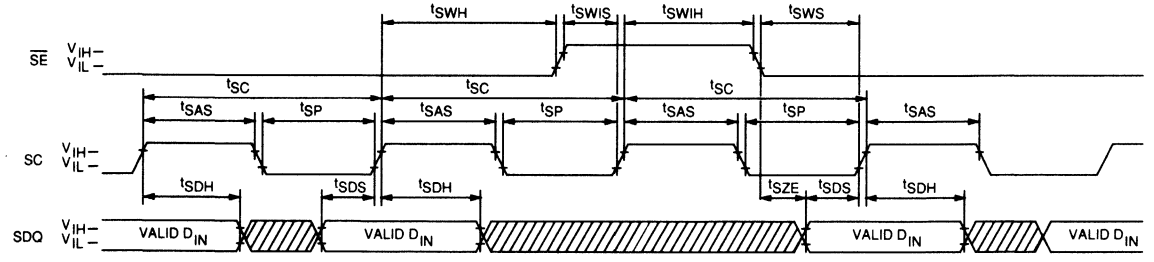
NOTE 1: $\overline{SE}$ must be LOW to input new serial data, but the serial address register is incremented by SC regardless of $\overline{SE}$.

NOTE 2: There must be no rising edges on the SC input during this time period.

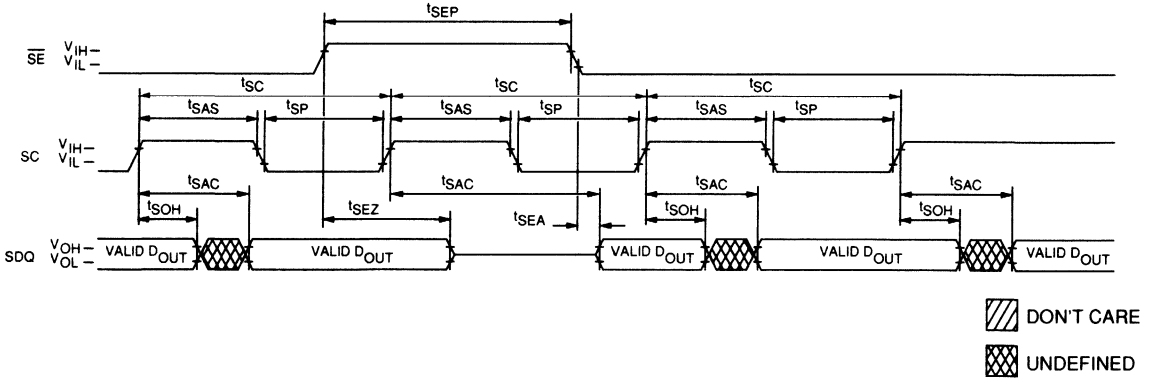
DON'T CARE

UNDEFINED

SAM SERIAL INPUT



SAM SERIAL OUTPUT



DON'T CARE

UNDEFINED

DYNAMIC RAMs 1
DYNAMIC RAM MODULES 2
MULTIPORT DYNAMIC RAMs 3
STATIC RAMs 4
STATIC RAM MODULES 5
CACHE DATA RAMs 6
FIFO MEMORIES 7
APPLICATION INFORMATION 8
MILITARY INFORMATION 9
PACKAGE INFORMATION 10
SALES INFORMATION 11

SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package and Number of Pins				Process	Page
				PDIP	SOJ	CDIP	LCC		
2K x 8	CE & OE	MT5C1608	12 to 35	24	24	24	24	CMOS	4-3
2K x 8	CE, OE & ALE	MT5C1628	15 to 45	28	28	28	28,32	CMOS	4-11
4K x 4	CE only	MT5C1604	12 to 35	20	24	20	20	CMOS	4-19
4K x 4	CE & OE	MT5C1605	12 to 35	22	24	22	22	CMOS	4-27
4K x 4	Separate I/O	MT5C1606	12 to 35	24	24	24	28	CMOS	4-35
4K x 4	Separate I/O HI-Z	MT5C1607	12 to 35	24	24	24	28	CMOS	4-35
8K x 8	CE1, CE2 & OE	MT5C6408	12 to 35	28	28	28	32	CMOS	4-43
16K x 1	CE only	MT5C1601	12 to 35	20	24	20	20	CMOS	4-51
16K x 4	CE only	MT5C6404	12 to 35	22	24	22	22	CMOS	4-59
16K x 4	CE & OE	MT5C6405	12 to 35	24	24	24	28	CMOS	4-67
16K x 4	Separate I/O, CE1, CE2	MT5C6406	12 to 35	28	28	28	28	CMOS	4-75
16K x 4	Separate I/O HI-Z	MT5C6407	12 to 35	28	28	28	28	CMOS	4-75
32K x 8	CE & OE	MT5C2568	20 to 45	28	28	28	32	CMOS	4-83
64K x 1	CE only	MT5C6401	12 to 35	22	24	22	22	CMOS	4-91
64K x 4	CE only	MT5C2564	20 to 45	24	24	24	28	CMOS	4-99
64K x 4	CE & OE	MT5C2565	20 to 45	28	28	28	28	CMOS	4-107
128K x 8	CE & OE	MT5C1008	20 to 45	28	-	28	-	CMOS	4-115
256K x 1	CE only	MT5C2561	20 to 45	24	24	24	28	CMOS	4-117
256K x 4	CE & OE	MT5C1005	20 to 45	28	-	28	-	CMOS	4-125
1MEG x 1	CE & OE	MT5C1001	20 to 45	28	-	28	-	CMOS	4-127

SRAM 2K x 8 SRAM

FEATURES

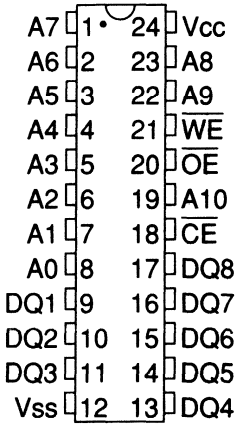
- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS

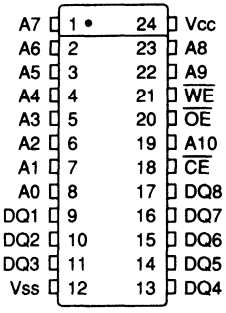
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC (28 pin)	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

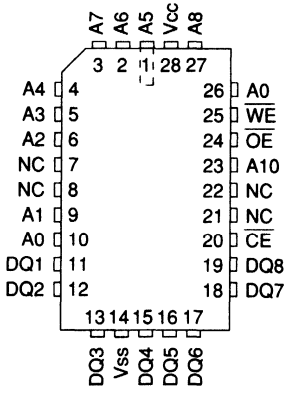
24L/300DIP (PG, CF)



24L/300 SOJ (DJB)



28L/LCC (ECF)



GENERAL DESCRIPTION

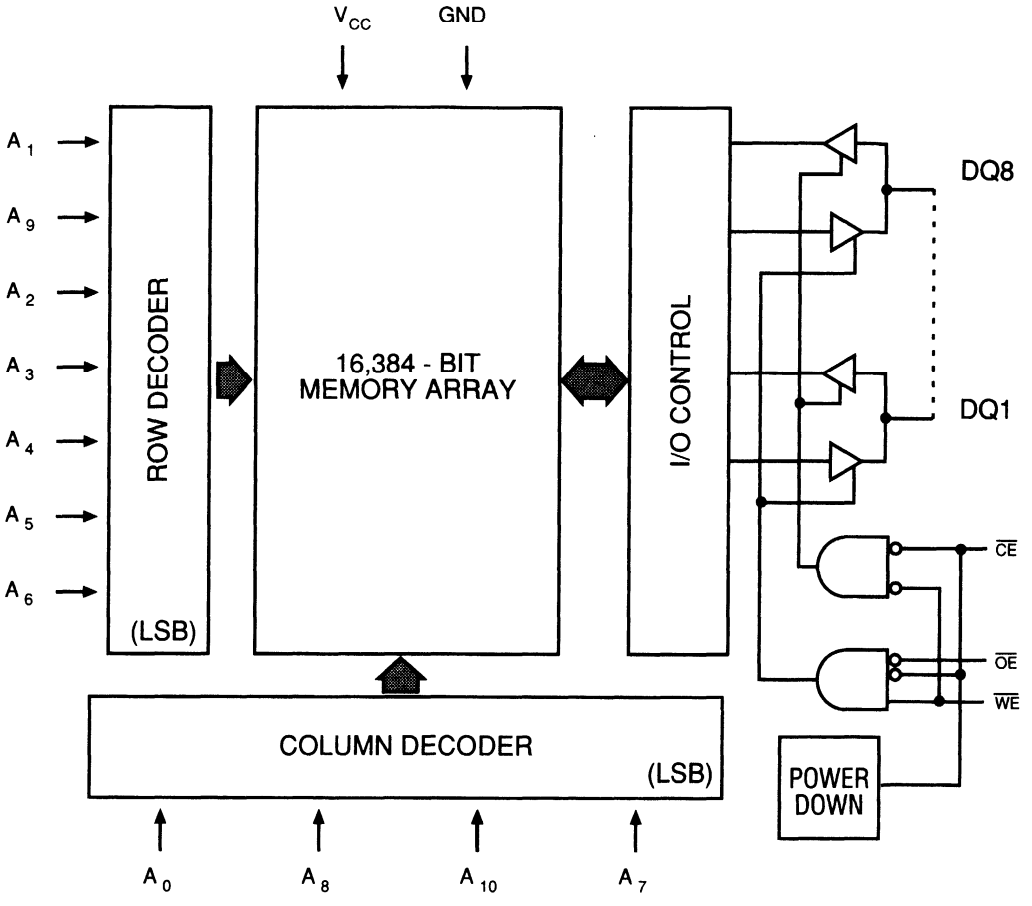
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	125	110	100	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	50	45	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	3	3	3	3	3	3	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C, V_{CC} = 5V ± 10%)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	t_{RC}	12		15		20		25		30		35		ns	
Address access time	t_{AA}		12		15		20		25		30		35	ns	
Chip enable access time	t_{ACE}		11		12		15		20		25		30	ns	
Output hold from access change	t_{OH}	3		3		3		3		3		3		ns	
Chip enable to output in low Z	t_{LZCE}	3		3		5		5		5		5		ns	
Chip disable to output in high Z	t_{HZCE}		7		7		10		10		15		20	ns	6,7
Chip enable to power up time	t_{PU}	0		0		0		0		0		0		ns	
Chip disable to power down time	t_{PD}		12		15		20		25		30		35	ns	
Output enable access time	t_{AOE}		7		7		9		10		15		20	ns	
Output enable to output in low Z	t_{LZOE}	0		0		0		0		0		0		ns	
Output disable to output in high Z	t_{HZOE}		6		6		10		10		15		20	ns	6
WRITE Cycle															
WRITE cycle time	t_{WC}	12		15		20		25		30		35		ns	
Chip enable to end of write	t_{CW}	10		12		15		20		25		25		ns	
Address valid to end of write	t_{AW}	12		12		15		20		25		25		ns	
Address set-up time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns	
Write pulse width	t_{WP}	10		12		15		20		25		25		ns	
Data set-up time	t_{DS}	7		8		10		10		15		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	2		2		2		2		2		2		ns	
Write enable to output in high Z	t_{HZWE}	0	6	0	6	0	8	0	10	0	12	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

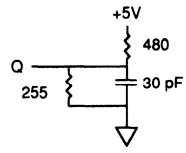


Fig. 1 OUTPUT LOAD EQUIVALENT

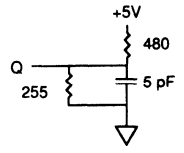


Fig. 2 OUTPUT LOAD EQUIVALENT

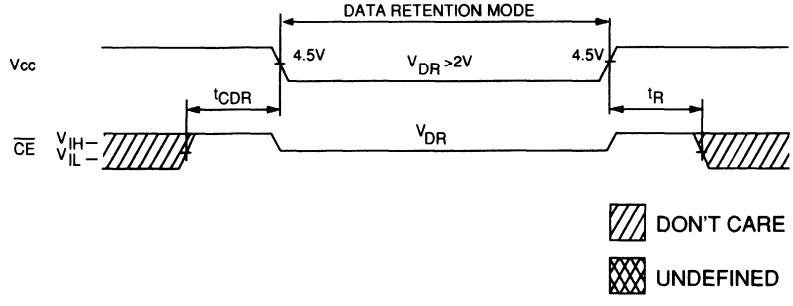
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.

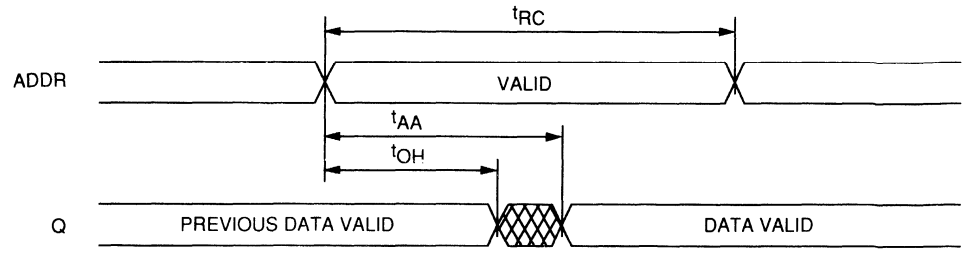
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	ICCDR		95	500	µA	
		Vcc=3v			350	750	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

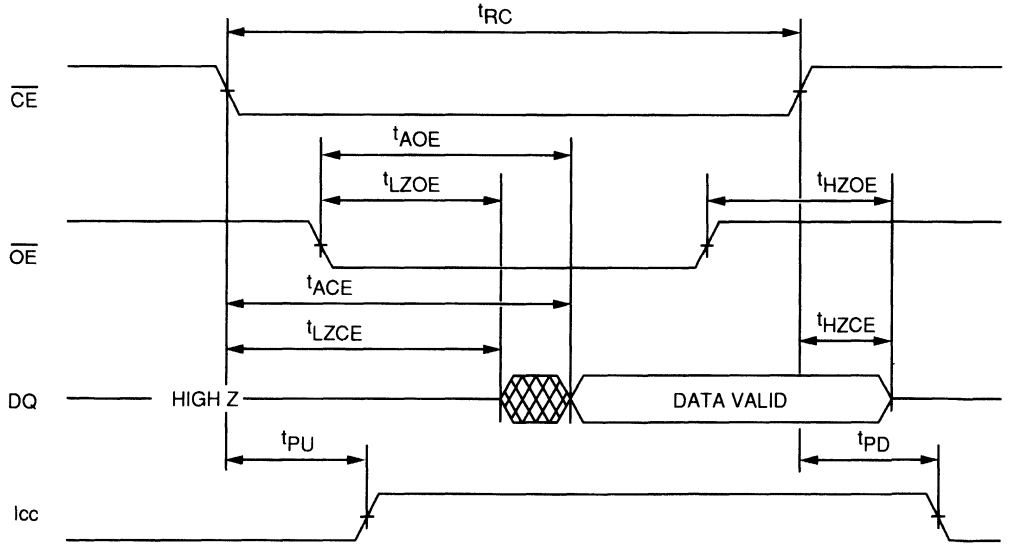
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 (NOTES 8, 9)



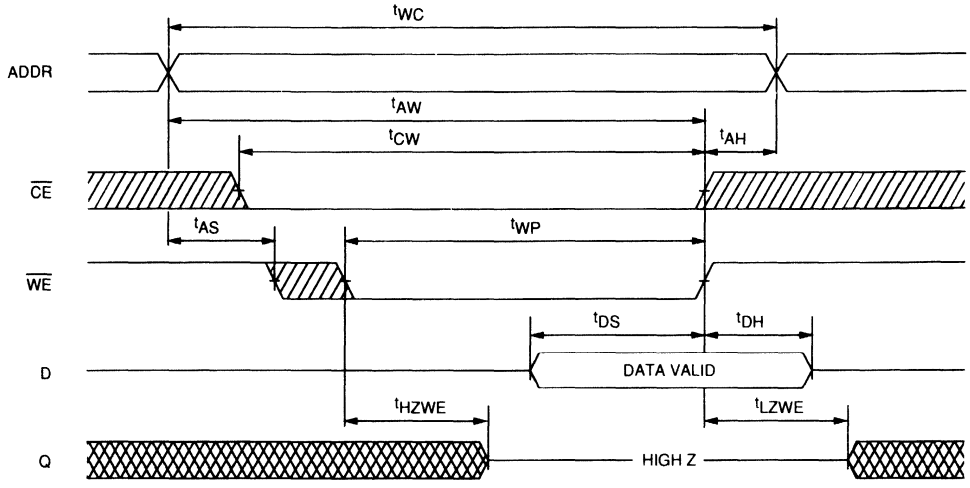
READ CYCLE NO. 2 (NOTES 7, 8, 10)



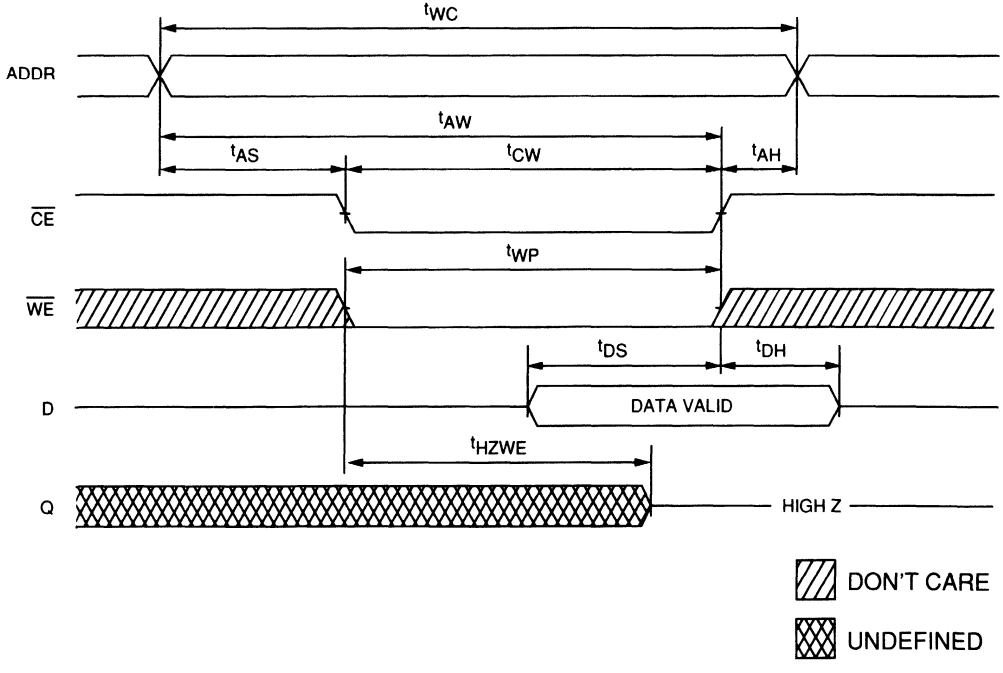
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



LATCHED SRAM

2K x 8 SRAM

WITH ADDRESS LATCH

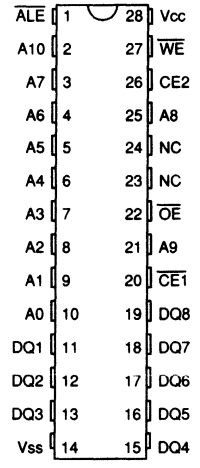
FEATURES

- Functionally compatible with Intel MCS-96 families of microcontrollers
- Eliminates the need for an external 74LS373 latch
- Low power, CMOS double metal process
- Single +5V (±10%) power supply
- Flexible memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

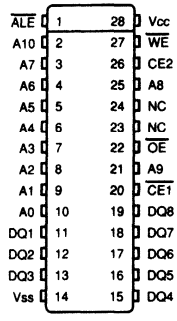
OPTIONS	MARKING
• Timing	
15ns access	-15
30ns access	-30
45ns access	-45
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC (28 pin)	EC
Ceramic LCC (32 pin)	ECW
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

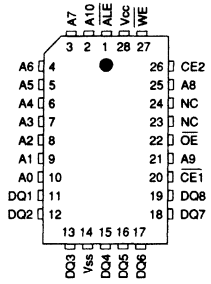
28L/DIP (PJ, CI)



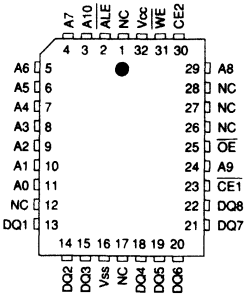
28L/ SOJ (DJC)



28L/LCC (ECF)



32L/LCC (ECH)



GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

Addresses are latched with a dedicated address latch enable ($\overline{ALE}$) pin. These transparent, on-board latches eliminate the need for an external address latch in multiplexed address/data bus applications typical in microcontroller based systems.

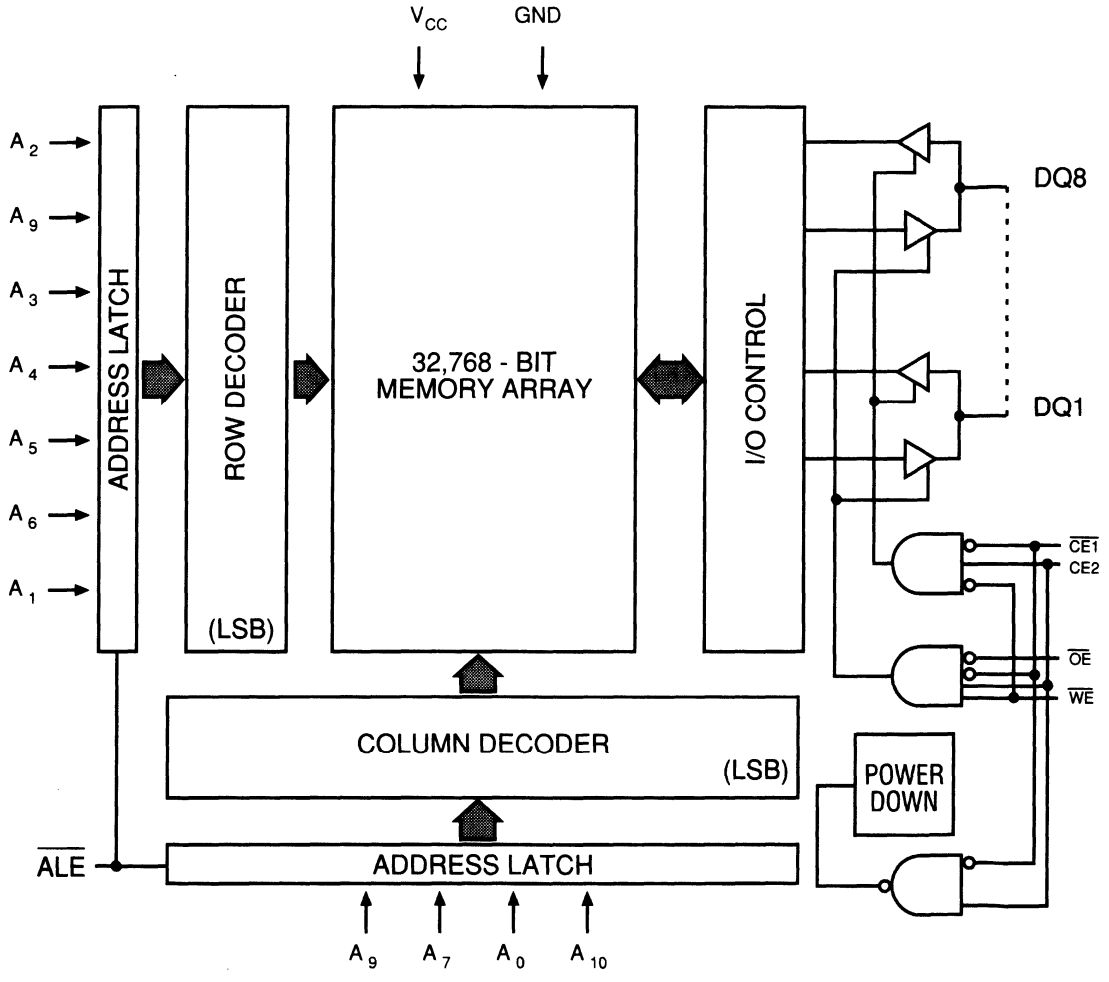
Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$, inputs are both LOW and CE2 is HIGH. Reading is accomplished when $\overline{WE}$ remains HIGH, $\overline{CE1}$ and $\overline{OE}$ go to LOW, and CE2 goes HIGH. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

For flexibility in high performance applications, Micron offers two chip enables. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Micron's latched 2K x 8 SRAM readily complements Intel's 87C257 latched 32K x 8 EPROM and 80C51 8-bit microcontroller and other similar microcontroller devices by providing additional memory capacity and latched addressing for complete embedded controller solutions.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{ALE}$	DQ OPERATION	POWER
STANDBY	H	X	X	X	X	HIGH Z	STANDBY
STANDBY	X	L	X	X	X	HIGH Z	STANDBY
READ	L	H	H	L	X	Q	ACTIVE
READ DISABLE	L	H	H	H	X	HIGH Z	ACTIVE
WRITE	L	H	L	X	X	D	ACTIVE

NOTE: The address latch is transparent when $\overline{ALE}$ is HIGH and the address is latched when $\overline{ALE}$ goes LOW.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, Vcc = 5.0V ± 10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX				
DESCRIPTION	CONDITIONS	SYMBOL	-15	-30	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, Vcc = Max., Outputs Open	I_{CC}	120	90	90	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, Vcc = Max	I_{SB1}	50	40	40	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, Vcc = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	Vcc = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	SYM	-15		-30		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle									
READ cycle time	t_{RC}	15		30		45		ns	
Address access time	t_{AA}		15		30		45	ns	11
Chip enable access time	t_{ACE}		15		30		45	ns	
Output hold from access change	t_{OH}	3		3		3		ns	
Chip enable to output in low Z	t_{LZCE}	5		5		5		ns	
Chip disable to output in high Z	t_{HZCE}		10		20		20	ns	6,7
Chip enable to power up time	t_{PU}	0		0		0		ns	
Chip disable to power down time	t_{PD}		15		30		45	ns	
Output enable access time	t_{AOE}		10		15		20	ns	
Output enable to output in low Z	t_{LZOE}	0		0		0		ns	
Output disable to output in high Z	t_{HZOE}		10		15		20	ns	6
WRITE Cycle									
WRITE cycle time	t_{WC}	15		30		45		ns	
Chip enable to end of write	t_{CW}	12		25		30		ns	
Address valid to end of write	t_{AW}	15		25		30		ns	
Address set-up time	t_{AS}	0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		ns	
Write pulse width	t_{WP}	12		25		30		ns	
Data set-up time	t_{DS}	10		15		20		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	0		0		0		ns	
Write enable to output in high Z	t_{HZWE}	0	10	0	12	0	20	ns	6
LATCH Characteristics									
Address setup time for latch enable	t_{LAS}	0		0		0		ns	
Address hold from latch enable	t_{LAH}	8		10		15		ns	
Latch deselect width	t_{LPW}	6		10		15		ns	
$\overline{ALE}$ to output enable LOW	t_{LOE}	0		0		0		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

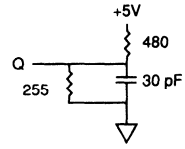


Fig. 1 OUTPUT LOAD EQUIVALENT

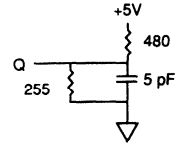


Fig. 2 OUTPUT LOAD EQUIVALENT

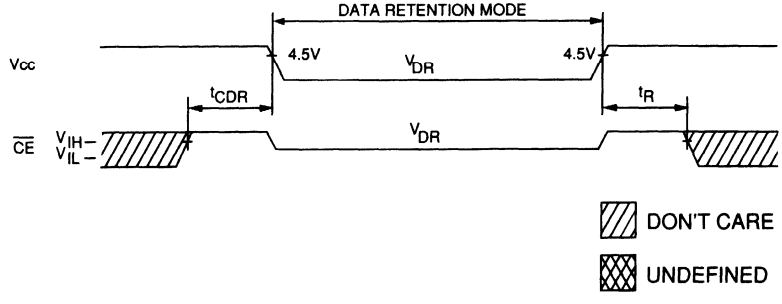
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Address valid prior to or coincident with latest occurring chip enable and the falling edge of $\overline{ALE}$.
10. ^{t}RC = Read Cycle Time.
11. Assume ^{t}LOE and ^{t}LAS operating at MIN limits. If ^{t}LAS, ^{t}LOE + ^{t}AOE > ^{t}AA, then access time is determined by the sum. $\overline{CE}$ and CE2 are active.

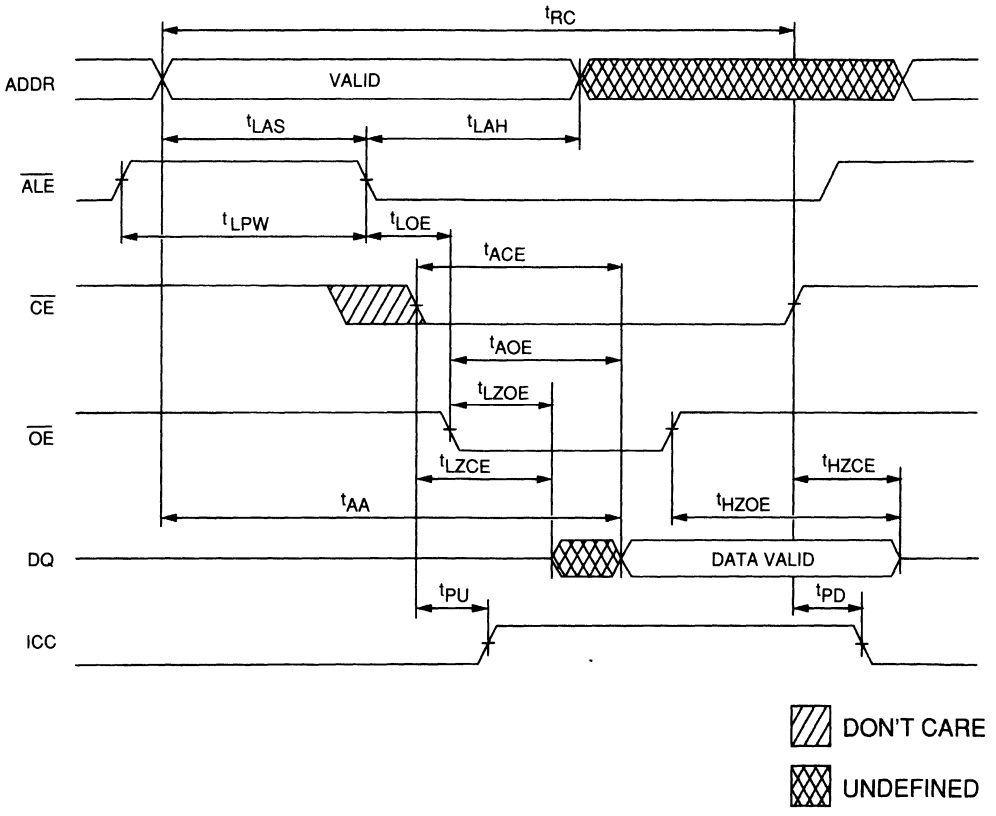
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	ICCDR		95	500	µA	
		Vcc=3v			350	750	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 10

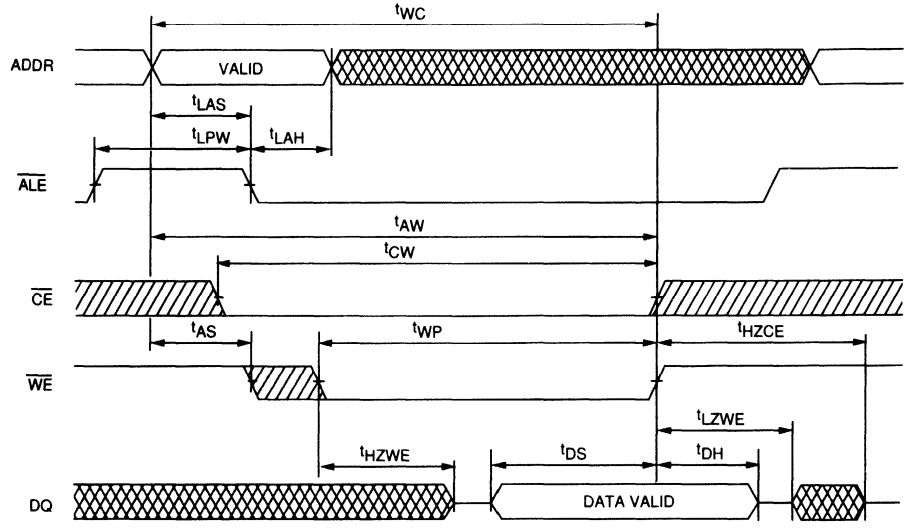
LOW Vcc DATA RETENTION WAVEFORM



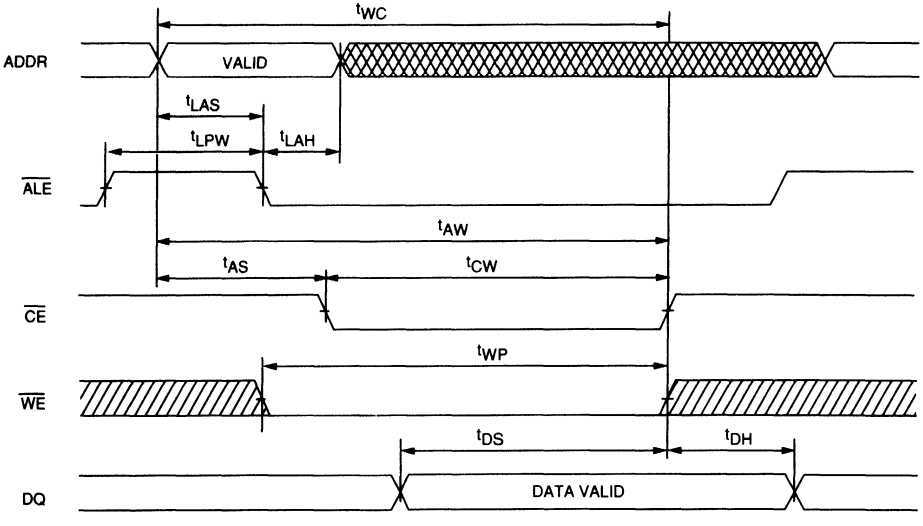
READ CYCLE (NOTES 8, 9)

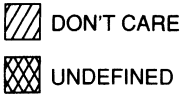


WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)





SRAM 4K x 4 SRAM

FEATURES

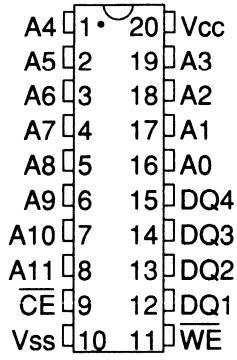
- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

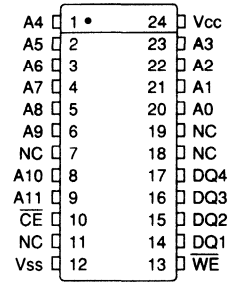
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

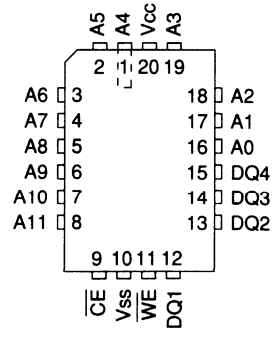
20L/300 DIP
(PE, CD)



24L/300 SOJ
(DJB)



20L/LCC
(ECC)



GENERAL DESCRIPTION

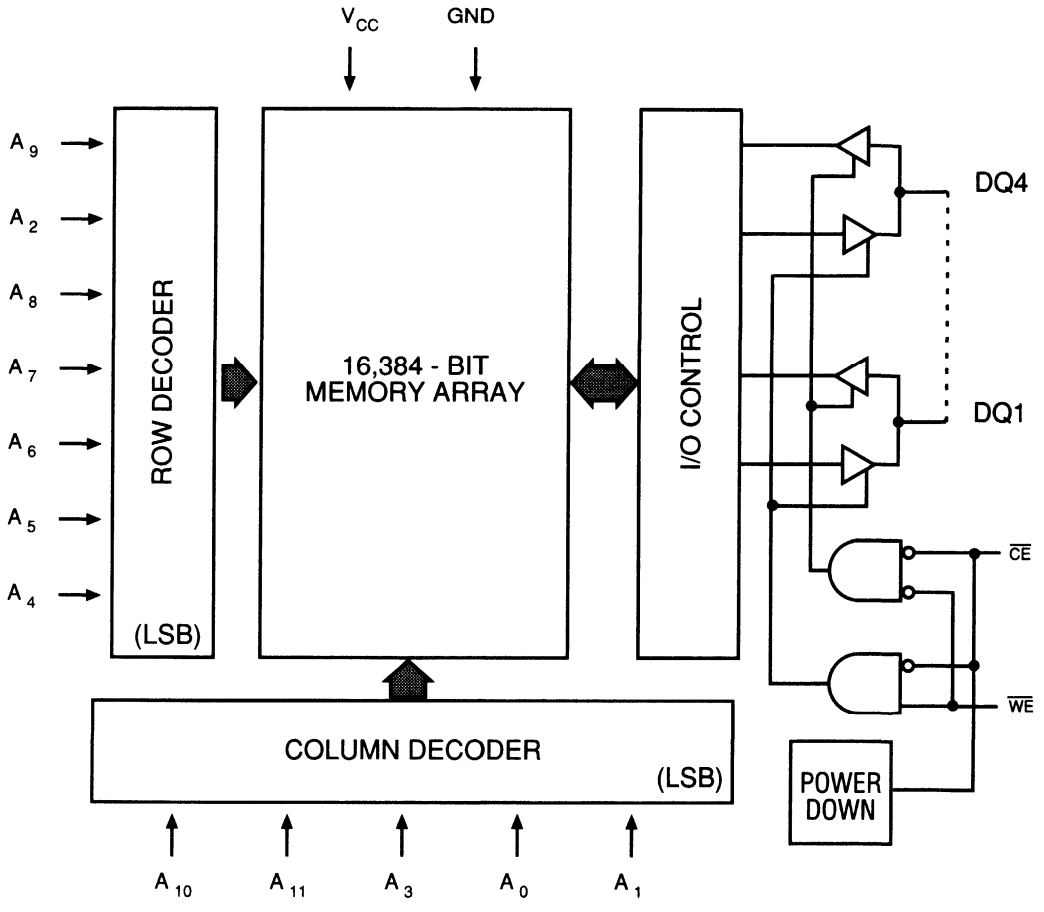
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	125	110	100	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	50	45	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	3	3	3	3	3	3	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip enable access time	^tACE		11		12		15		20		25		30	ns	
Output hold from access change	^tOH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	^tLZCE	3		3		5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		7		7		10		10		15		20	ns	6,7
Chip enable to power up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power down time	^tPD		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip enable to end of write	^tCW	10		12		15		20		25		25		ns	
Address valid to end of write	^tAW	12		12		15		20		25		25		ns	
Address set-up time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data set-up time	^tDS	7		8		10		10		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in low Z	^tLZWE	2		2		2		2		2		2		ns	
Write enable to output in high Z	^tHZWE	0	6	0	6	0	8	0	10	0	12	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

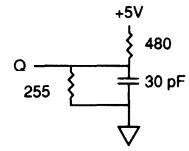


Fig. 1 OUTPUT LOAD EQUIVALENT

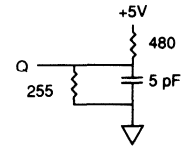


Fig. 2 OUTPUT LOAD EQUIVALENT

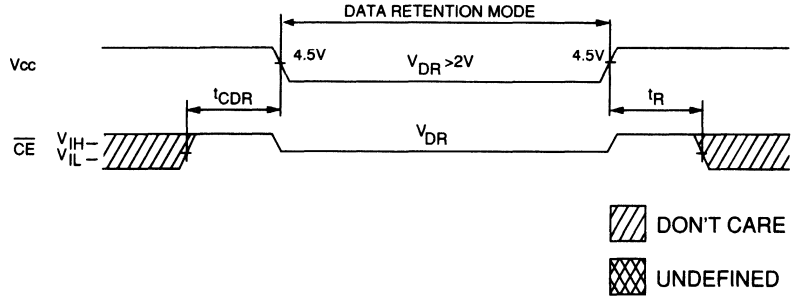
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.

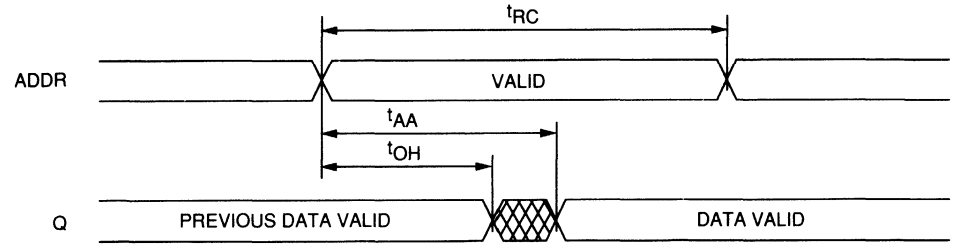
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	I_{CCDR}		95	500	µA	
		Vcc=3v			350	750	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 10

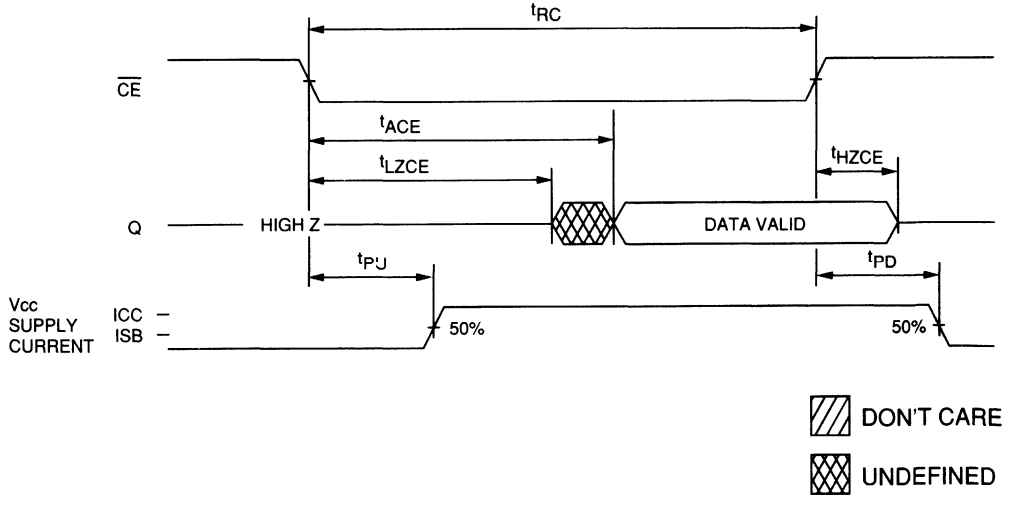
LOW Vcc DATA RETENTION WAVEFORM



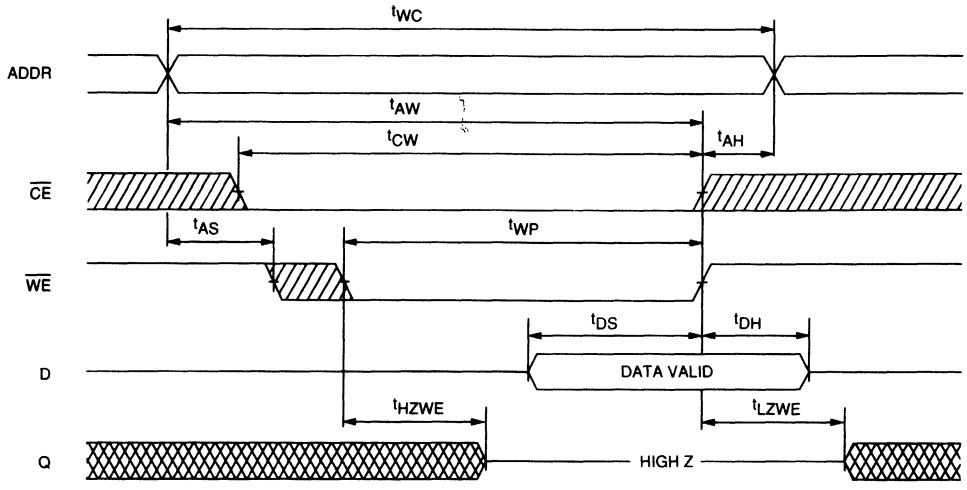
READ CYCLE NO. 1 (NOTES 8, 9)



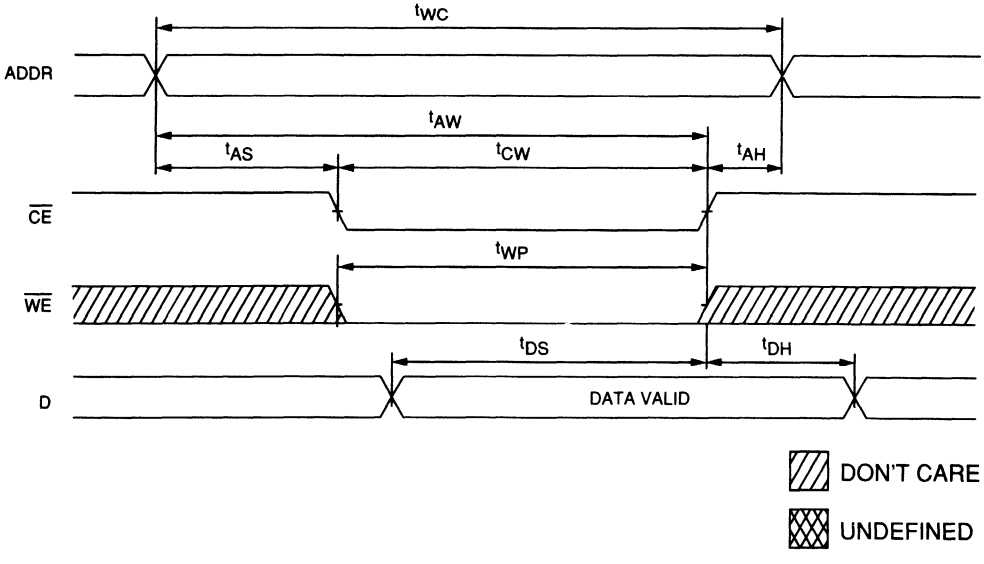
READ CYCLE NO. 2 (NOTES 7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



SRAM

4K x 4 SRAM

WITH OUTPUT ENABLE

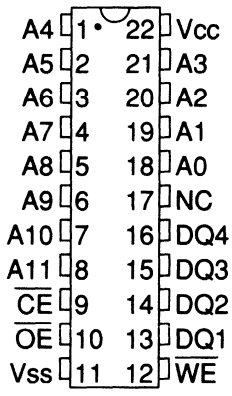
FEATURES

- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

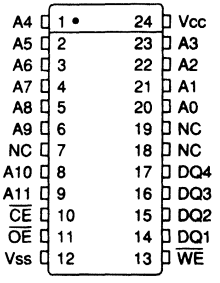
OPTIONS	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

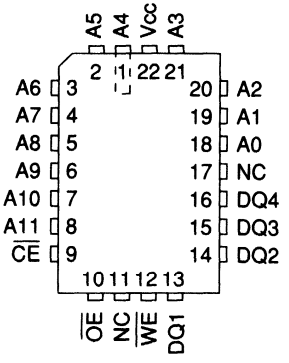
22L/300DIP (PF, CE)



24L/300 SOJ (DJB)



22L/LCC (ECE)



GENERAL DESCRIPTION

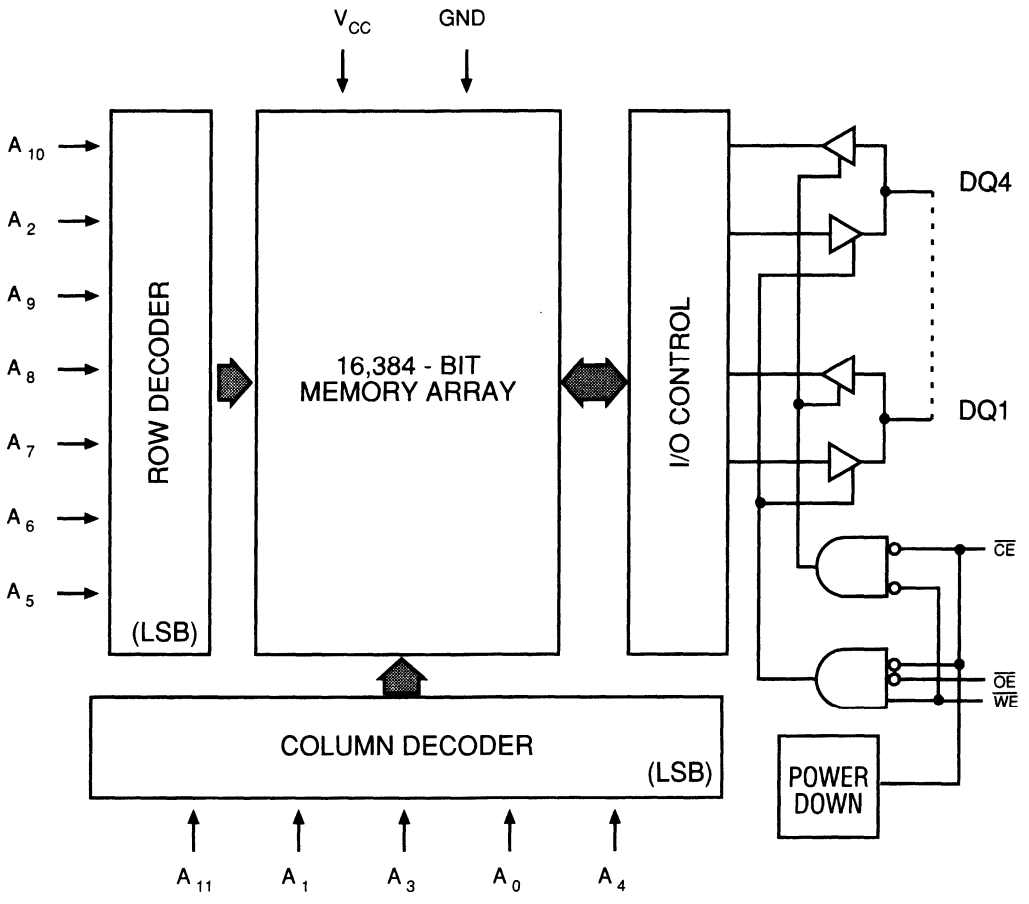
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	125	110	100	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	50	45	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	3	3	3	3	3	3	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C, Vcc = 5V ± 10%)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^tRC	12		15		20		25		30		35		ns	
Address access time	^tAA		12		15		20		25		30		35	ns	
Chip enable access time	^tACE		11		12		15		20		25		30	ns	
Output hold from access change	^tOH	3		3		3		3		3		3		ns	
Chip enable to output in low Z	^tLZCE	3		3		5		5		5		5		ns	
Chip disable to output in high Z	^tHZCE		7		7		10		10		15		20	ns	6,7
Chip enable to power up time	^tPU	0		0		0		0		0		0		ns	
Chip disable to power down time	^tPD		12		15		20		25		30		35	ns	
Output enable access time	^tAOE		7		7		9		10		15		20	ns	
Output enable to output in low Z	^tLZOE	0		0		0		0		0		0		ns	
Output disable to output in high Z	^tHZOE		6		6		10		10		15		20	ns	6
WRITE Cycle															
WRITE cycle time	^tWC	12		15		20		25		30		35		ns	
Chip enable to end of write	^tCW	10		12		15		20		25		25		ns	
Address valid to end of write	^tAW	12		12		15		20		25		25		ns	
Address set-up time	^tAS	0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		ns	
Write pulse width	^tWP	10		12		15		20		25		25		ns	
Data set-up time	^tDS	7		8		10		10		15		15		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in low Z	^tLZWE	2		2		2		2		2		2		ns	
Write enable to output in high Z	^tHZWE	0	6	0	6	0	8	0	10	0	12	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

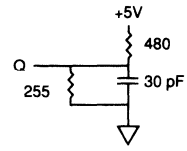


Fig. 1 OUTPUT LOAD EQUIVALENT

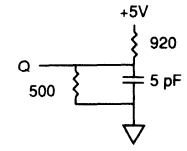


Fig. 2 OUTPUT LOAD EQUIVALENT

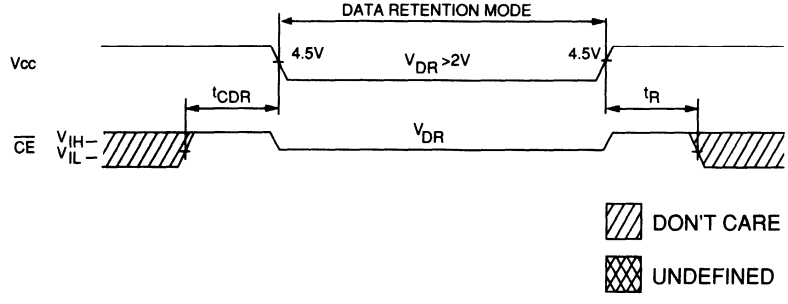
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.

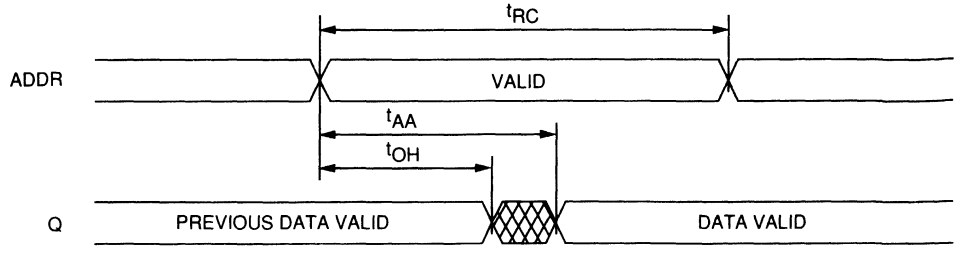
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	ICCDR		95	500	µA	
		Vcc=3v			350	750	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

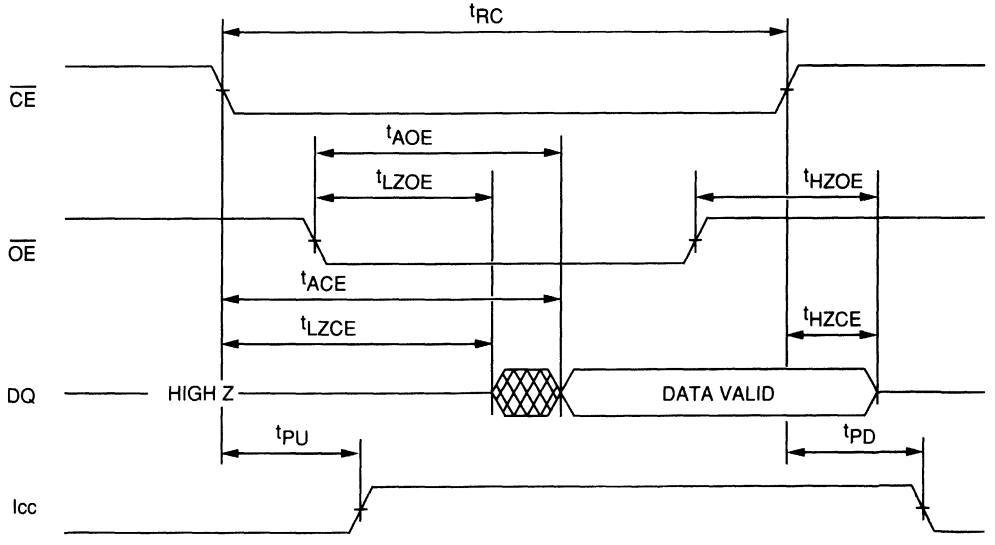
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 (NOTES 8, 9)



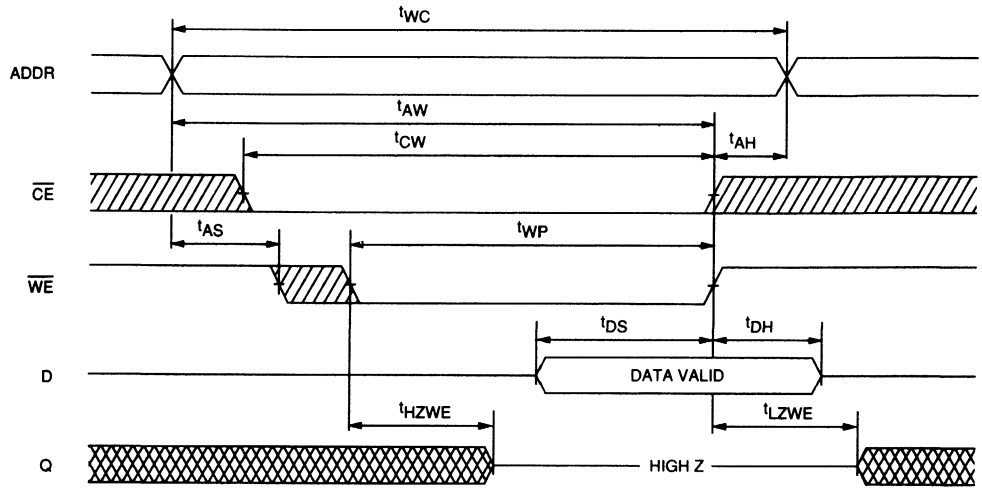
READ CYCLE NO. 2 (NOTES 7, 8, 10)



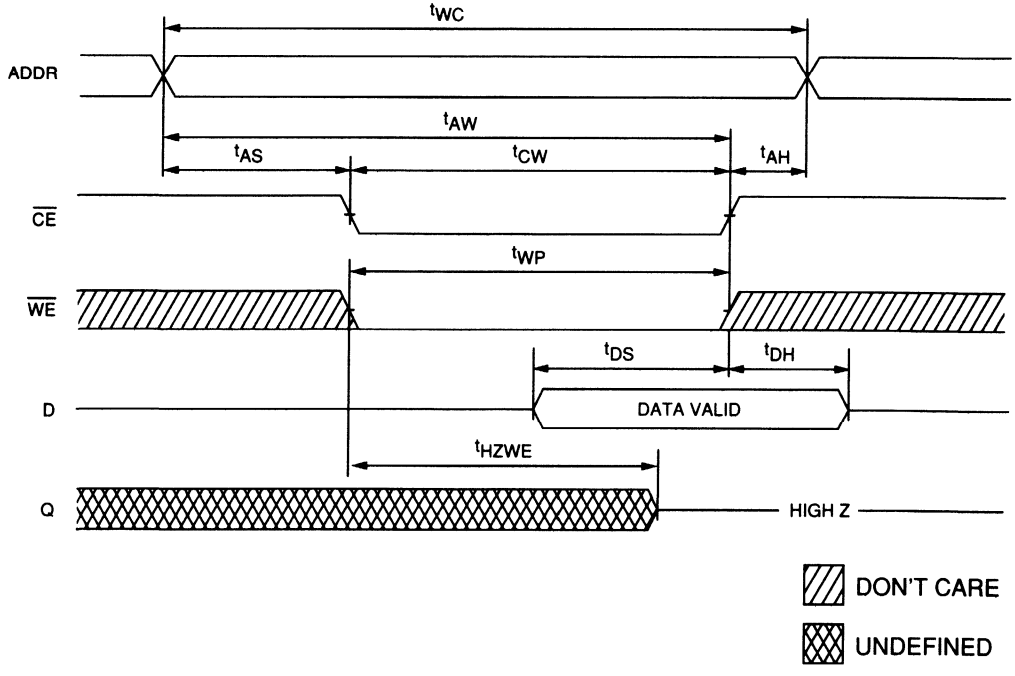
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



SRAM

4K x 4 SRAM

WITH SEPARATE INPUTS AND OUTPUTS

FEATURES

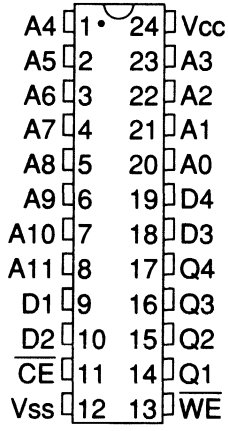
- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible
- MT5C1606 – output tracks input during WRITE
- MT5C1607 – output high impedance during WRITE

OPTIONS

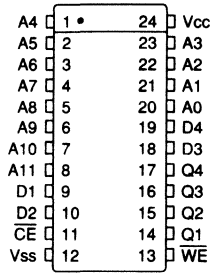
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

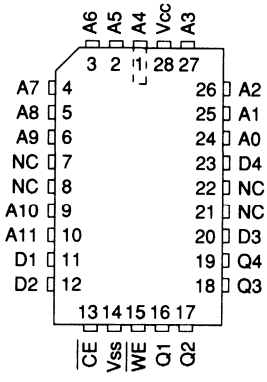
24L/300DIP
(PG, CG)



24L/300 SOJ
(DJB)



28L/LCC
(ECF)



GENERAL DESCRIPTION

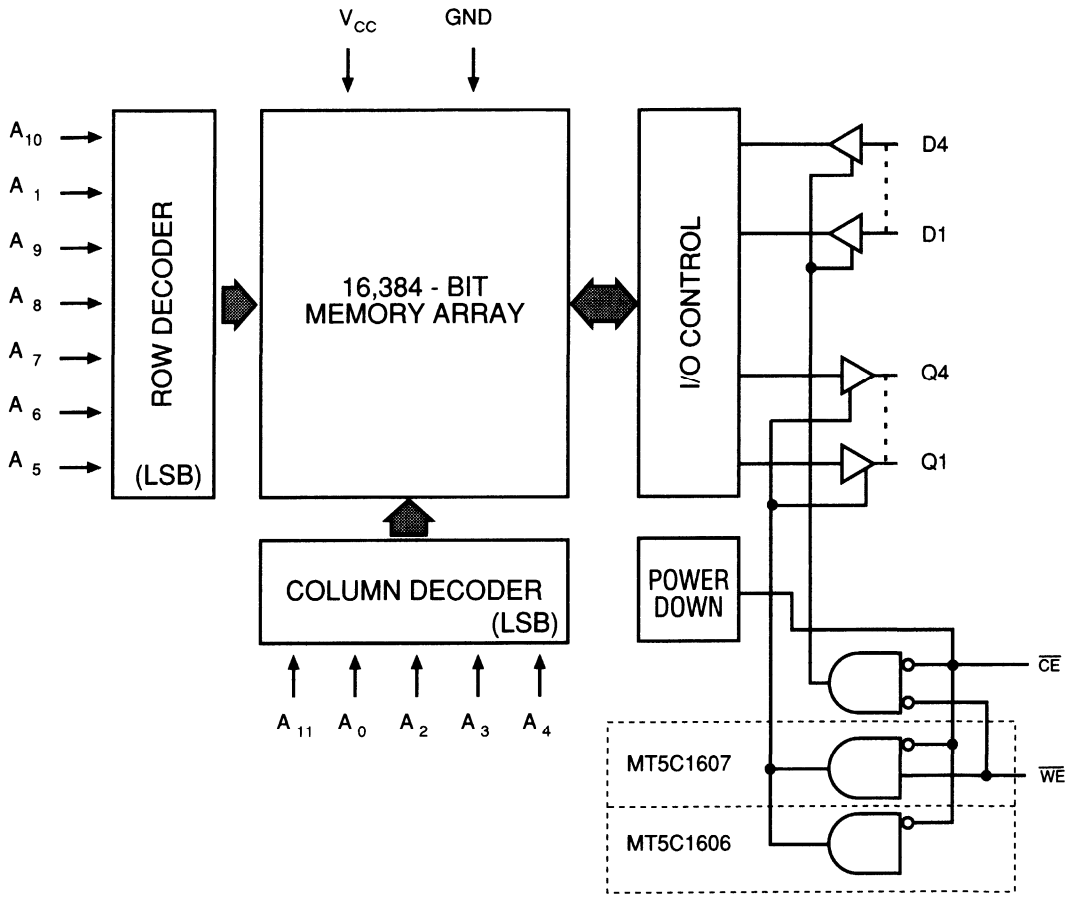
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 4 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE (1)	L	L	HIGH Z	ACTIVE
WRITE (2)	L	L	D	ACTIVE

NOTES: 1. MT5C1607 ONLY
2. MT5C1606 ONLY

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	125	110	100	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	50	45	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	3	3	3	3	3	3	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	t_{RC}	12		15		20		25		30		35		ns	
Address access time	t_{AA}		12		15		20		25		30		35	ns	
Chip enable access time	t_{ACE}		11		12		15		20		25		30	ns	
Output hold from access change	t_{OH}	3		3		3		3		3		3		ns	
Chip enable to output in low Z	t_{LZCE}	3		3		5		5		5		5		ns	
Chip disable to output in high Z	t_{HZCE}		7		7		10		10		15		20	ns	6,7
Chip enable to power up time	t_{PU}	0		0		0		0		0		0		ns	
Chip disable to power down time	t_{PD}		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	t_{WC}	12		15		20		25		30		35		ns	
Chip enable to end of write	t_{CW}	10		12		15		20		25		25		ns	
Address valid to end of write	t_{AW}	12		12		15		20		25		25		ns	
Address set-up time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns	
Write pulse width	t_{WP}	10		12		15		20		25		25		ns	
Data set-up time	t_{DS}	7		8		10		10		15		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	2		2		2		2		2		2		ns	
Write enable to output in high Z	t_{HZWE}	0	6	0	6	0	8	0	10	0	12	0	15	ns	
Write enable to output valid	t_{AWE}		12		15		20		25		30		35	ns	
Data valid to output valid	t_{ADV}		12		15		20		25		30		35	ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

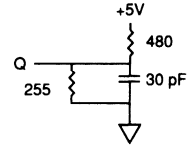


Fig. 1 OUTPUT LOAD EQUIVALENT

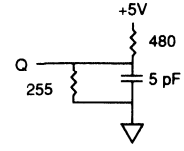


Fig. 2 OUTPUT LOAD EQUIVALENT

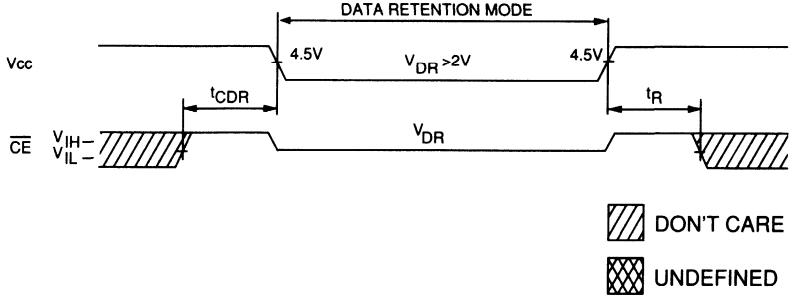
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.

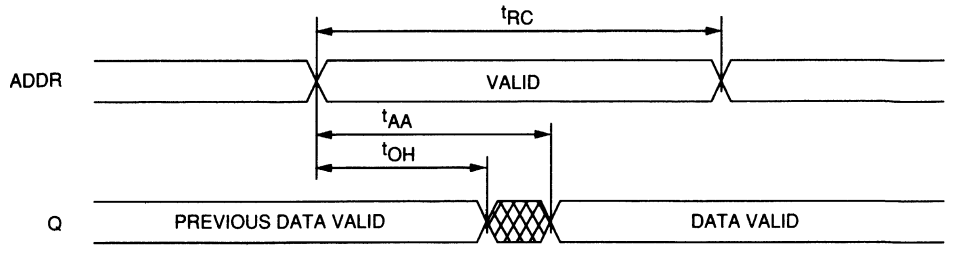
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	ICCDR		95	500	µA	
		Vcc=3v			350	750	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

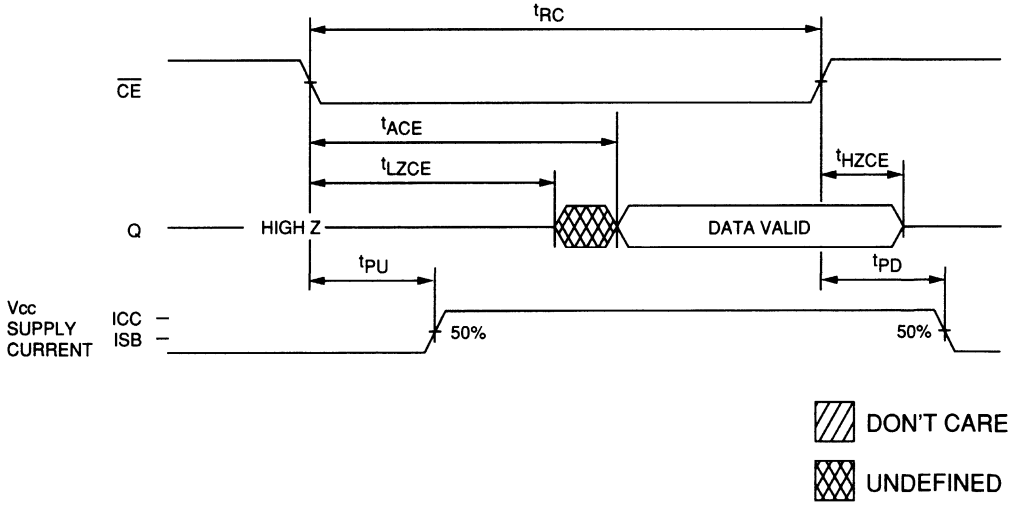
LOW Vcc DATA RETENTION WAVEFORM



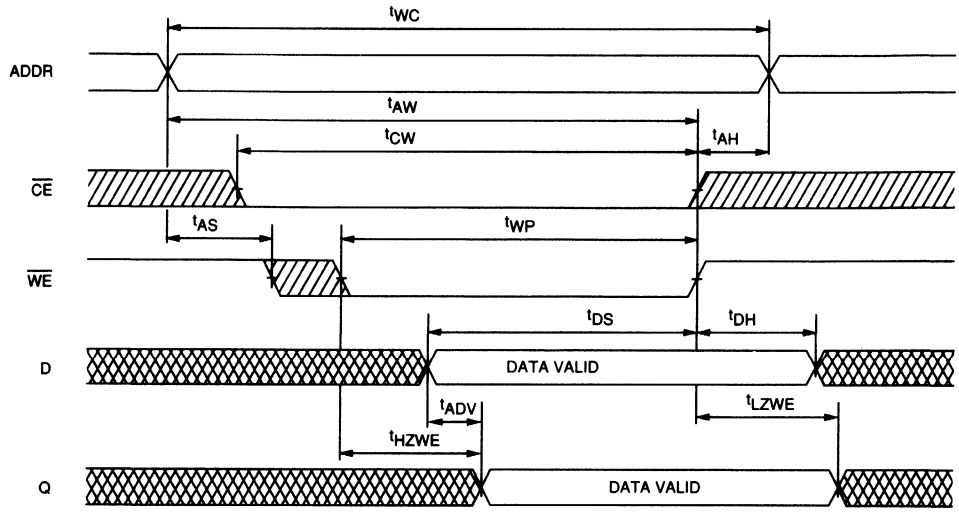
READ CYCLE NO. 1 (NOTES 8, 9)



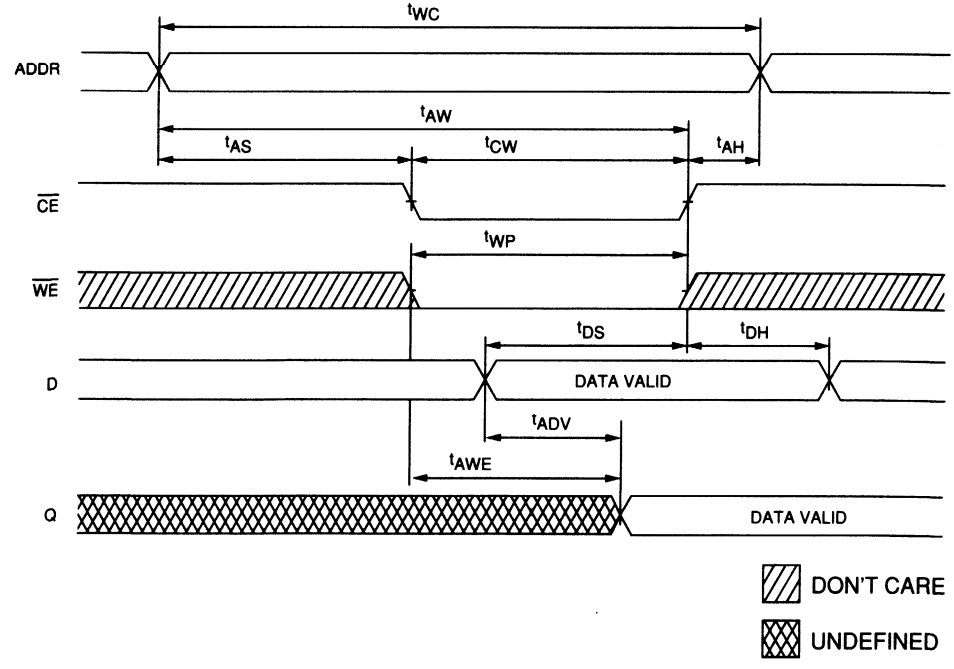
READ CYCLE NO. 2 (NOTES 7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



SRAM

8K x 8 SRAM

FEATURES

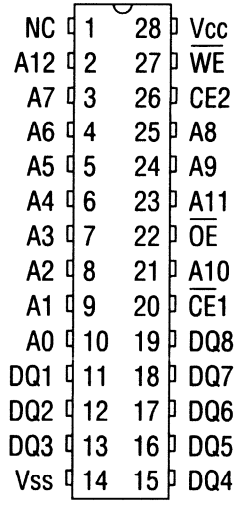
- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$1, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS

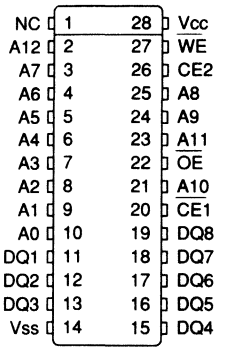
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC (28 pin)	EC
Ceramic LCC (32 pin)	ECW
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

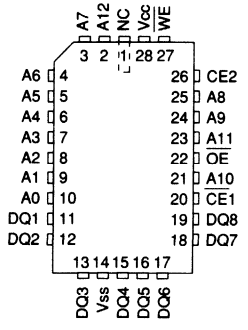
28L/300 DIP
(PJ, CI)



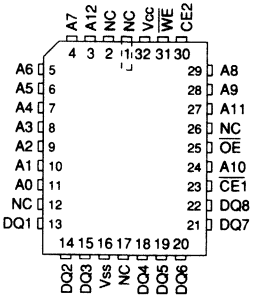
28L/300 SOJ
(DJC)



28L/LCC
(ECF)



32L/LCC
(ECH)



GENERAL DESCRIPTION

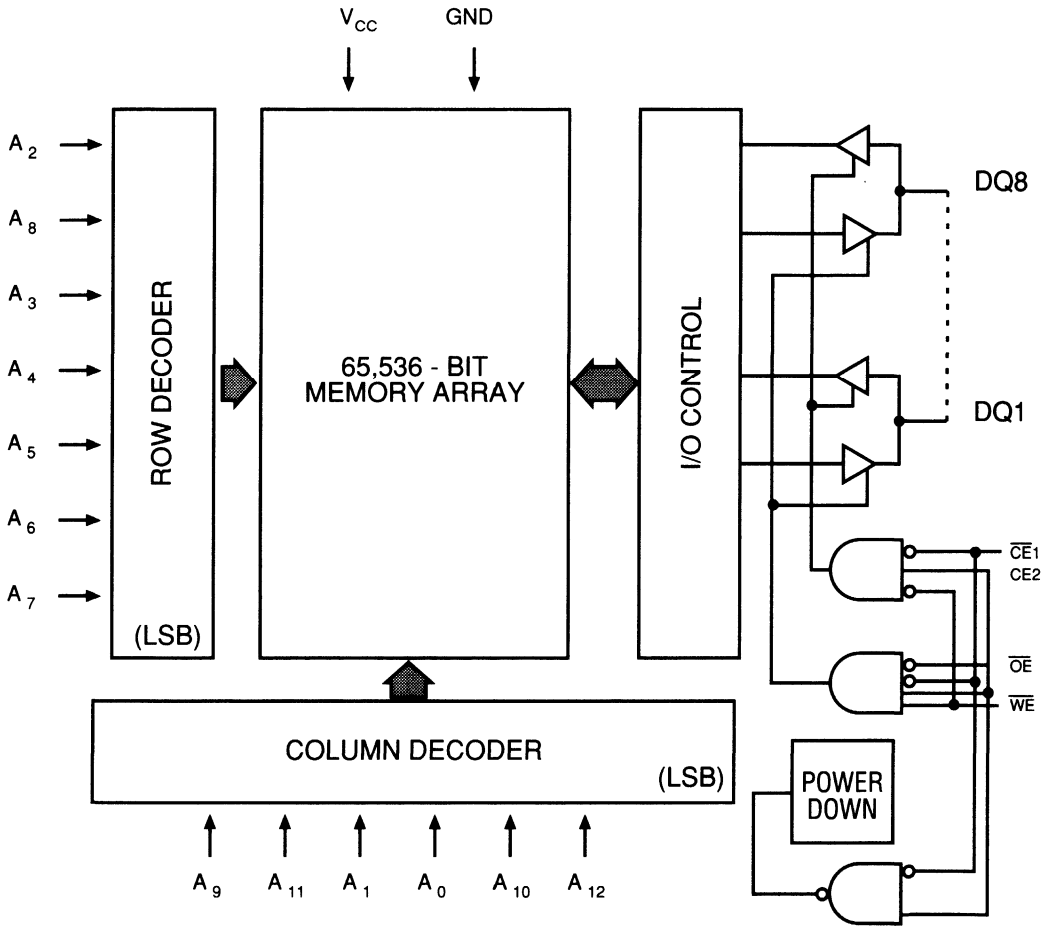
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers two chip enables on the x 8 organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	DQ OPERATION	POWER
STANDBY	H	X	X	X	HIGH Z	STANDBY
STANDBY	X	L	X	X	HIGH Z	STANDBY
READ	L	H	H	L	Q	ACTIVE
READ	L	H	H	H	HIGH Z	ACTIVE
WRITE	L	H	L	X	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, Vcc = Max., Outputs Open	Icc	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, Vcc = Max	I_{SB1}	60	50	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, Vcc = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz Vcc = 5V	Ci		7	pF	4
Output Capacitance		Co		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C, Vcc = 5V ± 10%)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	t_{RC}	12		15		20		25		30		35		ns	
Address access time	t_{AA}		12		15		20		25		30		35	ns	
Chip enable access time	t_{ACE}		12		12		15		20		25		30	ns	
Output hold from access change	t_{OH}	3		3		3		3		3		3		ns	
Chip enable to output in low Z	t_{LZCE}	3		3		5		5		5		5		ns	
Chip disable to output in high Z	t_{HZCE}		7		7		10		10		15		20	ns	6,7
Chip enable to power up time	t_{PU}	0		0		0		0		0		0		ns	
Chip disable to power down time	t_{PD}		12		15		20		25		30		35	ns	
Output enable access time	t_{AOE}		7		7		9		10		15		20	ns	
Output enable to output in low Z	t_{LZOE}	0		0		0		0		0		0		ns	
Output disable to output in high Z	t_{HZOE}		6		6		10		10		15		20	ns	6
WRITE Cycle															
WRITE cycle time	t_{WC}	12		15		20		25		30		35		ns	
Chip enable to end of write	t_{CW}	10		12		15		20		25		25		ns	
Address valid to end of write	t_{AW}	12		12		15		20		25		25		ns	
Address set-up time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns	
Write pulse width	t_{WP}	10		12		15		20		25		25		ns	
Data set-up time	t_{DS}	8		8		10		10		15		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	2		2		2		2		2		2		ns	
Write enable to output in high Z	t_{HZWE}	0	6	0	6	0	8	0	10	0	12	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

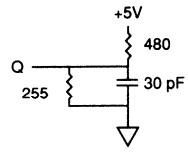


Fig. 1 OUTPUT LOAD EQUIVALENT

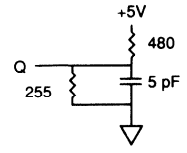


Fig. 2 OUTPUT LOAD EQUIVALENT

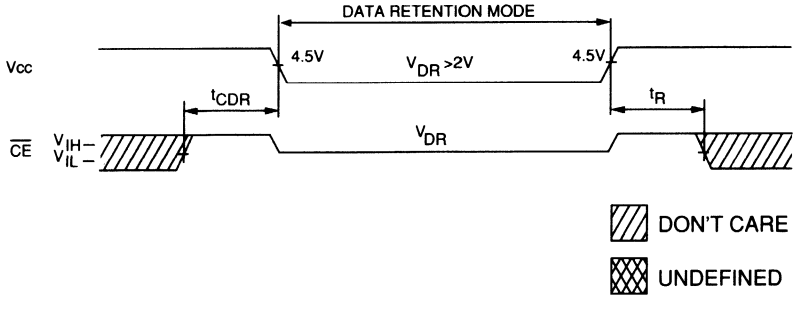
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.

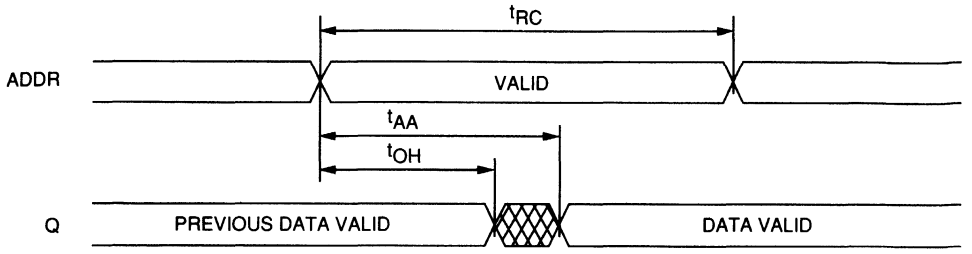
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	I_{CCDR}		95	500	µA	
		Vcc=3v			350	750	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

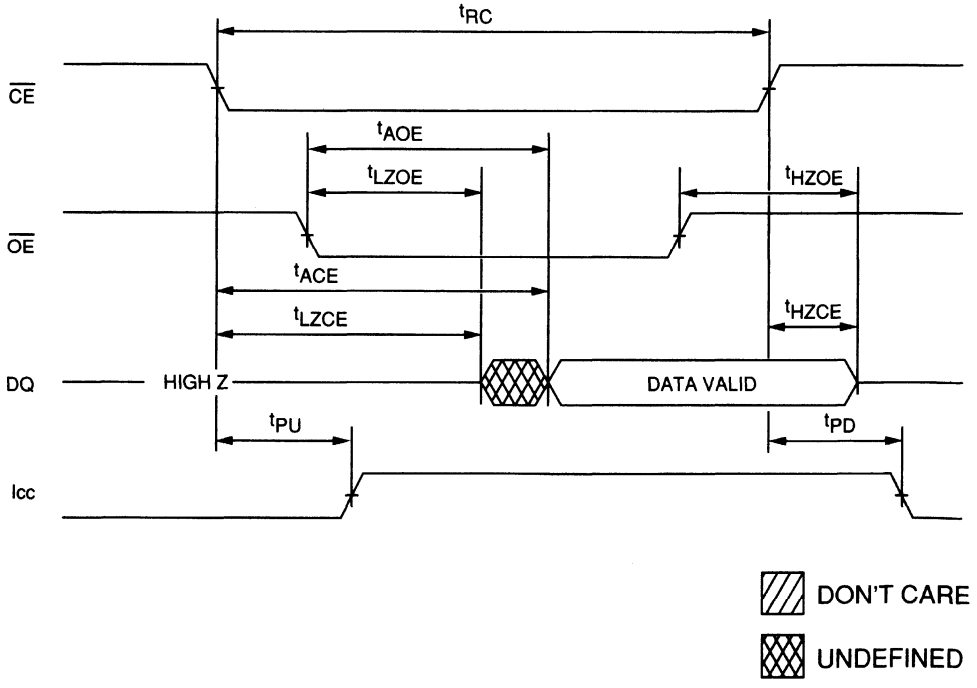
LOW Vcc DATA RETENTION WAVEFORM



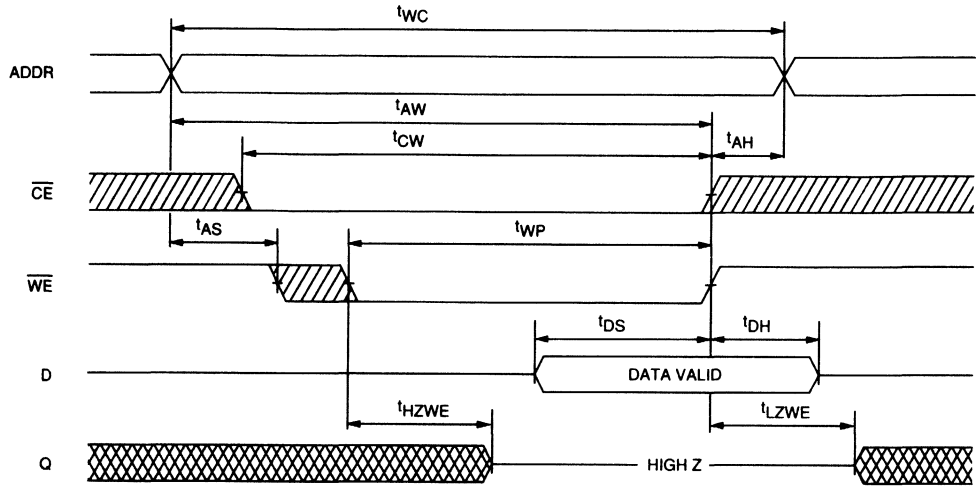
READ CYCLE NO. 1 (NOTES 8, 9)



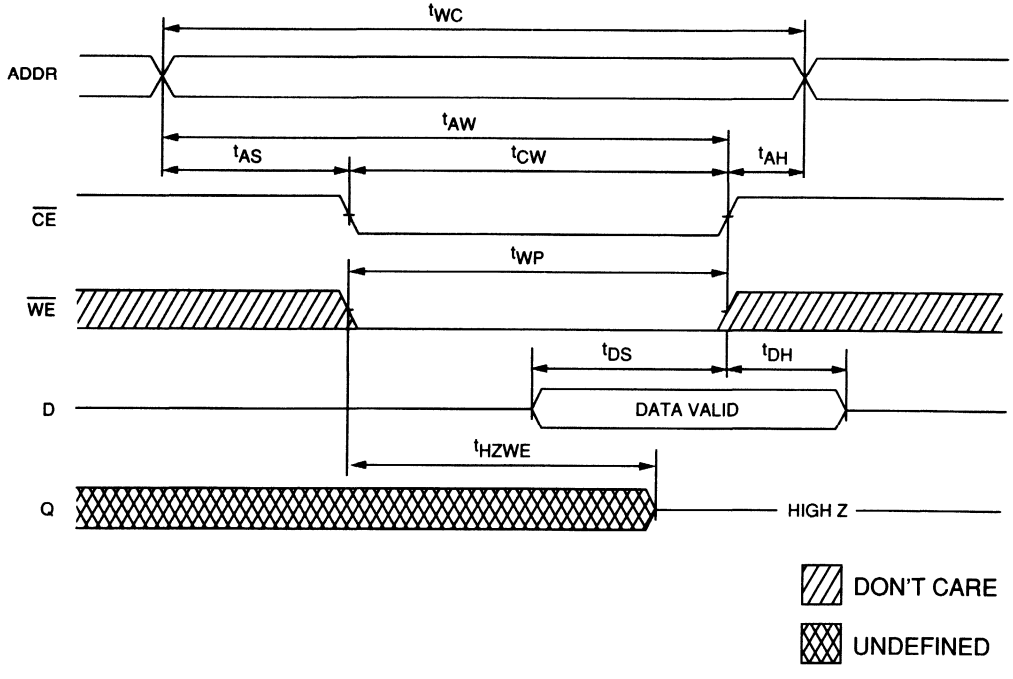
READ CYCLE NO. 2 (NOTES 7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



SRAM 16K x 1 SRAM

FEATURES

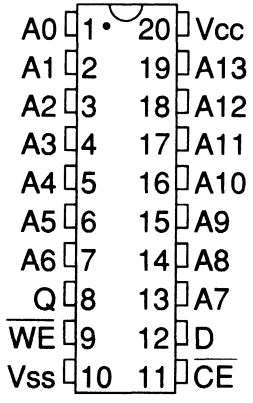
- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

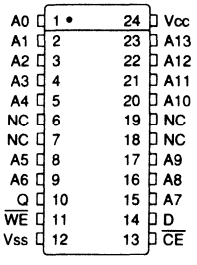
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

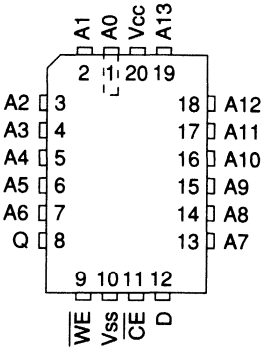
20L/300 DIP
(PD, CD)



24L/300 SOJ
(DJB)



20L/LCC
(ECC)



GENERAL DESCRIPTION

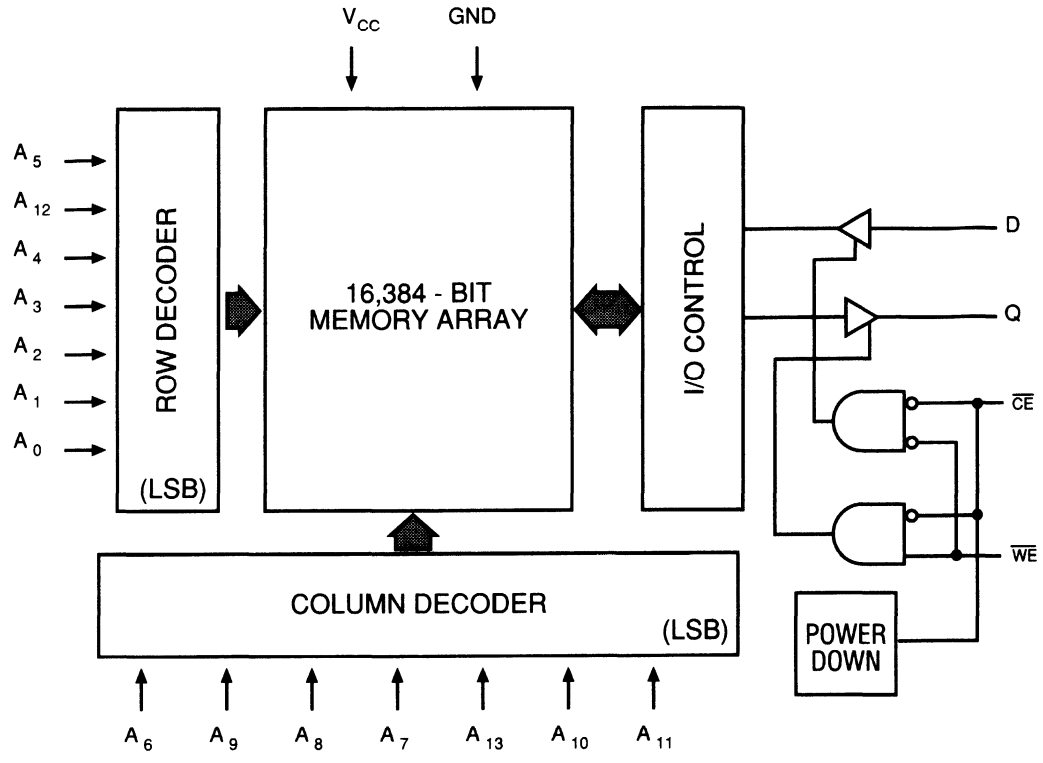
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	125	110	100	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	50	45	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	3	3	3	3	3	3	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C, Vcc = 5V ± 10%)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	t_{RC}	12		15		20		25		30		35		ns	
Address access time	t_{AA}		12		15		20		25		30		35	ns	
Chip enable access time	t_{ACE}		11		12		15		20		25		30	ns	
Output hold from access change	t_{OH}	3		3		3		3		3		3		ns	
Chip enable to output in low Z	t_{LZCE}	3		3		5		5		5		5		ns	
Chip disable to output in high Z	t_{HZCE}		7		7		10		10		15		20	ns	6,7
Chip enable to power up time	t_{PU}	0		0		0		0		0		0		ns	
Chip disable to power down time	t_{PD}		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	t_{WC}	12		15		20		25		30		35		ns	
Chip enable to end of write	t_{CW}	10		12		15		20		25		25		ns	
Address valid to end of write	t_{AW}	12		12		15		20		25		25		ns	
Address set-up time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns	
Write pulse width	t_{WP}	10		12		15		20		25		25		ns	
Data set-up time	t_{DS}	7		8		10		10		15		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	2		2		2		2		2		2		ns	
Write enable to output in high Z	t_{HZWE}	0	6	0	6	0	8	0	10	0	12	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

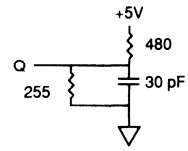


Fig. 1 OUTPUT LOAD EQUIVALENT

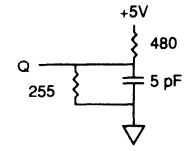


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

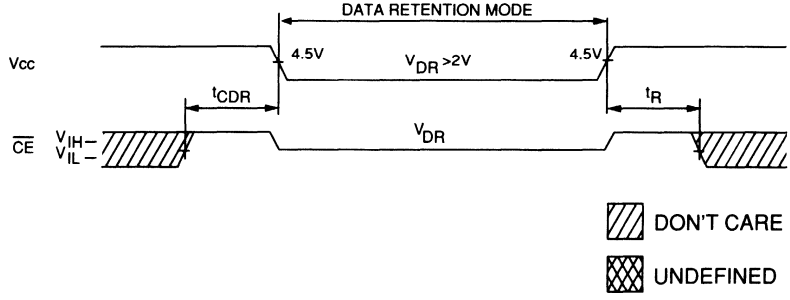
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.

FAST SRAM

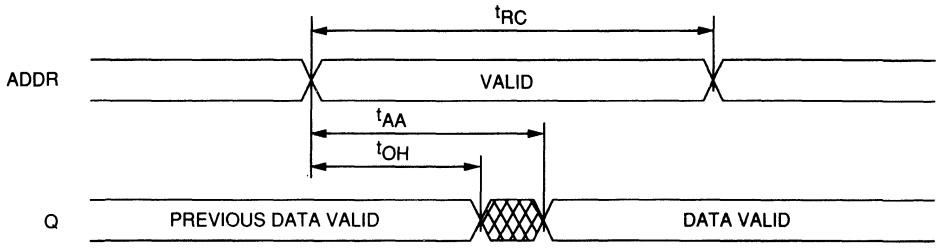
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	I_{CCDR}		95	500	µA	
		Vcc=3v			350	750	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

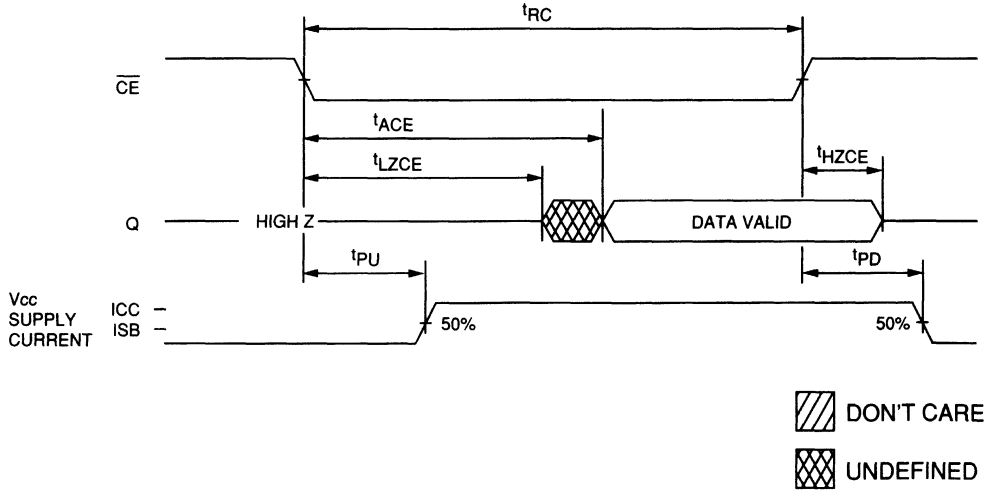
LOW Vcc DATA RETENTION WAVEFORM



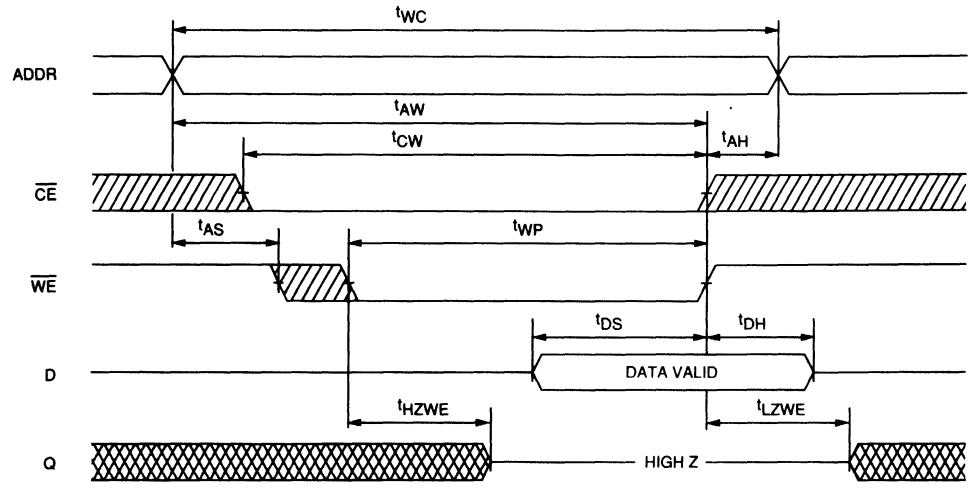
READ CYCLE NO. 1 (NOTES 8, 9)



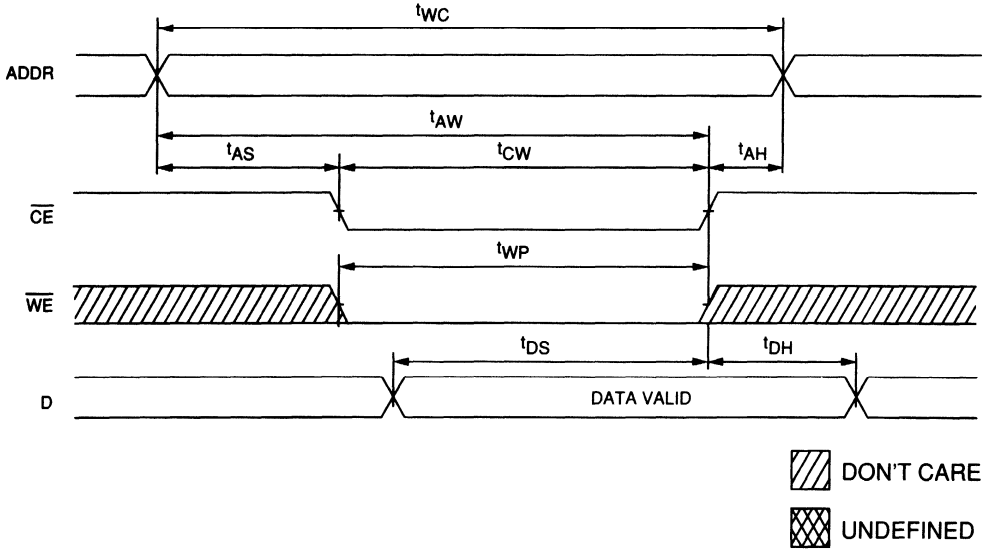
READ CYCLE NO. 2 (NOTES 7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



SRAM 16K x 4 SRAM

FEATURES

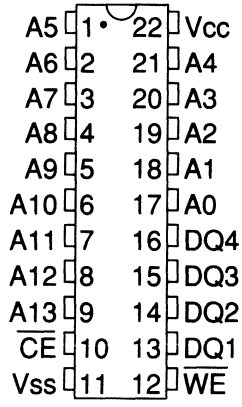
- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

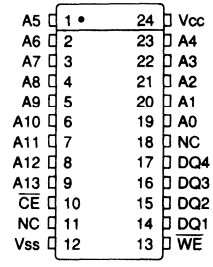
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

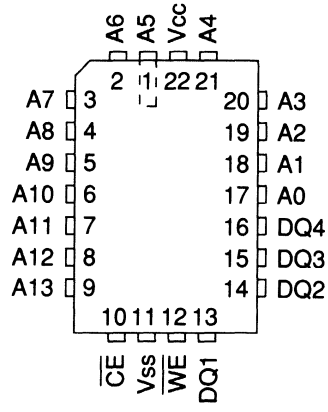
22L/300 DIP (PF, CF)



24L/300 SOJ (DJB)



22L/LCC (ECE)



GENERAL DESCRIPTION

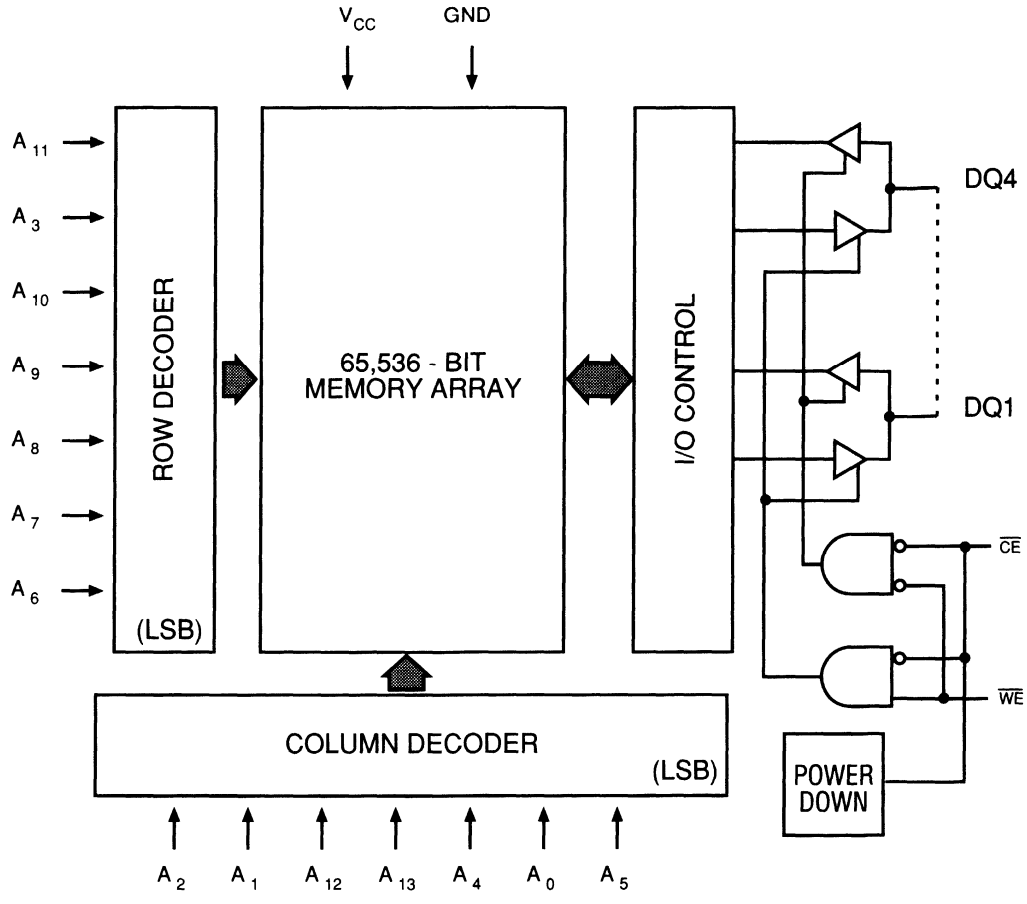
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	DIN	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	60	50	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	t_{RC}	12		15		20		25		30		35		ns	
Address access time	t_{AA}		12		15		20		25		30		35	ns	
Chip enable access time	t_{ACE}		12		12		15		20		25		30	ns	
Output hold from access change	t_{OH}	3		3		3		3		3		3		ns	
Chip enable to output in low Z	t_{LZCE}	3		3		5		5		5		5		ns	
Chip disable to output in high Z	t_{HZCE}		7		7		10		10		15		20	ns	6,7
Chip enable to power up time	t_{PU}	0		0		0		0		0		0		ns	
Chip disable to power down time	t_{PD}		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	t_{WC}	12		15		20		25		30		35		ns	
Chip enable to end of write	t_{CW}	10		12		15		20		25		25		ns	
Address valid to end of write	t_{AW}	12		12		15		20		25		25		ns	
Address set-up time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns	
Write pulse width	t_{WP}	10		12		15		20		25		25		ns	
Data set-up time	t_{DS}	8		8		10		10		15		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	2		2		2		2		2		2		ns	
Write enable to output in high Z	t_{HZWE}	0	6	0	6	0	8	0	10	0	12	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

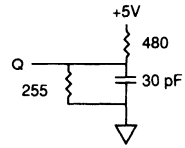


Fig. 1 OUTPUT LOAD EQUIVALENT

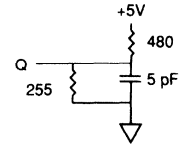


Fig. 2 OUTPUT LOAD EQUIVALENT

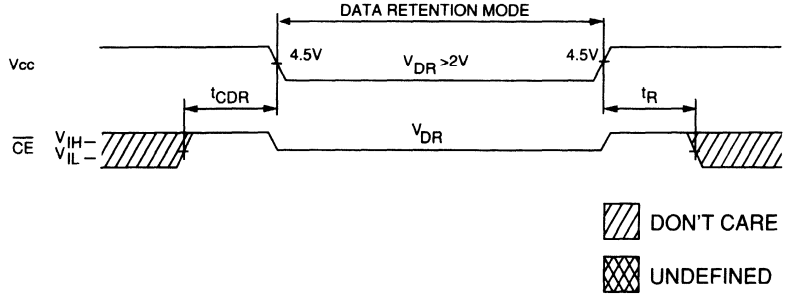
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.

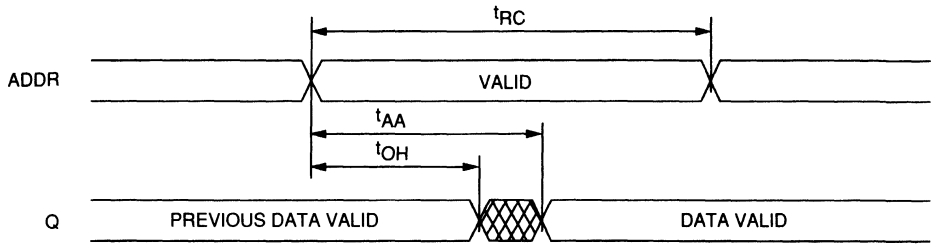
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	ICCDR		95	500	µA	
		Vcc=3v			350	750	µA	
Chip Deselect to Data Retention Time			tCDR	0		—	ns	4
Operation Recovery Time			tR	tRC			ns	4, 11

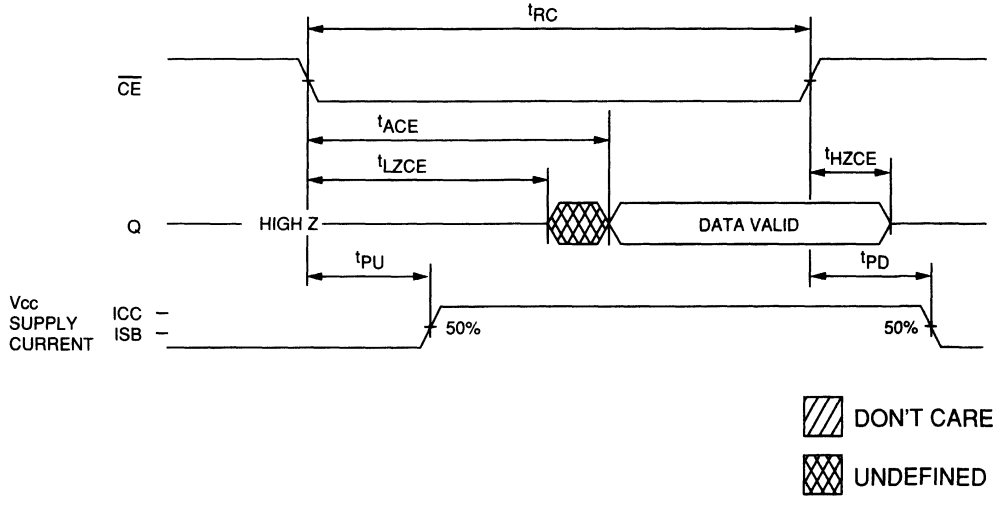
LOW Vcc DATA RETENTION WAVEFORM



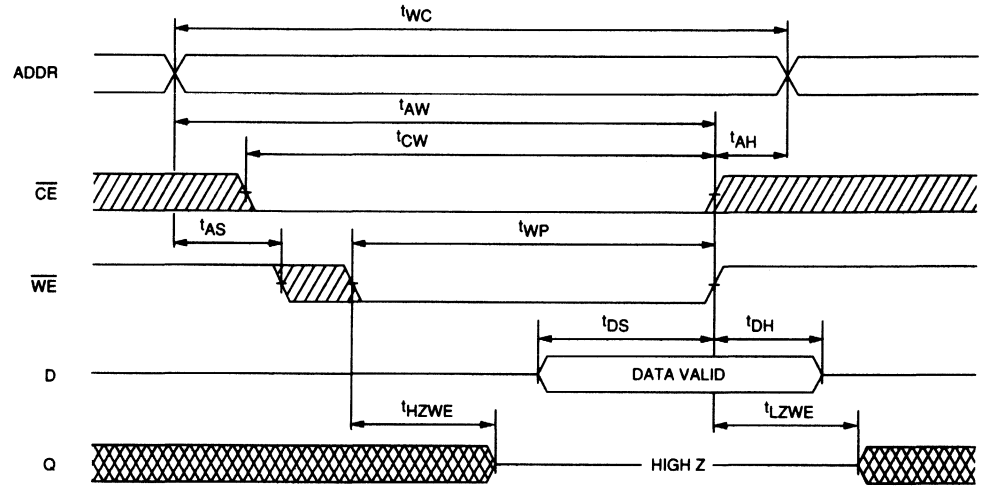
READ CYCLE NO. 1 (NOTES 8, 9)



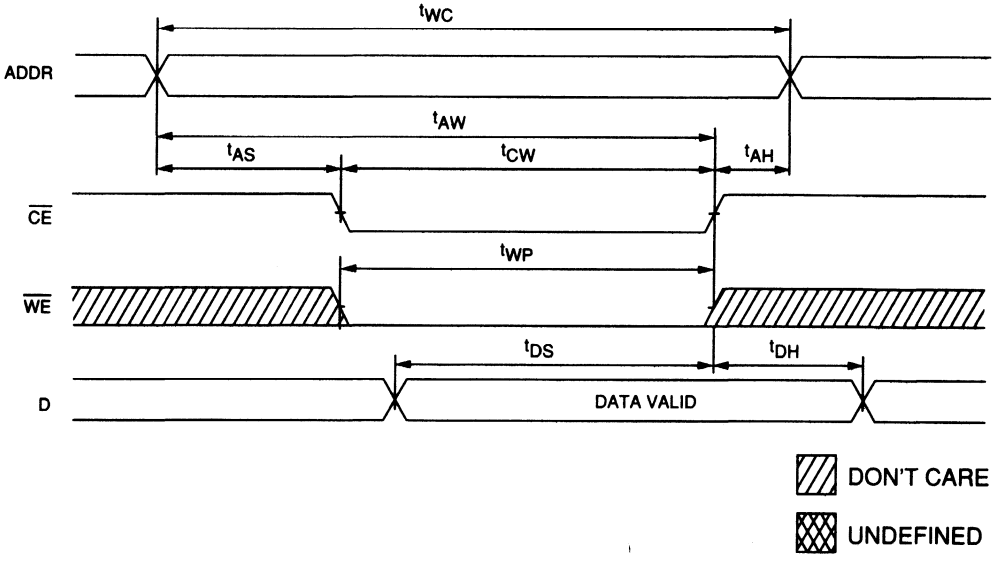
READ CYCLE NO. 2 (NOTES 7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



SRAM

16K x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

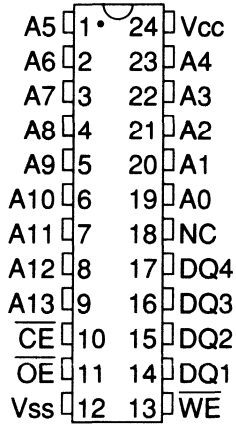
- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS

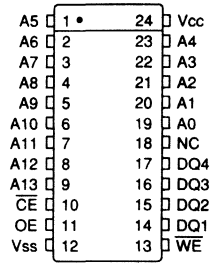
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

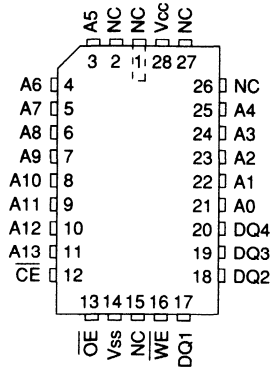
24L/300 DIP (PG, CG)



24L/300 SOJ (DJB)



28L/LCC (ECF)



GENERAL DESCRIPTION

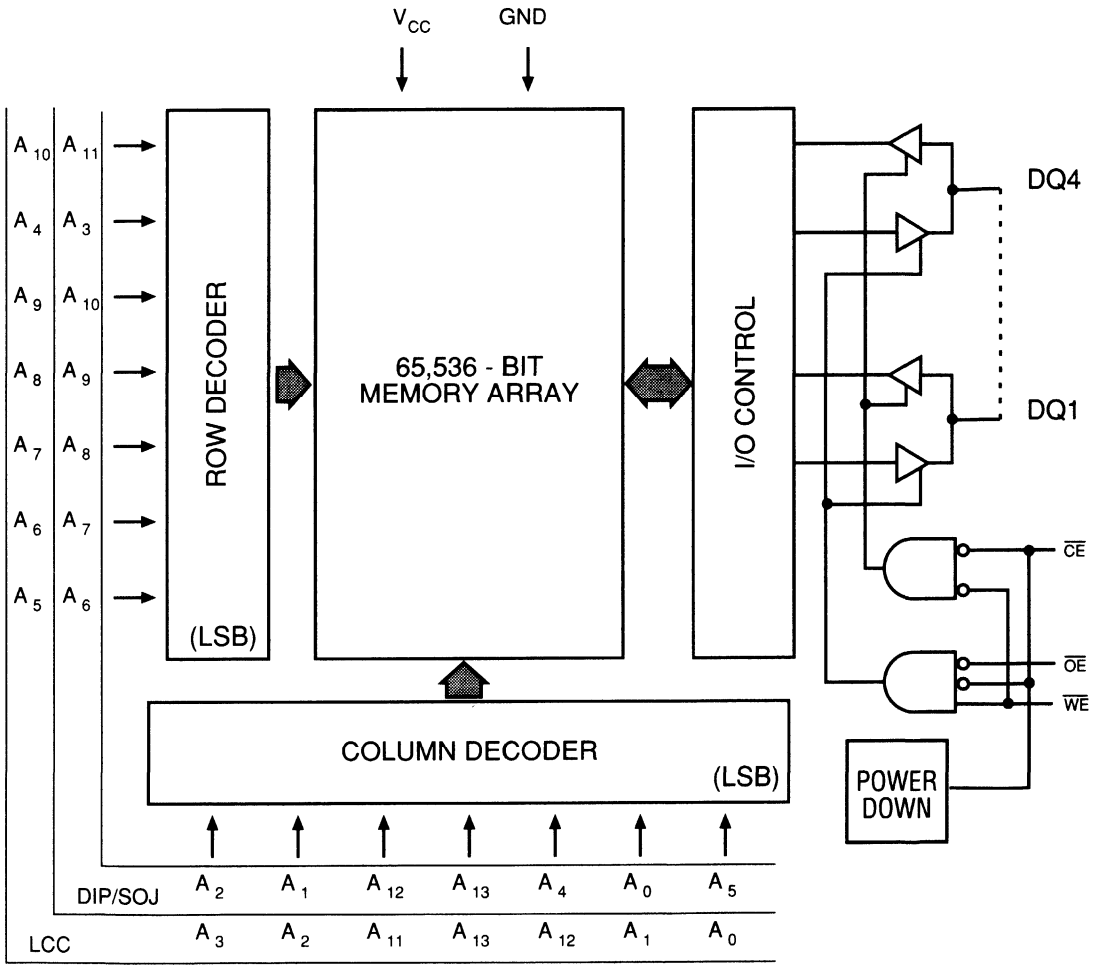
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	60	50	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	t_{RC}	12		15		20		25		30		35		ns	
Address access time	t_{AA}		12		15		20		25		30		35	ns	
Chip enable access time	t_{ACE}		12		12		15		20		25		30	ns	
Output hold from access change	t_{OH}	3		3		3		3		3		3		ns	
Chip enable to output in low Z	t_{LZCE}	3		3		5		5		5		5		ns	
Chip disable to output in high Z	t_{HZCE}		7		7		10		10		15		20	ns	6,7
Chip enable to power up time	t_{PU}	0		0		0		0		0		0		ns	
Chip disable to power down time	t_{PD}		12		15		20		25		30		35	ns	
Output enable access time	t_{AOE}		7		7		9		10		15		20	ns	
Output enable to output in low Z	t_{LZOE}	0		0		0		0		0		0		ns	
Output disable to output in high Z	t_{HZOE}		6		6		10		10		15		20	ns	6
WRITE Cycle															
WRITE cycle time	t_{WC}	12		15		20		25		30		35		ns	
Chip enable to end of write	t_{CW}	10		12		15		20		25		25		ns	
Address valid to end of write	t_{AW}	12		12		15		20		25		25		ns	
Address set-up time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns	
Write pulse width	t_{WP}	10		12		15		20		25		25		ns	
Data set-up time	t_{DS}	8		8		10		10		15		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	2		2		2		2		2		2		ns	
Write enable to output in high Z	t_{HZWE}	0	6	0	6	0	8	0	10	0	12	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

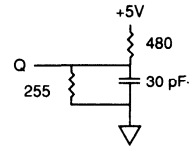


Fig. 1 OUTPUT LOAD EQUIVALENT

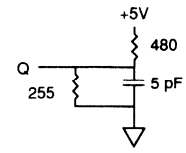


Fig. 2 OUTPUT LOAD EQUIVALENT

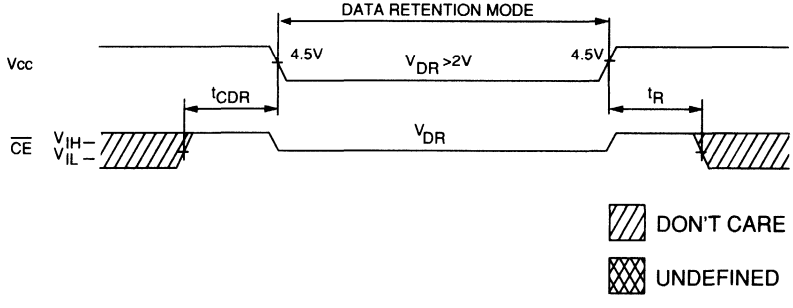
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.

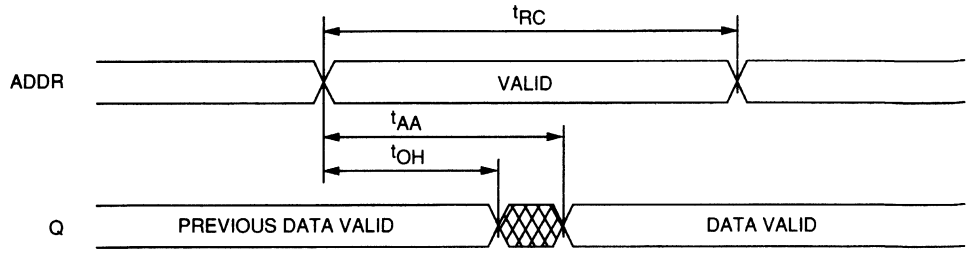
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	I_{CCDR}		95	500	µA	
		Vcc=3v			350	750	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

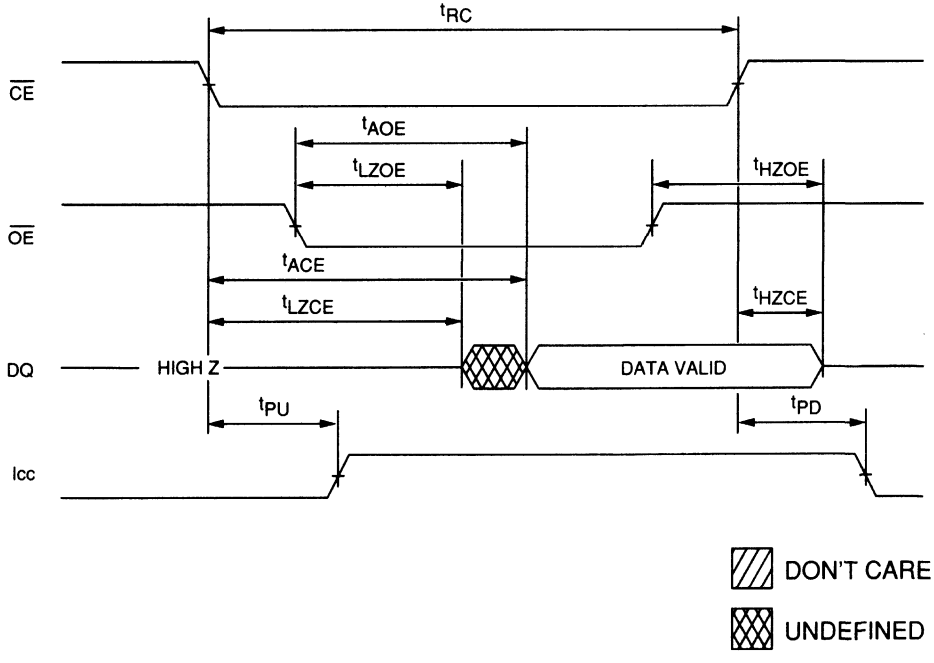
LOW Vcc DATA RETENTION WAVEFORM



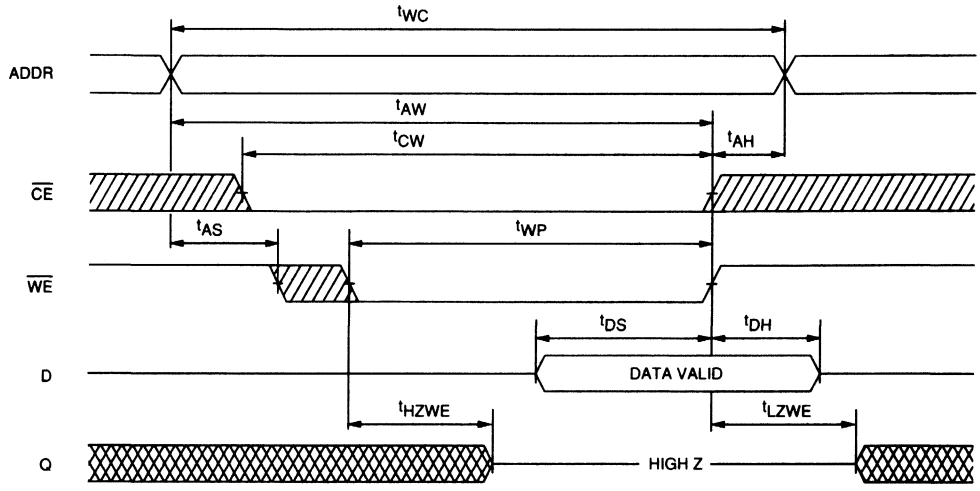
READ CYCLE NO. 1 (NOTES 8, 9)



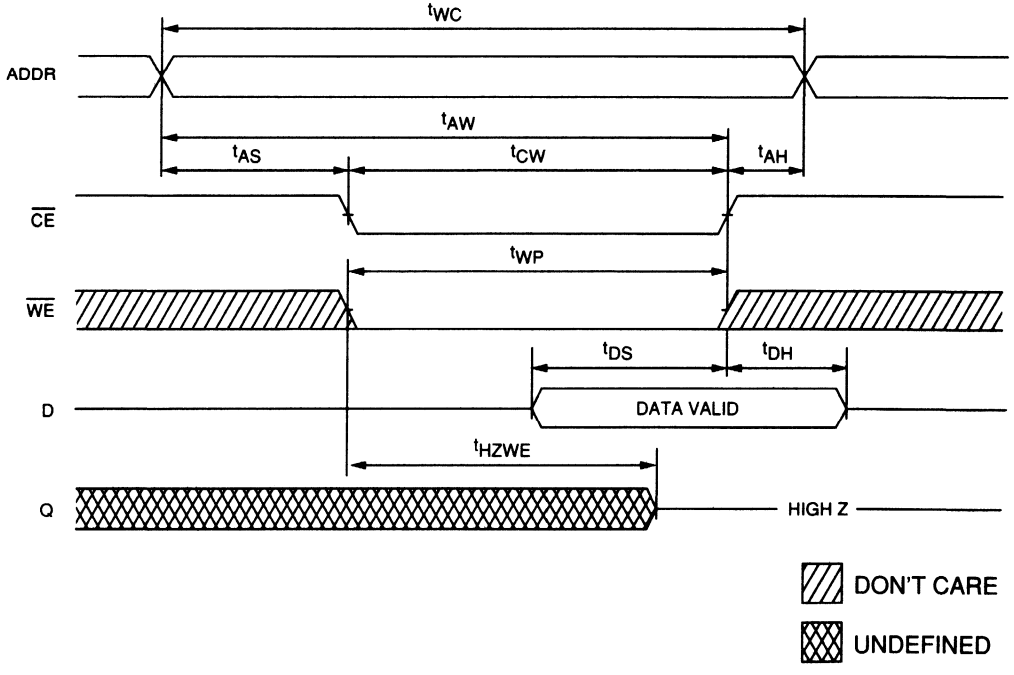
READ CYCLE NO. 2 (NOTES 7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



SRAM

16K x 4 SRAM

WITH SEPARATE INPUTS AND OUTPUTS

FEATURES

- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}1$, $\overline{CE}2$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- MT5C6406 – output tracks input during WRITE
- MT5C6407 – output high impedance during WRITE

OPTIONS / MARKING

• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

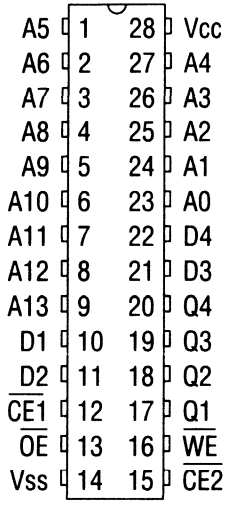
For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 4 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

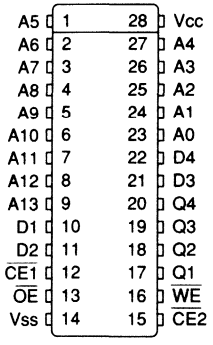
All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

PIN ASSIGNMENT (Top View)

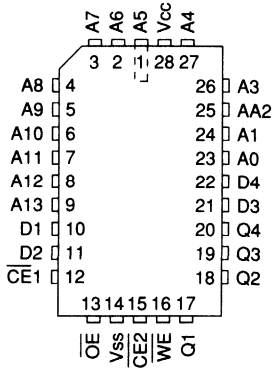
28L/300 DIP
(PJ, CI)



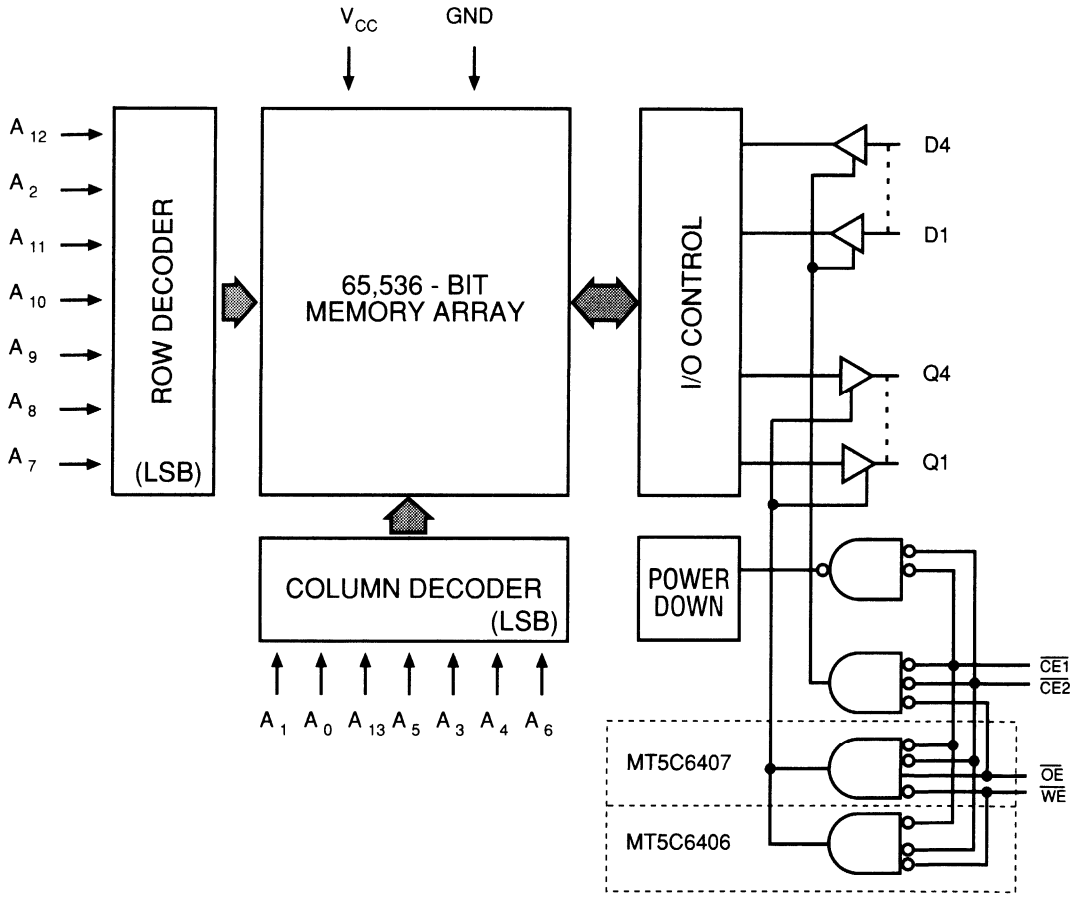
28L/300 SOJ
(DJC)



28L/LCC
(ECF)



FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE1}$	$\overline{CE2}$	$\overline{OE}$	$\overline{WE}$	OUTPUTS	POWER
STANDBY	H	X	X	X	HIGH Z	STANDBY
STANDBY	X	H	X	X	HIGH Z	STANDBY
READ	L	L	L	H	Q	ACTIVE
READ	L	L	H	H	HIGH Z	ACTIVE
WRITE (1)	L	L	X	L	HIGH Z	ACTIVE
WRITE (2)	L	L	L	L	D	ACTIVE
WRITE (2)	L	L	H	L	HIGH Z	ACTIVE

NOTES: 1. MT5C6407 ONLY
2. MT5C6406 ONLY

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	60	50	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	t_{RC}	12		15		20		25		30		35		ns	
Address access time	t_{AA}		12		15		20		25		30		35	ns	
Chip enable access time	t_{ACE}		12		12		15		20		25		30	ns	
Output hold from access change	t_{OH}	3		3		3		3		3		3		ns	
Chip enable to output in low Z	t_{LZCE}	3		3		5		5		5		5		ns	
Chip disable to output in high Z	t_{HZCE}		7		7		10		10		15		20	ns	6,7
Chip enable to power up time	t_{PU}	0		0		0		0		0		0		ns	
Chip disable to power down time	t_{PD}		12		15		20		25		30		35	ns	
Output enable access time	t_{AOE}		7		7		9		10		15		20	ns	
Output enable to output in low Z	t_{LZOE}	0		0		0		0		0		0		ns	
Output disable to output in high Z	t_{HZOE}		6		6		10		10		15		20	ns	6
WRITE Cycle															
WRITE cycle time	t_{WC}	12		15		20		25		30		35		ns	
Chip enable to end of write	t_{CW}	10		12		15		20		25		25		ns	
Address valid to end of write	t_{AW}	12		12		15		20		25		25		ns	
Address set-up time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns	
Write pulse width	t_{WP}	10		12		15		20		25		25		ns	
Data set-up time	t_{DS}	8		8		10		10		15		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	2		2		2		2		2		2		ns	
Write enable to output in high Z	t_{HZWE}	0	6	0	6	0	8	0	10	0	12	0	15	ns	6
Write enable to output valid	t_{AWE}		12		15		20		25		30		35	ns	
Data valid to output valid	t_{ADV}		12		15		20		25		30		35	ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

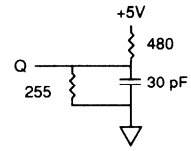


Fig. 1 OUTPUT LOAD EQUIVALENT

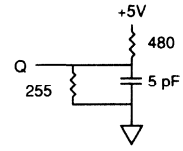


Fig. 2 OUTPUT LOAD EQUIVALENT

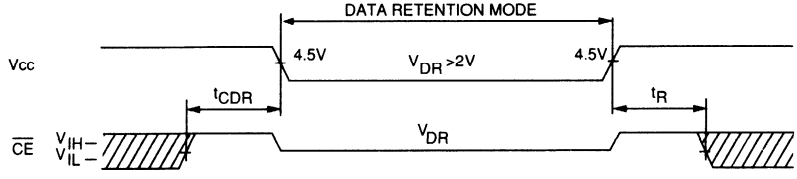
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	I_{CCDR}		95	500	µA	
		Vcc=3v			350	750	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

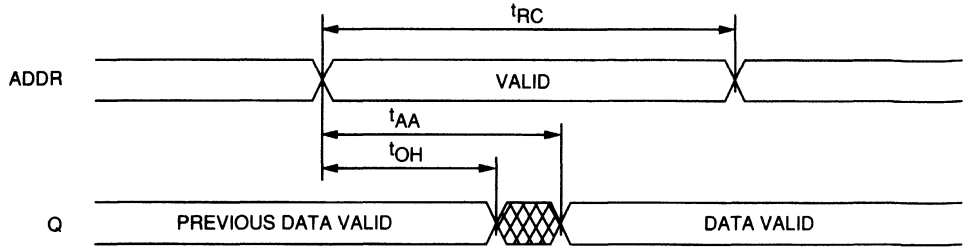
LOW Vcc DATA RETENTION WAVEFORM



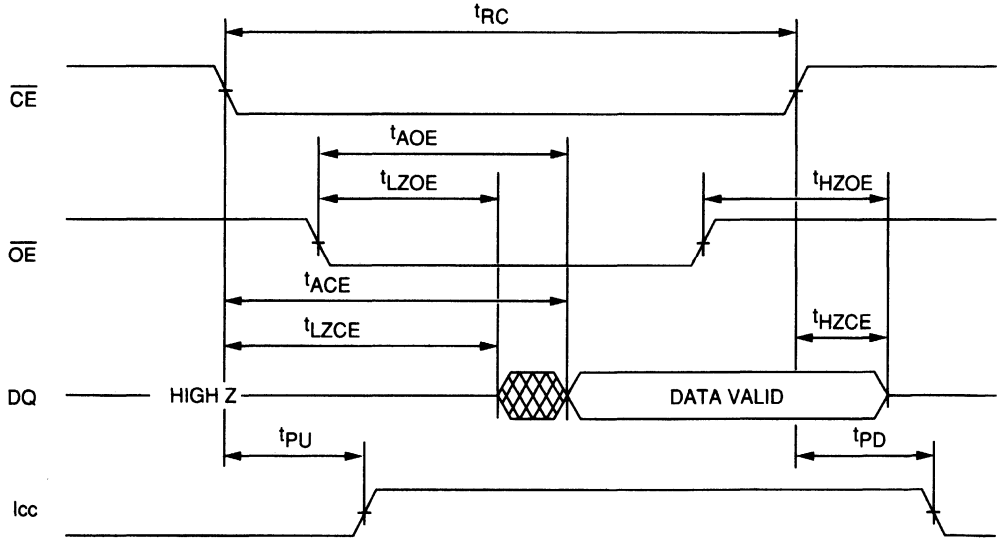
DON'T CARE

UNDEFINED

READ CYCLE NO. 1 (NOTES 8, 9)



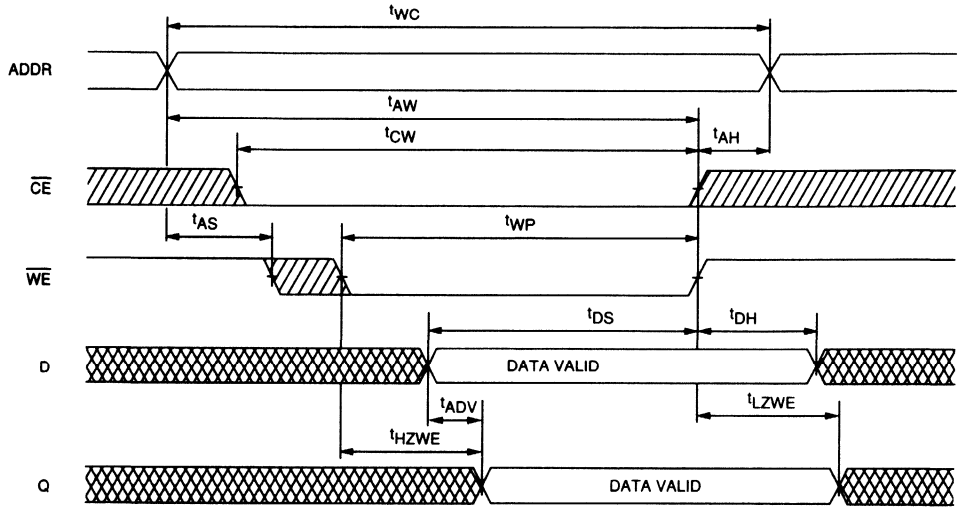
READ CYCLE NO. 2 (NOTES 7, 8, 10)



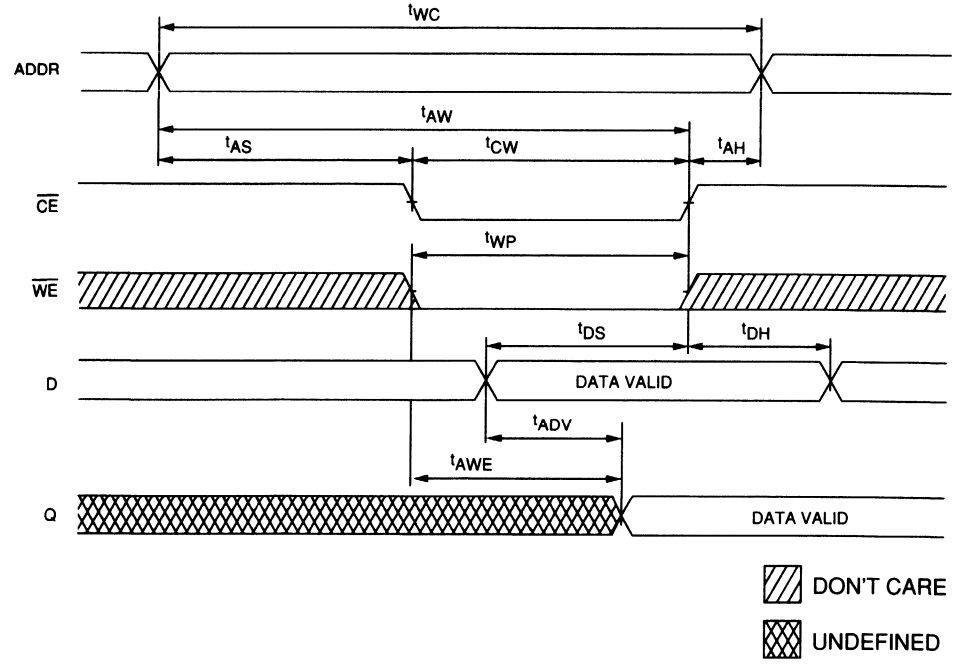
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



SRAM 32K x 8 SRAM

FEATURES

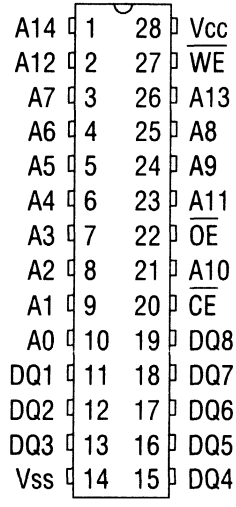
- High speed: 20, 25, 30, 35, and 45ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS

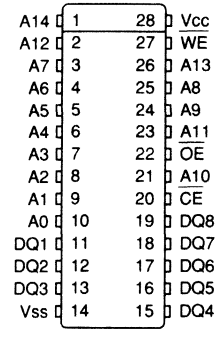
	MARKING
• Timing	
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
Ceramic DIP (300 mil)	C
Ceramic DIP (600 mil)	CW
Plastic SOJ (300 mil)	DJ
Ceramic LCC (28 pin)	EC
Ceramic LCC (32 pin)	ECW
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

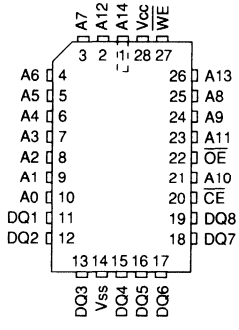
28L/300/600 DIP
(PJ, PK, CI, CK)



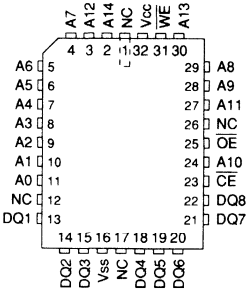
28L/300 SOJ
(DJC)



28L/LCC
(ECF)



32L/LCC
(ECH)



GENERAL DESCRIPTION

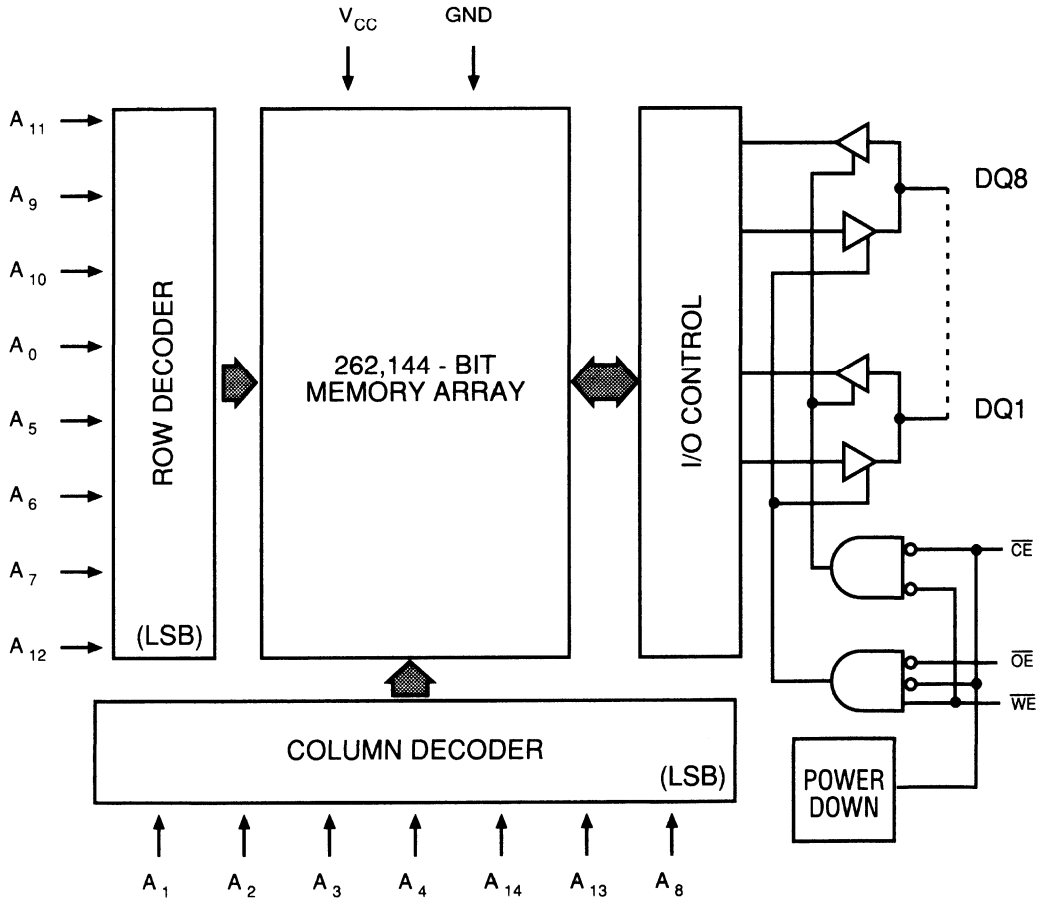
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	105	95	95	90	90	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	30	25	25	25	25	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	5	5	5	7	7	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-20		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	t_{RC}	20		25		30		35		45		ns	
Address access time	t_{AA}		20		25		30		35		45	ns	
Chip enable access time	t_{ACE}		20		25		30		35		45	ns	
Output hold from address change	t_{OH}	3		5		5		5		5		ns	
Chip enable to output in low Z	t_{LZCE}	6		6		6		6		6		ns	
Chip disable to output in high Z	t_{HZCE}		9		9		12		15		18	ns	6, 7
Chip enable to power up time	t_{PU}	0		0		0		0		0		ns	
Chip disable to power down time	t_{PD}		20		25		30		35		45	ns	
Output Enable Access Time	t_{AOE}		8		8		10		12		15	ns	
Output Enable to output in low Z	t_{LZOE}	2		2		2		2		2		ns	
Output disable to out put in high Z	t_{HZOE}		7		7		10		12		15	ns	
WRITE Cycle													
WRITE cycle time	t_{WC}	20		20		25		30		35		ns	
Chip enable to end of write	t_{CW}	15		15		18		20		25		ns	
Address Valid to end of write	t_{AW}	15		15		18		20		25		ns	
Address set-up time	t_{AS}	0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		ns	
Write pulse width	t_{WP}	15		15		18		20		25		ns	
Data set-up time	t_{DS}	10		10		12		15		20		ns	
Data hold time	t_{DH}	0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	5		5		5		5		5		ns	
Write enable to output in high Z	t_{HZWE}	0	10	0	10	0	12	0	15	0	18	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

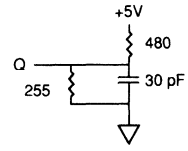


Fig. 1 OUTPUT LOAD EQUIVALENT

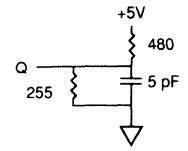


Fig. 2 OUTPUT LOAD EQUIVALENT

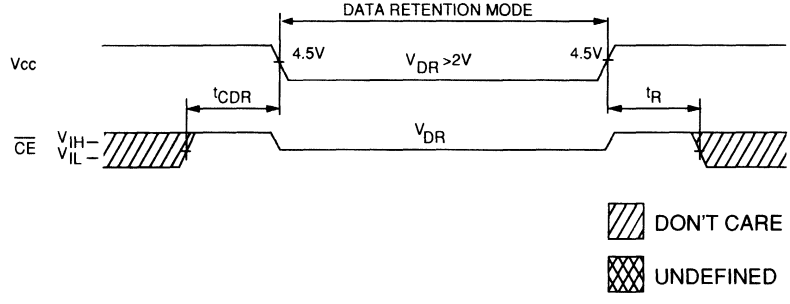
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF asin Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.

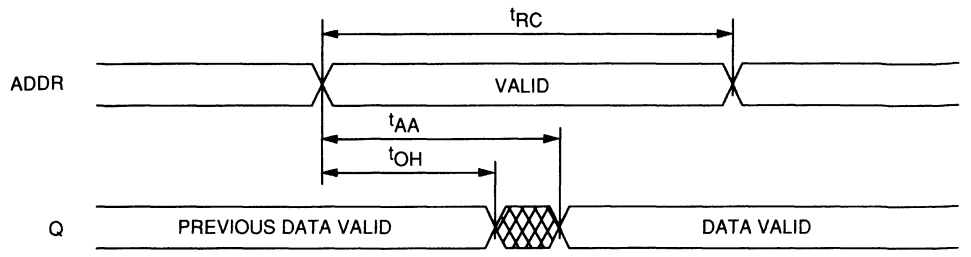
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	I_{CCDR}		95	500	µA	
		Vcc=3v			350	750	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

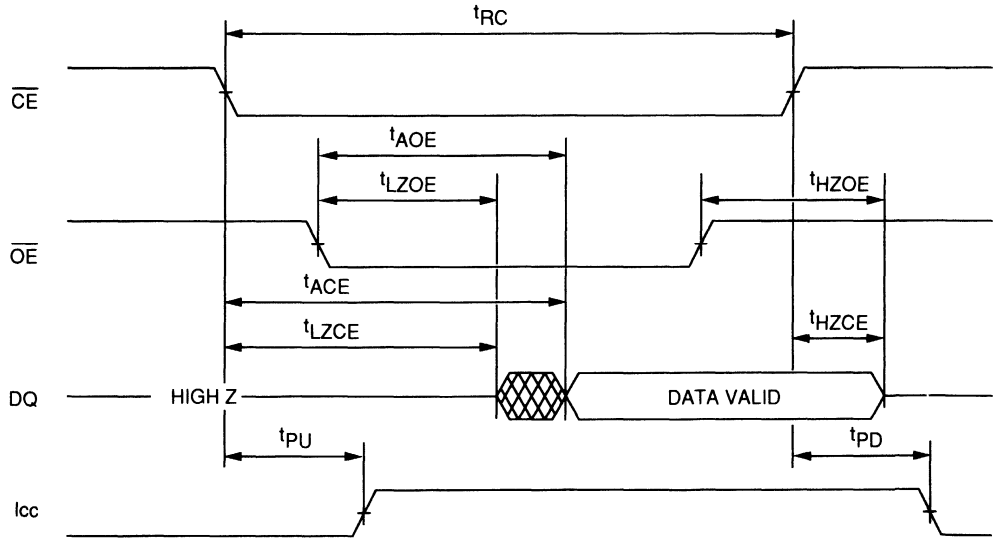
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 (NOTES 8, 9)



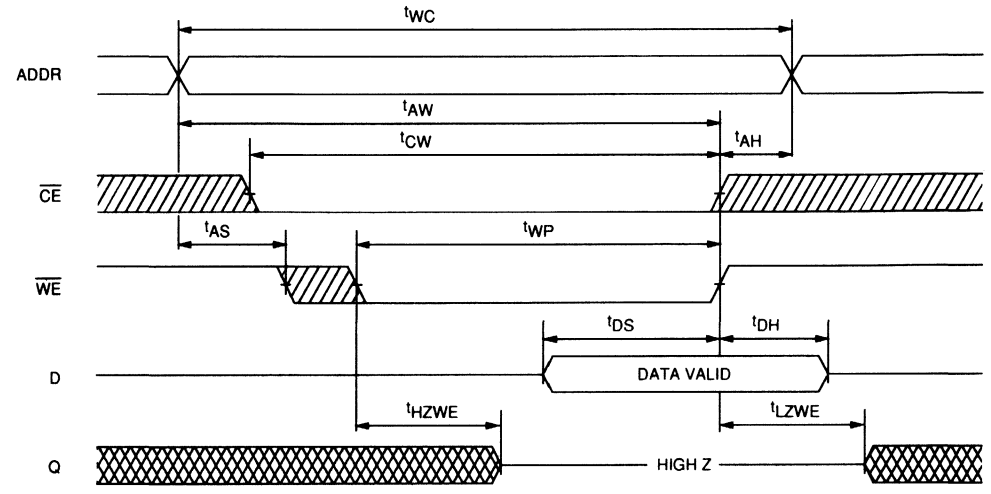
READ CYCLE NO. 2 (NOTES 7, 8, 10)



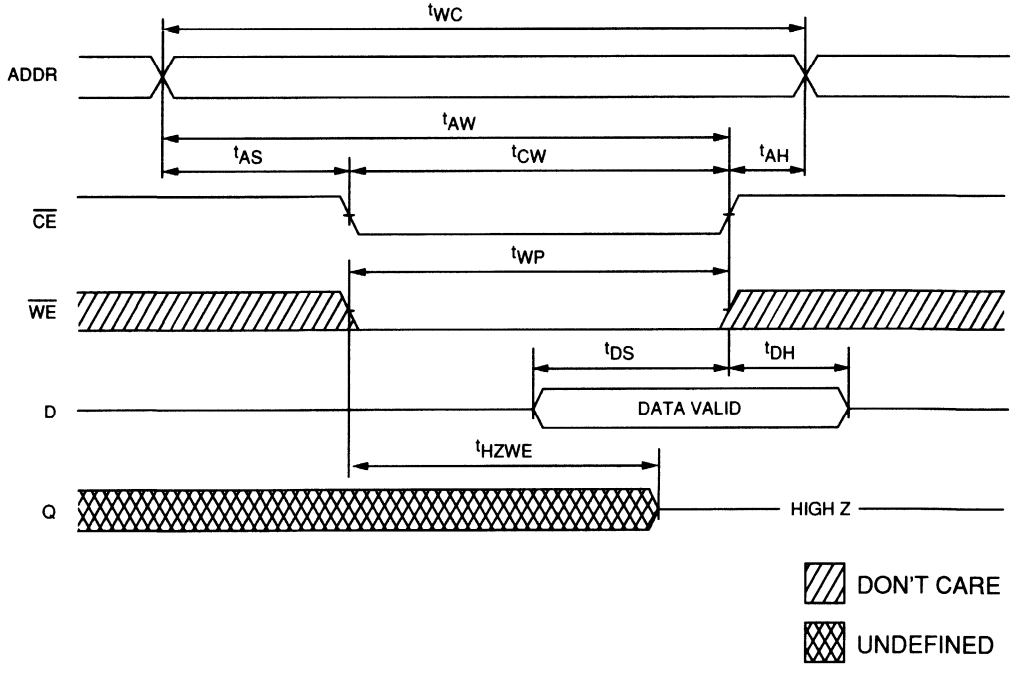
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



SRAM

64K x 1 SRAM

FEATURES

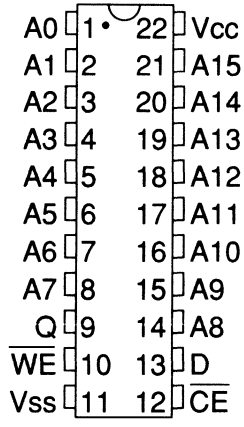
- High speed: 12, 15, 20, 25, 30 and 35ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

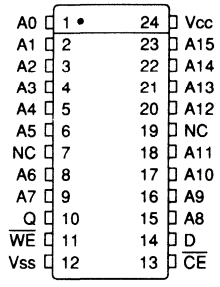
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

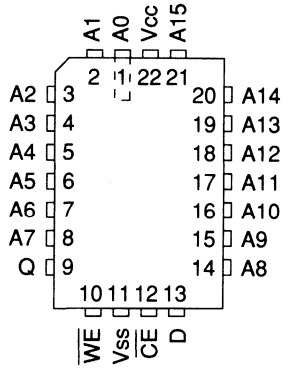
22L/300 DIP
(PF, CI)



24L/300 SOJ
(DJB)



22L/LCC
(ECE)



GENERAL DESCRIPTION

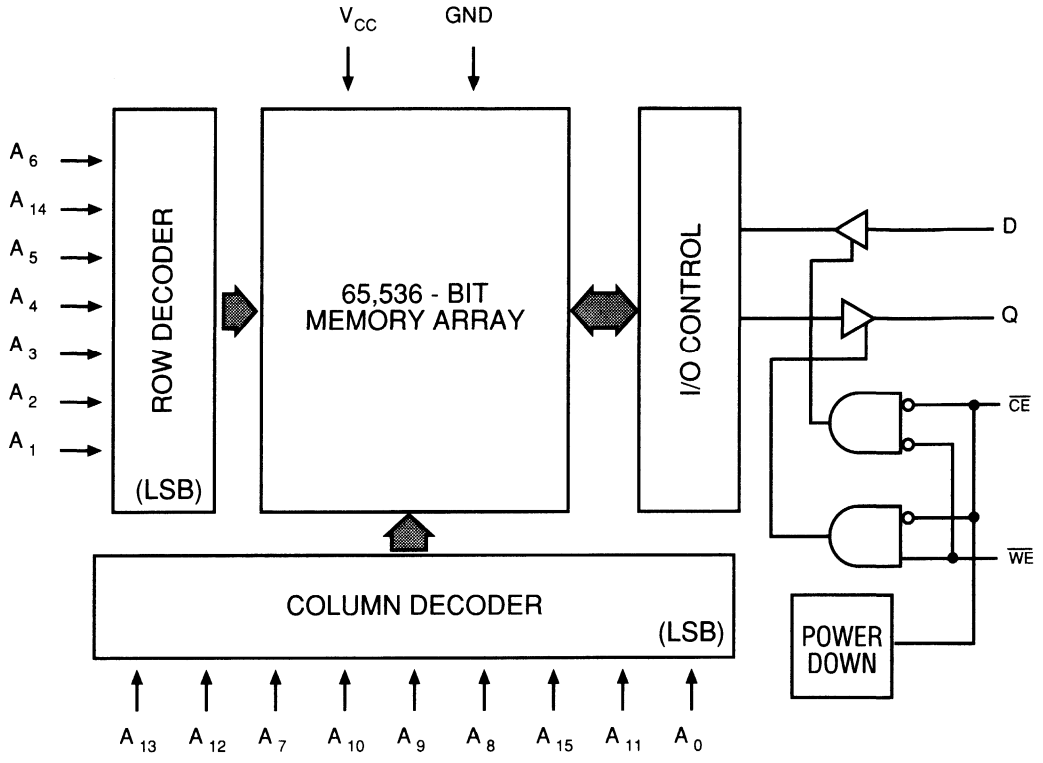
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	60	50	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	t_{RC}	12		15		20		25		30		35		ns	
Address access time	t_{AA}		12		15		20		25		30		35	ns	
Chip enable access time	t_{ACE}		12		12		15		20		25		30	ns	
Output hold from access change	t_{OH}	3		3		3		3		3		3		ns	
Chip enable to output in low Z	t_{LZCE}	3		3		5		5		5		5		ns	
Chip disable to output in high Z	t_{HZCE}		7		7		10		10		15		20	ns	6,7
Chip enable to power up time	t_{PU}	0		0		0		0		0		0		ns	
Chip disable to power down time	t_{PD}		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	t_{WC}	12		15		20		25		30		35		ns	
Chip enable to end of write	t_{CW}	10		12		15		20		25		25		ns	
Address valid to end of write	t_{AW}	12		12		15		20		25		25		ns	
Address set-up time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns	
Write pulse width	t_{WP}	10		12		15		20		25		25		ns	
Data set-up time	t_{DS}	8		8		10		10		15		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	2		2		2		2		2		2		ns	
Write enable to output in high Z	t_{HZWE}	0	6	0	6	0	8	0	10	0	12	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

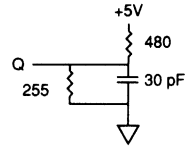


Fig. 1 OUTPUT LOAD EQUIVALENT

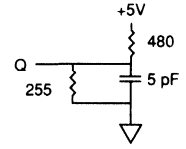


Fig. 2 OUTPUT LOAD EQUIVALENT

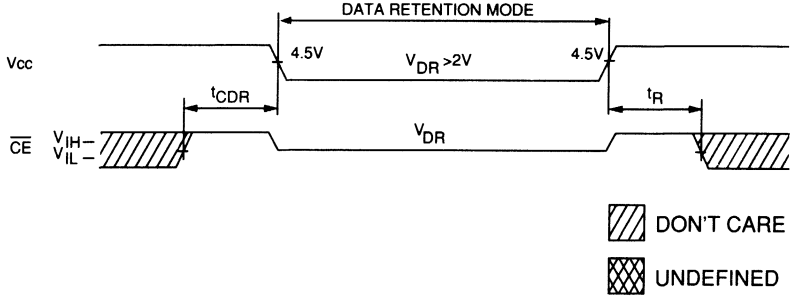
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{T}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.

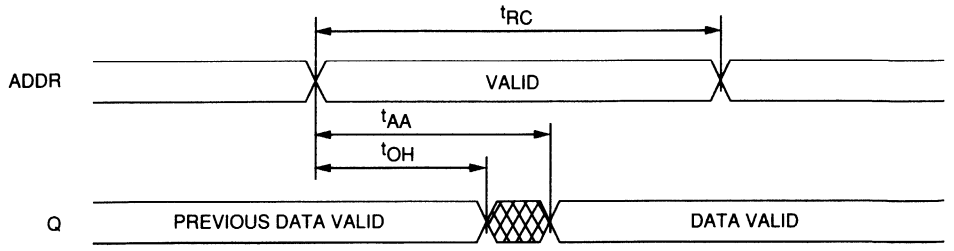
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	I_{CCDR}		95	500	µA	
		Vcc=3v			350	750	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

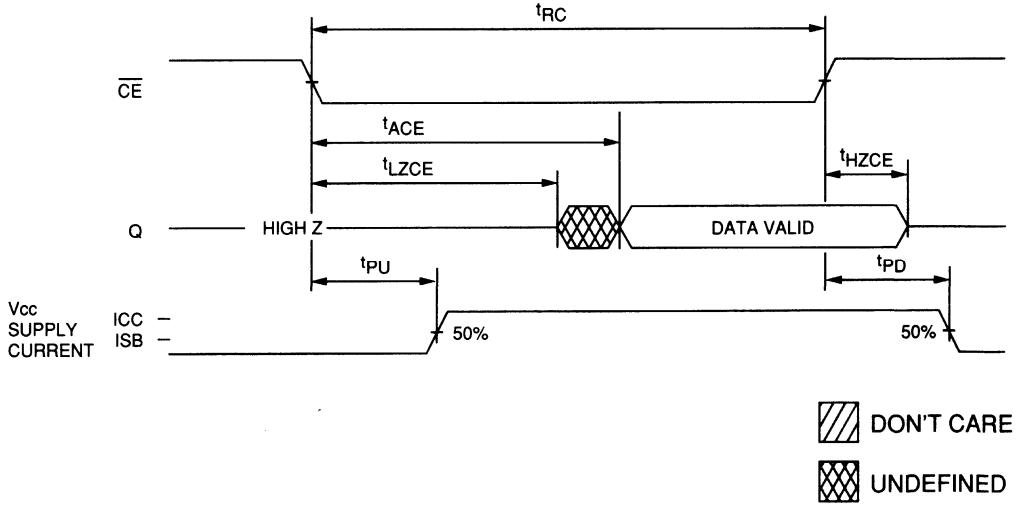
LOW Vcc DATA RETENTION WAVEFORM



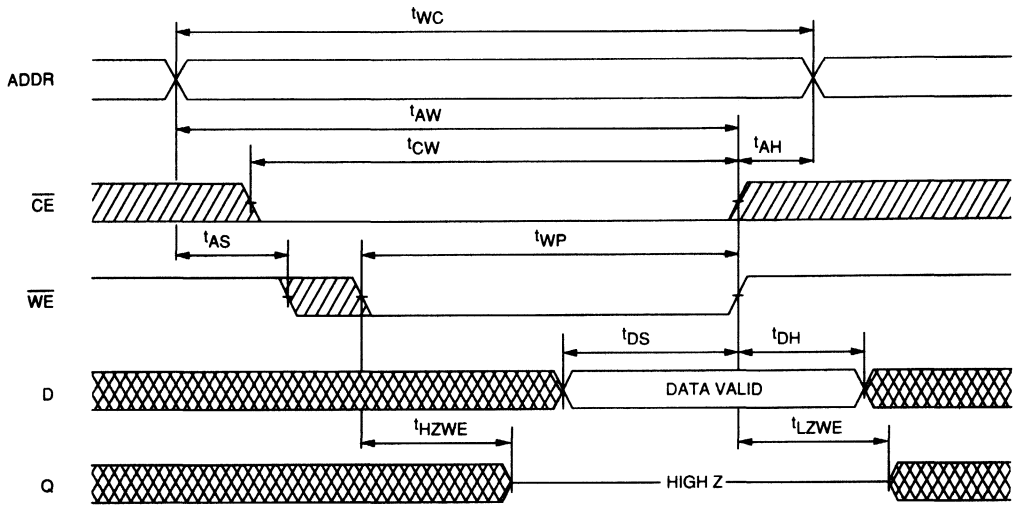
READ CYCLE NO. 1 (NOTES 8, 9)



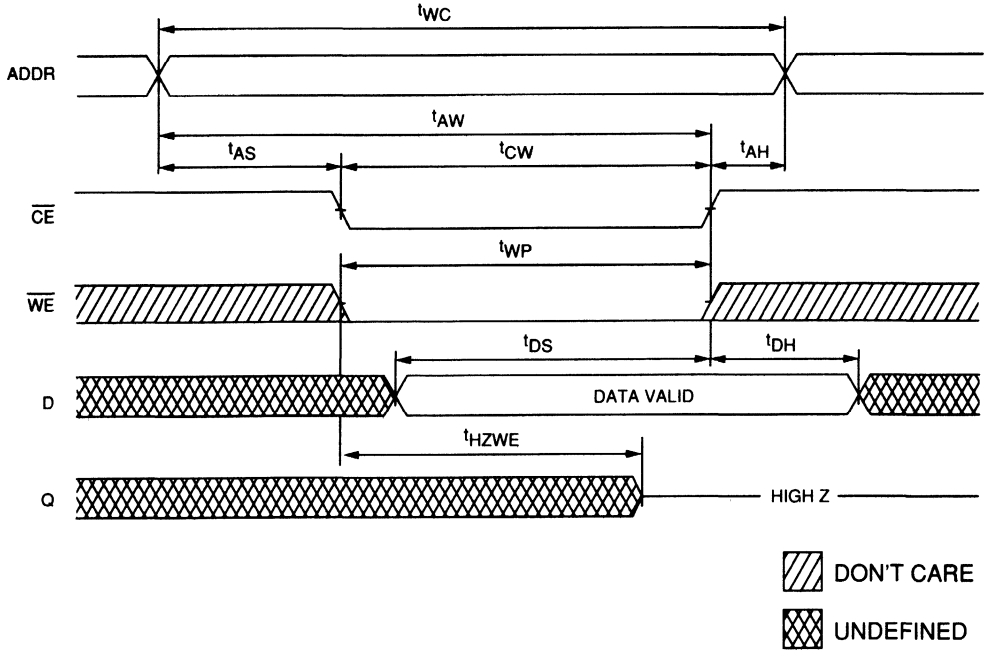
READ CYCLE NO. 2 (NOTES 7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



SRAM 64K x 4 SRAM

FEATURES

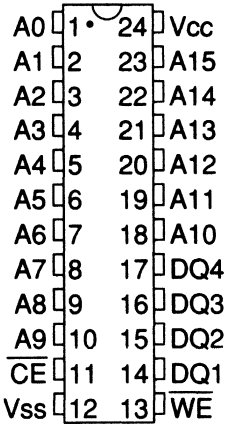
- High speed: 20, 25, 30, 35, and 45ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

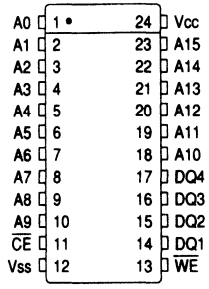
	MARKING
• Timing	
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

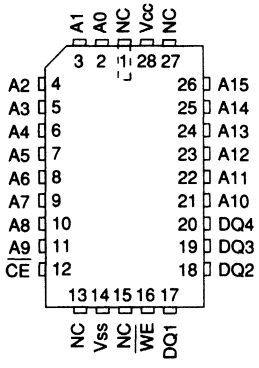
24L/300 DIP (PG, CG)



24L/300 SOJ (DJB)



28L/LCC (ECF)



GENERAL DESCRIPTION

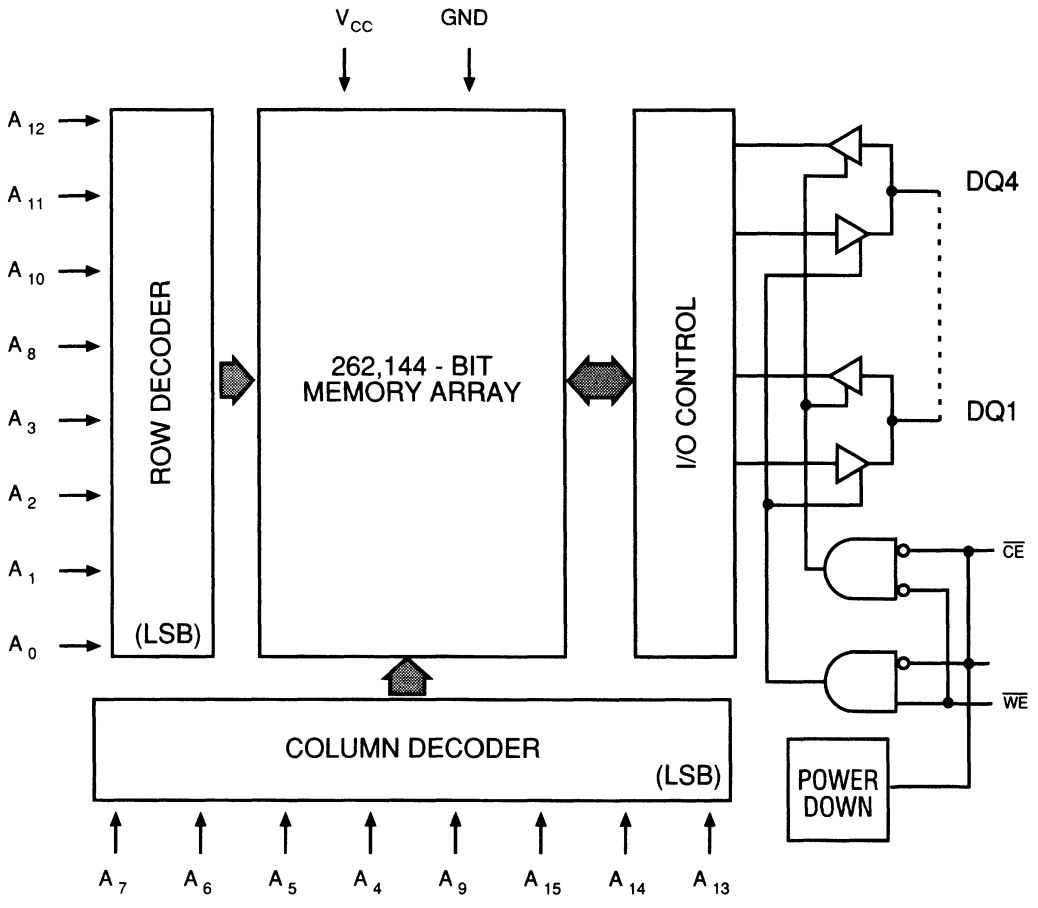
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	$V_{CC}+1$	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-20	-25	-30	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	105	95	95	90	90	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	30	25	25	25	25	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	5	5	5	7	7	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-20		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	t_{RC}	20		25		30		35		45		ns	
Address access time	t_{AA}		20		25		30		35		45	ns	
Chip enable access time	t_{ACE}		20		25		30		35		45	ns	
Output hold from address change	t_{OH}	3		5		5		5		5		ns	
Chip enable to output in low Z	t_{LZCE}	6		6		6		6		6		ns	
Chip disable to output in high Z	t_{HZCE}		9		9		12		15		18	ns	6, 7
Chip enable to power up time	t_{PU}	0		0		0		0		0		ns	
Chip disable to power down time	t_{PD}		20		25		30		35		45	ns	
WRITE Cycle													
WRITE cycle time	t_{WC}	20		20		25		30		35		ns	
Chip enable to end of write	t_{CW}	15		15		18		20		25		ns	
Address valid to end of write	t_{AW}	15		15		18		20		25		ns	
Address set-up time	t_{AS}	0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		ns	
Write pulse width	t_{WP}	15		15		18		20		25		ns	
Data set-up time	t_{DS}	10		10		12		15		20		ns	
Data hold time	t_{DH}	0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	5		5		5		5		5		ns	
Write enable to output in high Z	t_{HZWE}	0	10	0	10	0	12	0	15	0	18	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

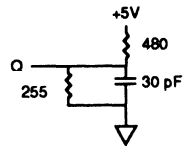


Fig. 1 OUTPUT LOAD EQUIVALENT

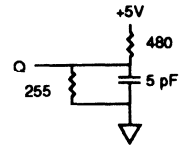


Fig. 2 OUTPUT LOAD EQUIVALENT

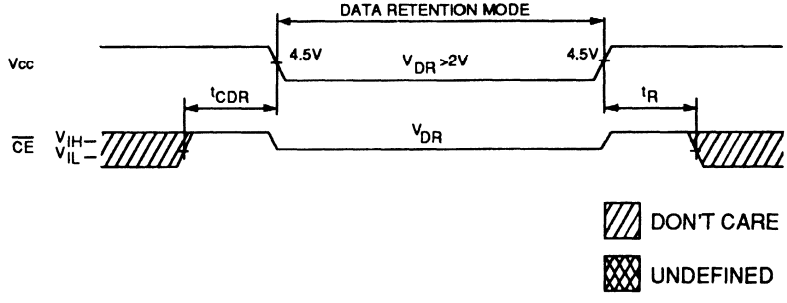
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.

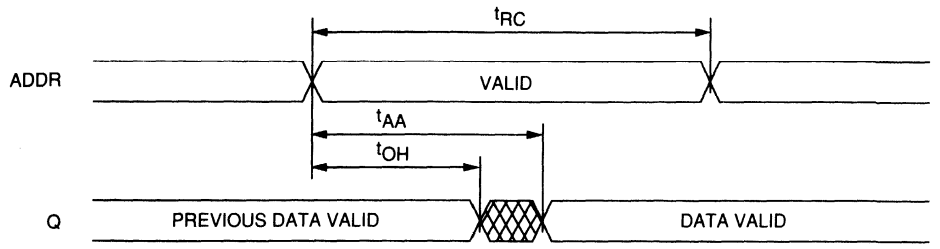
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	ICCDR		95	500	µA	
		Vcc=3v			350	750	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 10

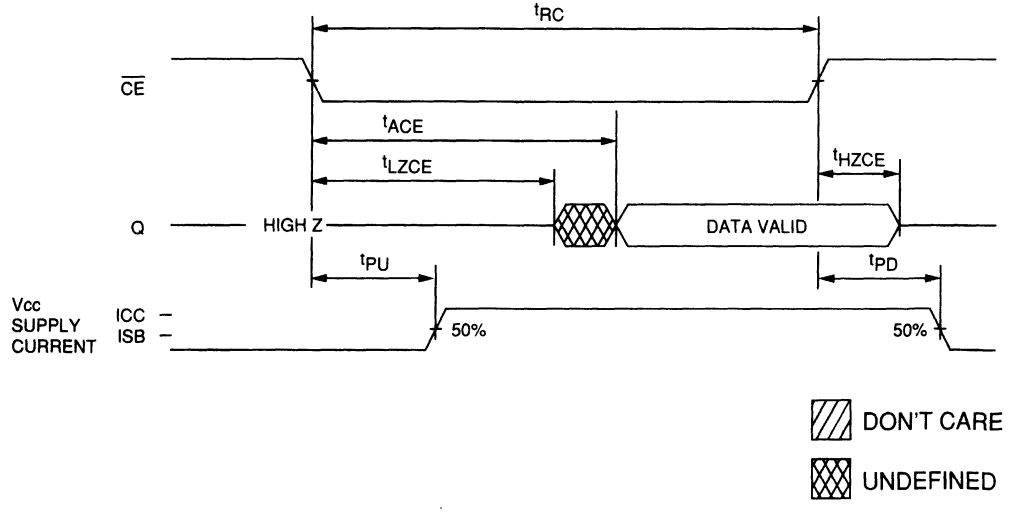
LOW Vcc DATA RETENTION WAVEFORM



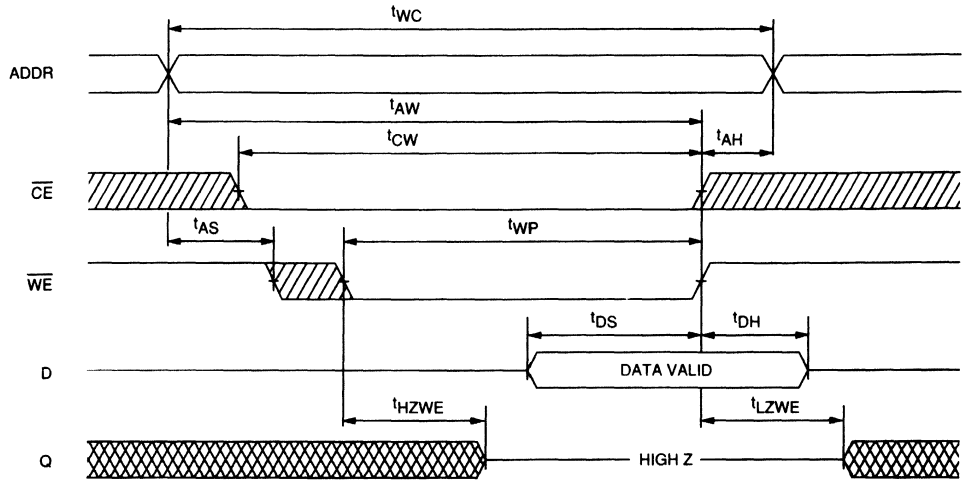
READ CYCLE NO. 1 (NOTES 8, 9)



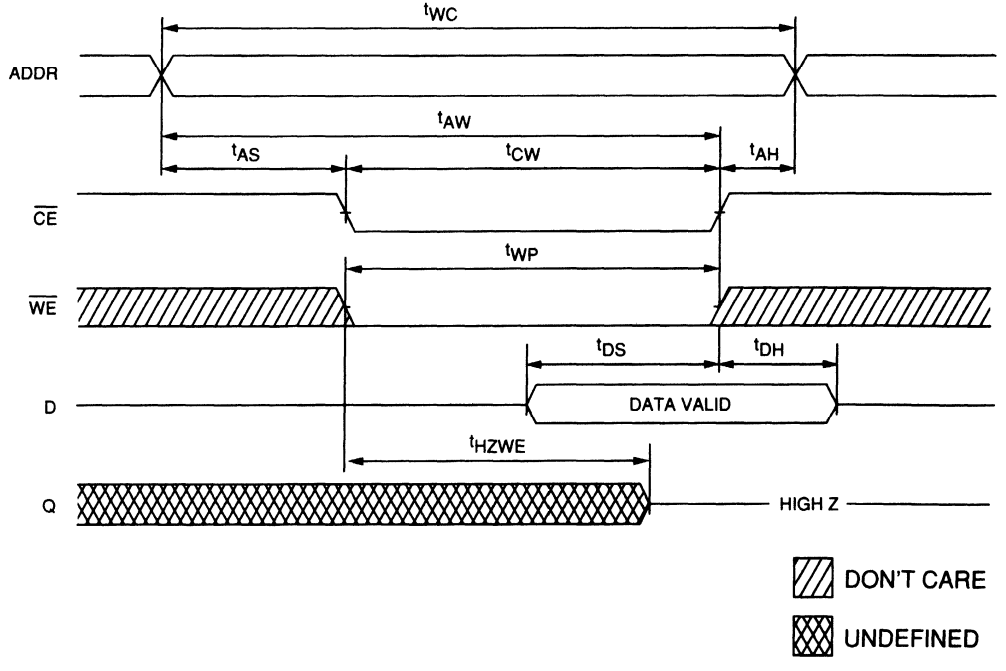
READ CYCLE NO. 2 (NOTES 7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



SRAM

64K x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

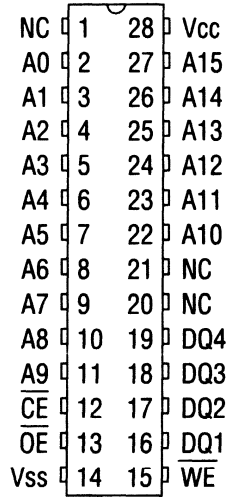
- High speed: 20, 25, 30, 35, and 45ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS / MARKING

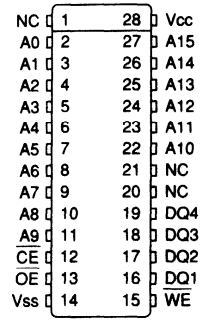
• Timing	
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

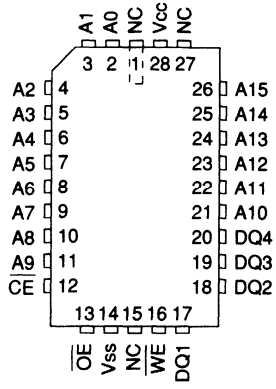
28L/300 DIP
(PJ, CI)



28L/300 SOJ
(DJC)



28L/LCC
(ECF)



GENERAL DESCRIPTION

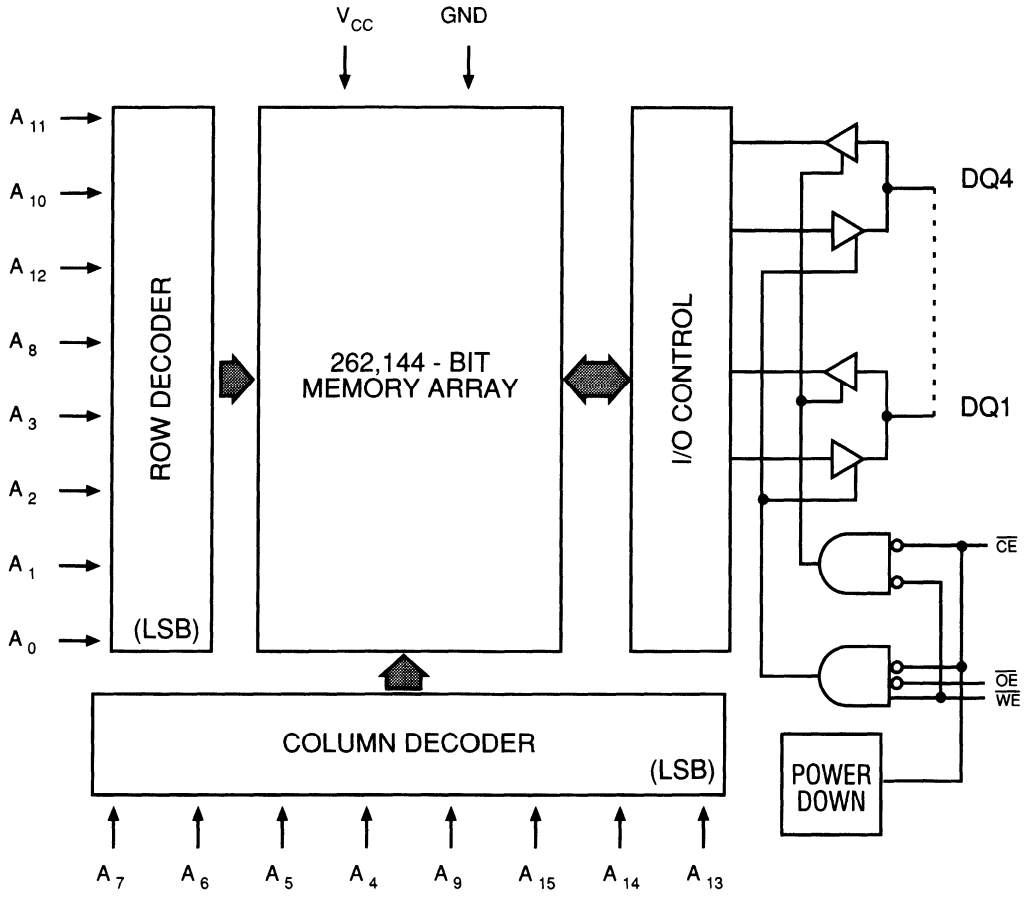
The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	$V_{CC}+1$	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-20	-25	-30	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	105	95	95	90	90	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	30	25	25	25	25	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	5	5	5	7	7	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C, Vcc = 5V ± 10%)

DESCRIPTION		-20		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	20		25		30		35		45		ns	
Address access time	^tAA		20		25		30		35		45	ns	
Chip enable access time	^tACE		20		25		30		35		45	ns	
Output hold from address change	^tOH	3		5		5		5		5		ns	
Chip enable to output in low Z	^tLZCE	6		6		6		6		6		ns	
Chip disable to output in high Z	^tHZCE		9		9		12		15		18	ns	6, 7
Chip enable to power up time	^tPU	0		0		0		0		0		ns	
Chip disable to power down time	^tPD		20		25		30		35		45	ns	
Output Enable Access Time	^tAOE		8		8		10		12		15	ns	
Output Enable to output in low Z	^tLZOE	2		2		2		2		2		ns	
Output disable to out put in high Z	^tHZOE		7		7		10		12		15	ns	
WRITE Cycle													
WRITE cycle time	^tWC	20		20		25		30		35		ns	
Chip enable to end of write	^tCW	15		15		18		20		25		ns	
Address Valid to end of write	^tAW	15		15		18		20		25		ns	
Address set-up time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
Write pulse width	^tWP	15		15		18		20		25		ns	
Data set-up time	^tDS	10		10		12		15		20		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in low Z	^tLZWE	5		5		5		5		5		ns	
Write enable to output in high Z	^tHZWE	0	10	0	10	0	12	0	15	0	18	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

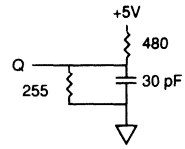


Fig. 1 OUTPUT LOAD EQUIVALENT

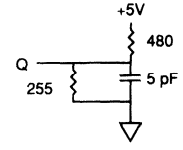


Fig. 2 OUTPUT LOAD EQUIVALENT

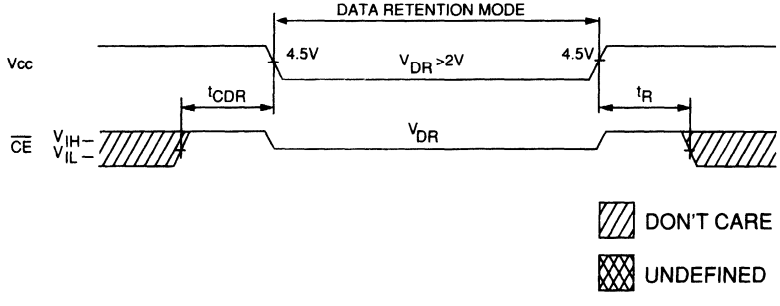
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.

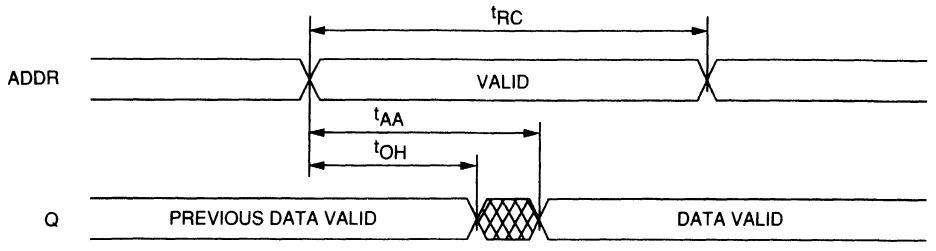
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	ICCDR		95	500	µA	
		Vcc=3v			350	750	µA	
Chip Deselect to Data Retention Time			tCDR	0		—	ns	4
Operation Recovery Time			tR	tRC			ns	4, 11

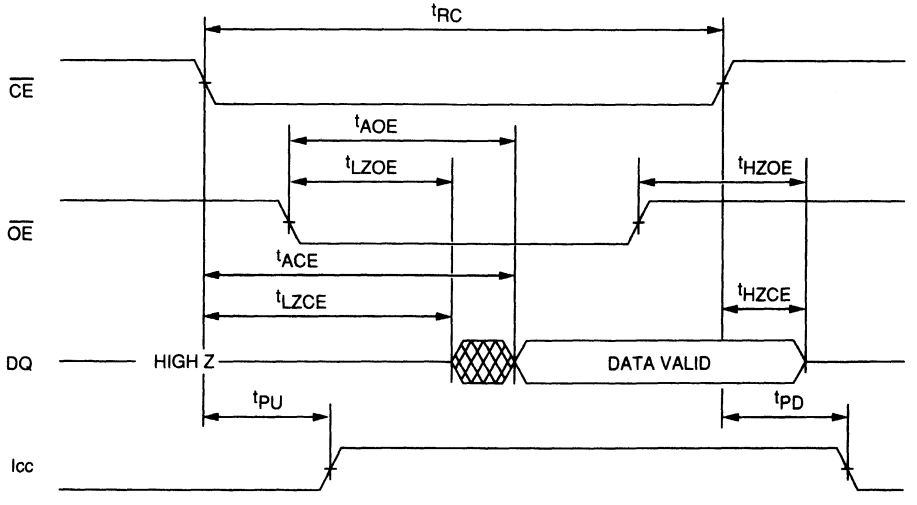
LOW Vcc DATA RETENTION WAVEFORM



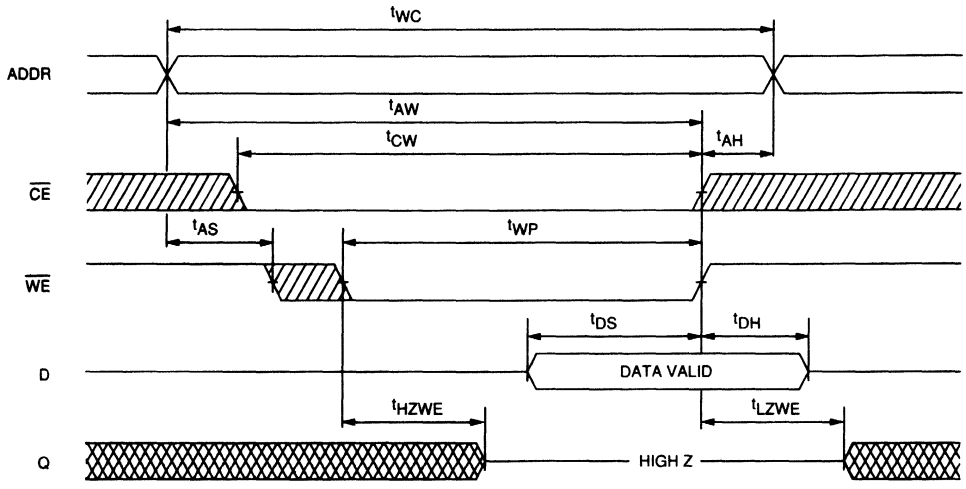
READ CYCLE NO. 1 (NOTES 8, 9)



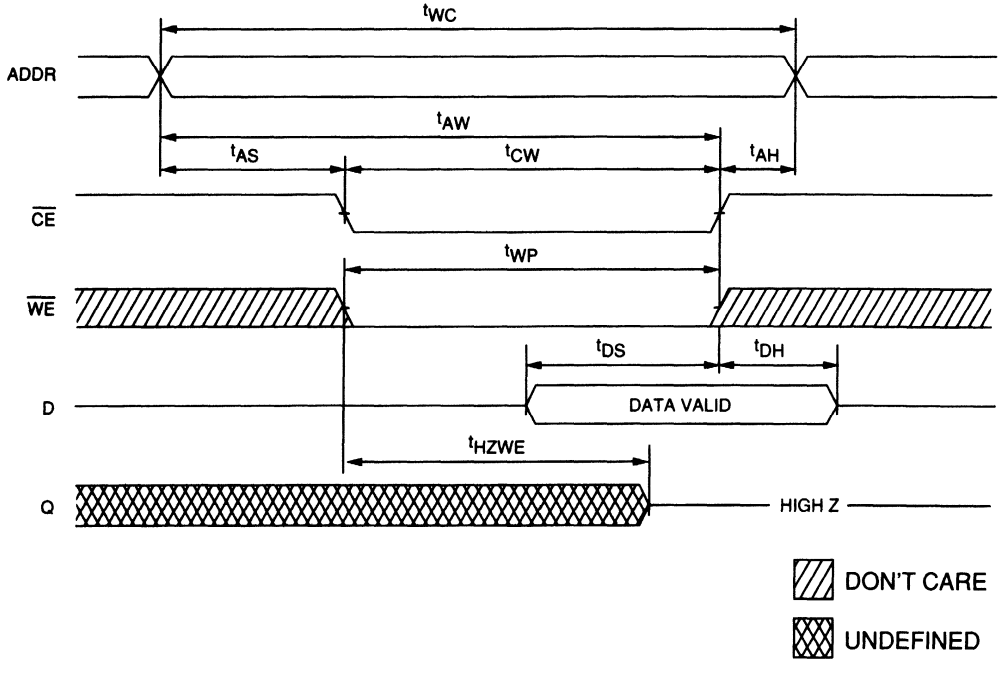
READ CYCLE NO. 2 (NOTES 7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



SRAM 128K x 8 SRAM

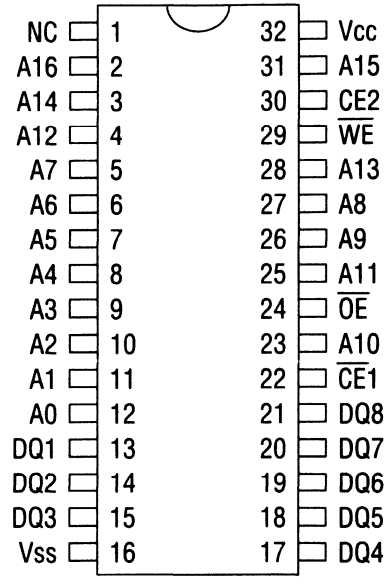
FEATURES

- High speed: 25, 35 and 45ns
- Automatic chip enable power down
- All inputs and outputs are TTL compatible
- High performance, low power, CMOS process
- Single +5V (±10%) power supply
- Low power, ICC (max.) 70mA

OPTIONS MARKING

• Timing	
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP	None
Ceramic DIP	C
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)



GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. Output enable ($\overline{OE}$) is an enhancement available and can place the output in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. $\overline{OE}$ must also be LOW to read the device. The devices offer a reduced power standby mode when disabled. This allows system designs for low power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

SRAM 256K x 1 SRAM

FEATURES

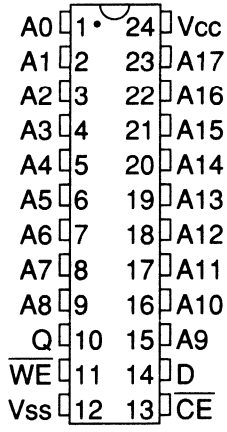
- High speed: 20, 25, 30, 35, and 45ns
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

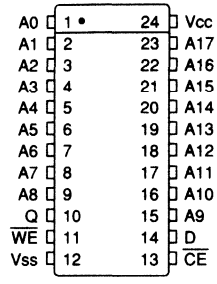
	MARKING
• Timing	
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

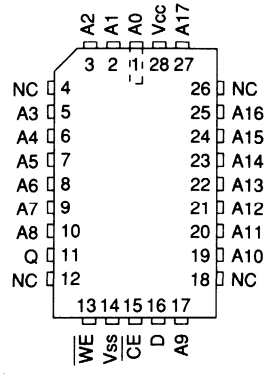
24L/300 DIP
(PG, CG)



24L/300 SOJ
(DJB)



28L/LCC
(ECF)



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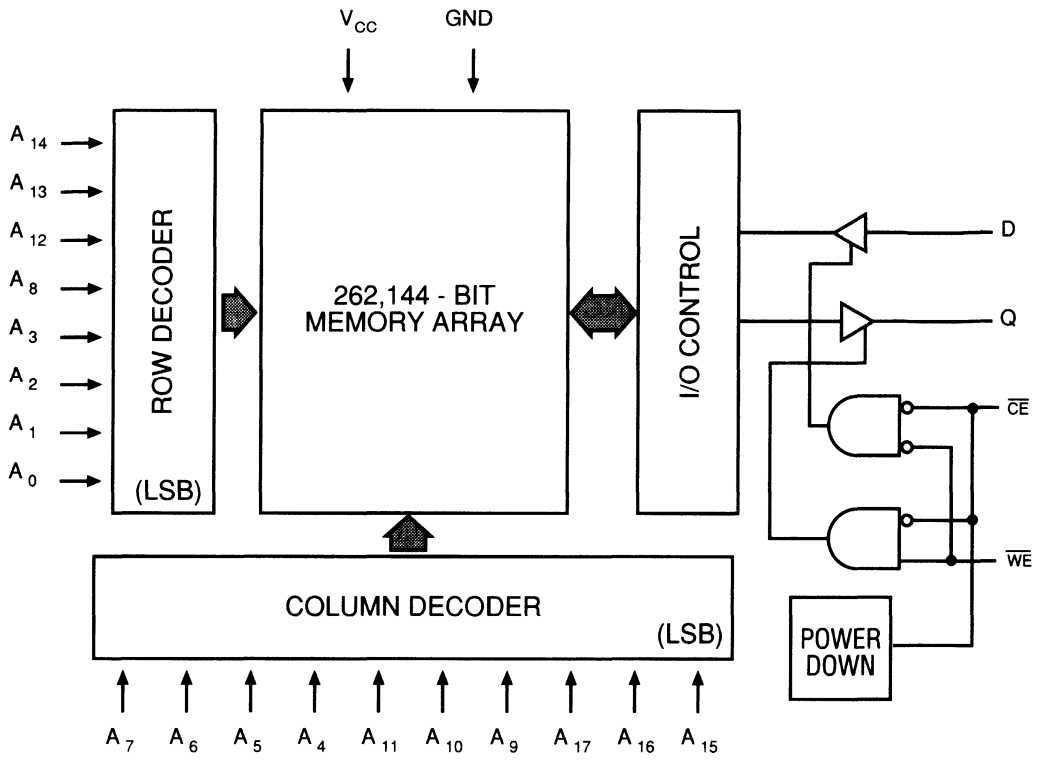
Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
STANDBY	H	X	HIGH Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-20	-25	-30	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	105	95	95	90	90	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max	I_{SB1}	30	25	25	25	25	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}	5	5	5	7	7	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C, V_{CC} = 5V ± 10%)

DESCRIPTION		-20		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	t_{RC}	20		25		30		35		45		ns	
Address access time	t_{AA}		20		25		30		35		45	ns	
Chip enable access time	t_{ACE}		20		25		30		35		45	ns	
Output hold from address change	t_{OH}	3		5		5		5		5		ns	
Chip enable to output in low Z	t_{LZCE}	6		6		6		6		6		ns	
Chip disable to output in high Z	t_{HZCE}		9		9		12		15		18	ns	6, 7
Chip enable to power up time	t_{PU}	0		0		0		0		0		ns	
Chip disable to power down time	t_{PD}		20		25		30		35		45	ns	
WRITE Cycle													
WRITE cycle time	t_{WC}	20		20		25		30		35		ns	
Chip enable to end of write	t_{CW}	15		15		18		20		25		ns	
Address valid to end of write	t_{AW}	15		15		18		20		25		ns	
Address set-up time	t_{AS}	0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		ns	
Write pulse width	t_{WP}	15		15		18		20		25		ns	
Data set-up time	t_{DS}	10		10		12		15		20		ns	
Data hold time	t_{DH}	0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	5		5		5		5		5		ns	
Write enable to output in high Z	t_{HZWE}	0	10	0	10	0	12	0	15	0	18	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

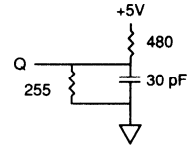


Fig. 1 OUTPUT LOAD EQUIVALENT

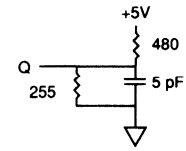


Fig. 2 OUTPUT LOAD EQUIVALENT

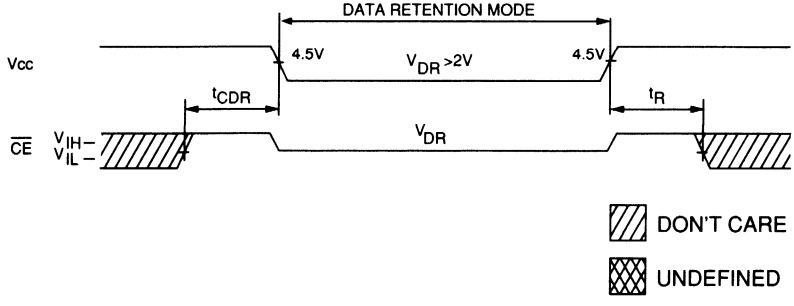
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. at Vcc = 2V.
12. at Vcc = 3V.
13. ^{t}RC = Read Cycle Time.

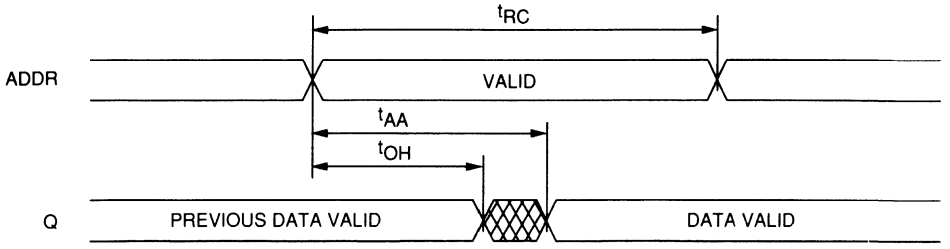
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	ICCDR		95	500	µA	
		Vcc=3v			350	750	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

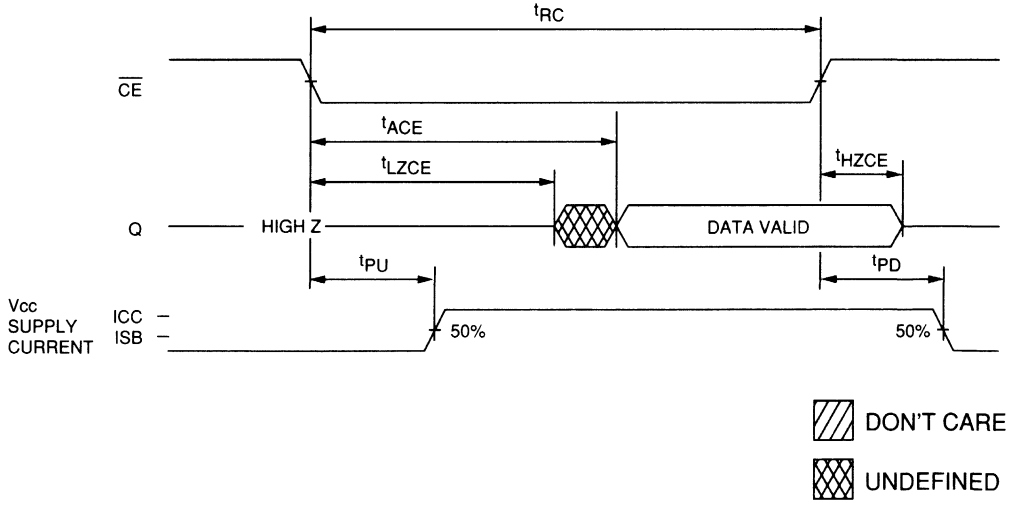
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 (NOTES 8, 9)



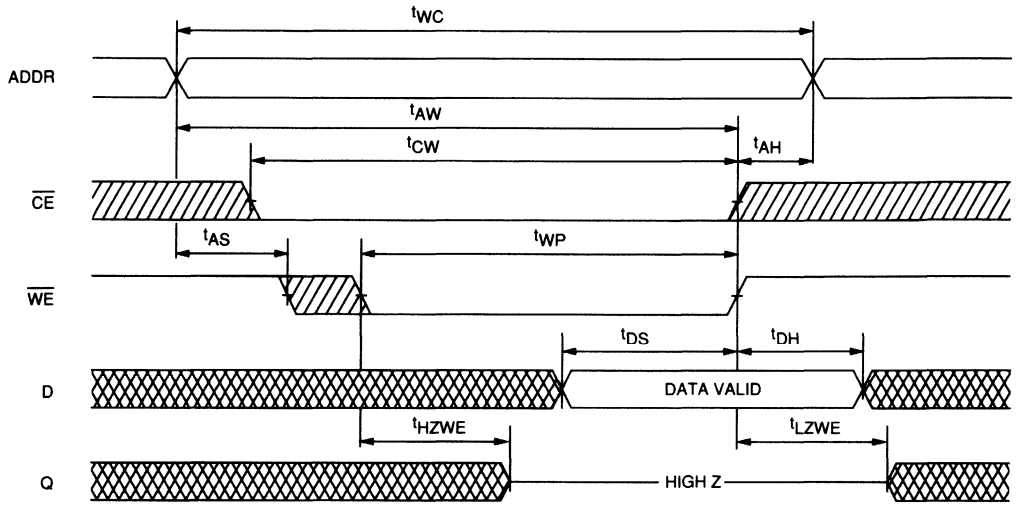
READ CYCLE NO. 2 (NOTES 7, 8, 10)



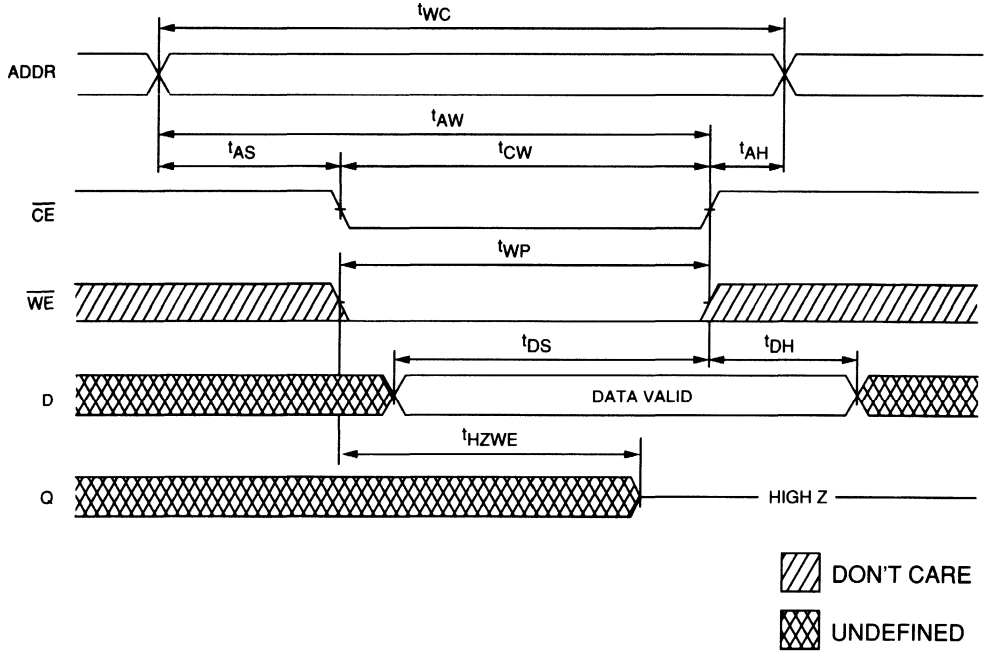
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



SRAM

256K x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

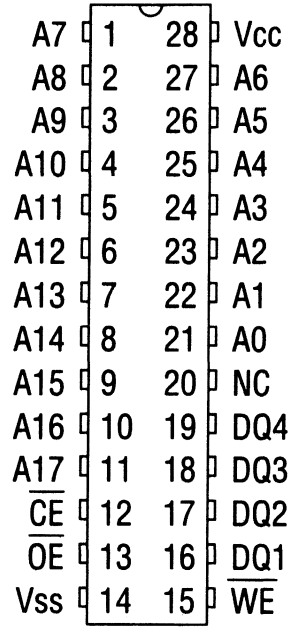
- High speed: 25, 35 and 45ns
- Automatic chip enable power down
- All inputs and outputs are TTL compatible
- High performance, low power, CMOS process
- Single +5V (±10%) power supply
- Low power, ICC (max.) 70mA

OPTIONS

	MARKING
• Timing	
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP	None
Ceramic DIP	C
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

28L/DIP



GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. Output enable ($\overline{OE}$) is an enhancement available and can place the output in a high impedance state for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. $\overline{OE}$ must also be LOW to read the device. The devices offer a reduced power standby mode when disabled. This allows system designs for low power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

SRAM

1MEG x 1 SRAM

FEATURES

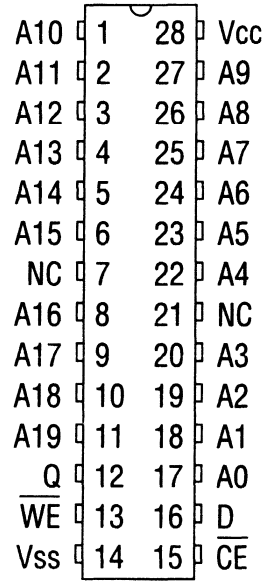
- High speed: 25, 35 and 45ns
- Automatic chip enable power down
- All inputs and outputs are TTL compatible
- High performance, low power, CMOS process
- Single +5V (±10%) power supply
- Low power, ICC (max.) 70mA

OPTIONS

OPTIONS	MARKING
• Timing	
25ns access	-25
35ns access	-35
45ns access	-45
• Packages	
Plastic DIP	None
Ceramic DIP	C
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

28L/DIP



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The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. The x 1 organization features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The devices offer a reduced power standby mode when disabled. This allows system designs for low power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

DYNAMIC RAMs 1
DYNAMIC RAM MODULES 2
MULTIPORT DYNAMIC RAMs 3
STATIC RAMs 4
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MILITARY INFORMATION 9
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SRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Package and No. of Pins		
				DIP	Process	Page
32K X16	CE & OE	MT85C1632	30, 35, 45ns	40	CMOS	5-3
64K X16	CE & OE	MT85C1664	30, 35, 45ns	40	CMOS	5-11
128K X 8	CE & OE	MT85C8128	30, 35, 45ns	32	CMOS	5-19

SRAM MODULE

32K x 16 SRAM

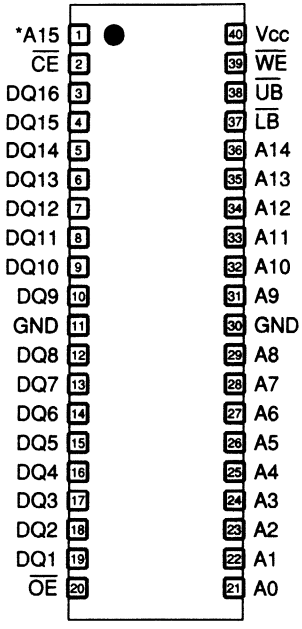
FEATURES

- High speed: 30ns, 35ns and 45ns
- High performance, low power, CMOS process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ function
- Upper and Lower Byte Select
- All inputs and outputs are TTL compatible

OPTIONS	MARKING
• Timing	
30ns access	-30
35ns access	-35
45ns access	-45
• Packages:	
40-pin DIP (600 mil)	None
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

40 PIN DIP
(MT)



* Address A15 must be connected to Vss

GENERAL DESCRIPTION

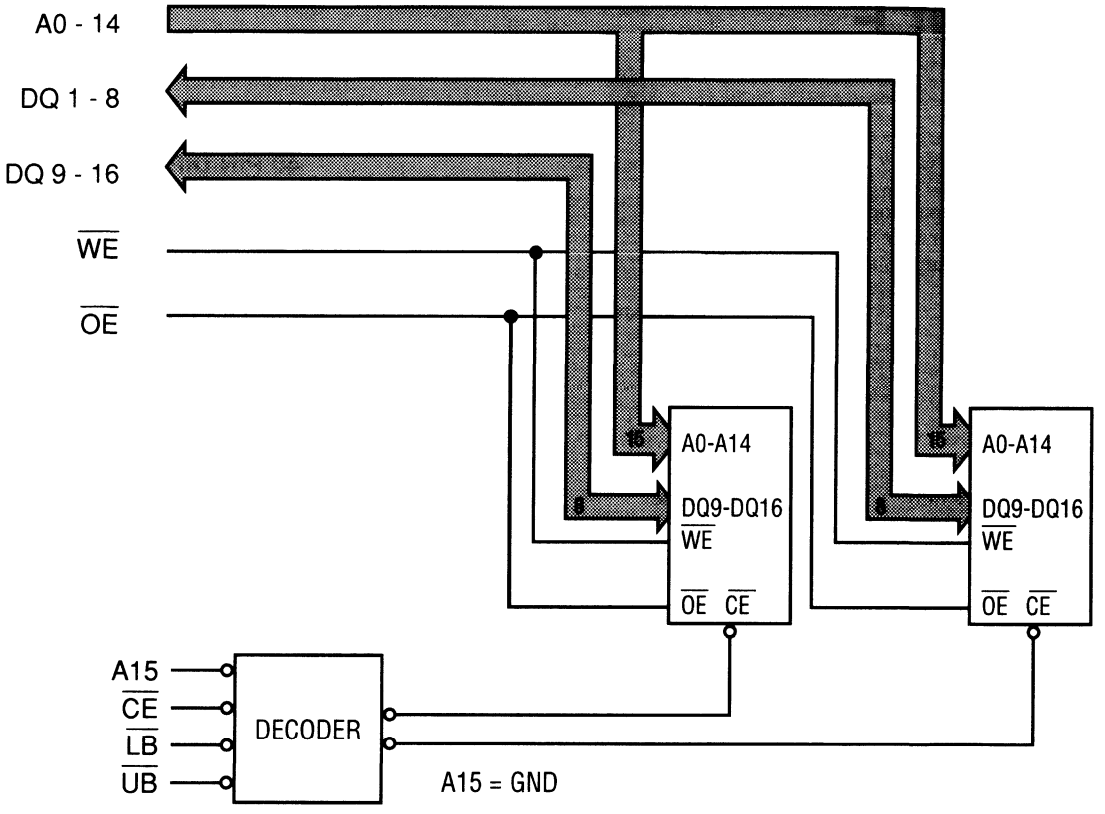
The MT85C1632 is a high speed SRAM memory module containing 32,768 words organized in a x16-bit configuration. The Micron DIP style module is manufactured using two 32Kx8 fast static RAMs together with a CMOS decoder which are mounted on a FR4 printed circuit board.

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. $\overline{LB}$ and $\overline{UB}$ control the lower and upper byte selection. $\overline{CE}$ can place the output in a high impedance state for additional flexibility in system design. Memory expansion is accomplished by use of the output enable ($\overline{OE}$) function. Address bit (A15) should be externally grounded for proper operation.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible. The L option offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	CE	UB	LB	OE	WE	A15	DQ OPERATION	POWER
STANDBY	H	X	X	X	X	L	HIGH Z	STANDBY
STANDBY	L	H	H	X	X	L	HIGH Z	STANDBY
READ: WORD	L	L	L	L	H	L	Q (1-16)	ACTIVE (X16)
READ: LOWER BYTE	L	H	L	L	H	L	Q (1-8)	ACTIVE (X8)
READ: UPPER BYTE	L	L	H	L	H	L	Q (9-16)	ACTIVE (X8)
READ: WORD	L	L	L	H	H	L	HIGH Z	ACTIVE (X16)
READ: LOWER BYTE	L	H	L	H	H	L	HIGH Z	ACTIVE (X8)
READ: UPPER BYTE	L	L	H	H	H	L	HIGH Z	ACTIVE (X8)
WRITE: WORD	L	L	L	X	L	L	D (1-16)	ACTIVE (X16)
WRITE: LOWER BYTE	L	H	L	X	L	L	D (1-8)	ACTIVE (X8)
WRITE: UPPER BYTE	L	L	H	X	L	L	D (9-16)	ACTIVE (X8)

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	$V_{CC}+1$	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Operating in x16 Mode	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CCx16}		290	mA	3
Power Supply Current: Operating in x8 Mode	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CCx8}		180	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max.	I_{SB1}		110	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}		20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		32	pF	4
Output Capacitance	V_{CC} = 5V	C_O		32	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	SYM	-30		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle									
READ cycle time	t_{RC}	30		35		45		ns	
Address access time	t_{AA}		30		35		45	ns	
Chip Enable access time	t_{ACE}		30		35		45	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip Enable LOW to output in low Z	t_{LZCE}	5		5		5		ns	7
Chip Enable to output in high Z	t_{HZCE}		20		20		25	ns	6, 7
Chip Enable LOW to power up time	t_{PU}	0		0		0		ns	
Chip Enable HIGH to power down time	t_{PD}		30		35		45	ns	
Output Enable Access Time	t_{AOE}		20		20		25	ns	
Output Enable LOW to output in low Z	t_{LZOE}	0		0		0		ns	
Output Enable HIGH to output in high Z	t_{HZOE}		20		20		30	ns	
WRITE Cycle									
WRITE cycle time	t_{WC}	30		35		45		ns	
Chip enable to end of write	t_{CW}	25		30		30		ns	
Address Valid to end of write	t_{AW}	25		25		30		ns	
Address set-up time	t_{AS}	0		0		0		ns	
Address hold from end of write	t_{AH}	2		2		2		ns	
Write pulse width	t_{WP}	25		25		30		ns	
Data set-up time	t_{DS}	15		15		18		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write Enable LOW to output in low Z	t_{LZWE}	0		0		0		ns	
Write Enable HIGH to output in high Z	t_{HZWE}	0	20	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

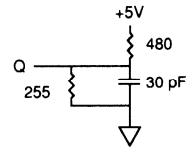


Fig. 1 OUTPUT LOAD EQUIVALENT

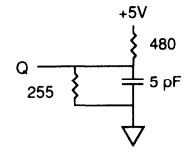


Fig. 2 OUTPUT LOAD EQUIVALENT

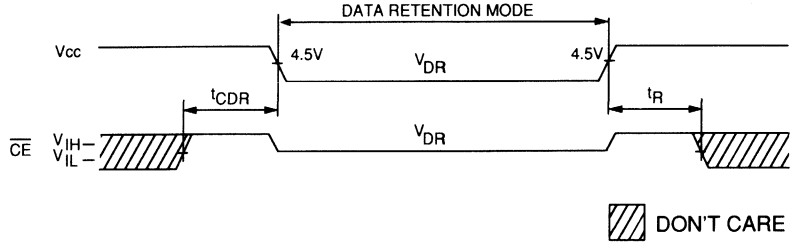
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.

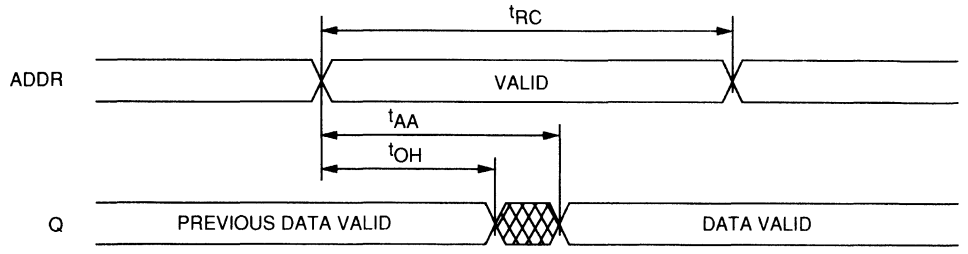
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	ICCDR		0.9	4	mA	
		Vcc=3v			1.9	5	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4

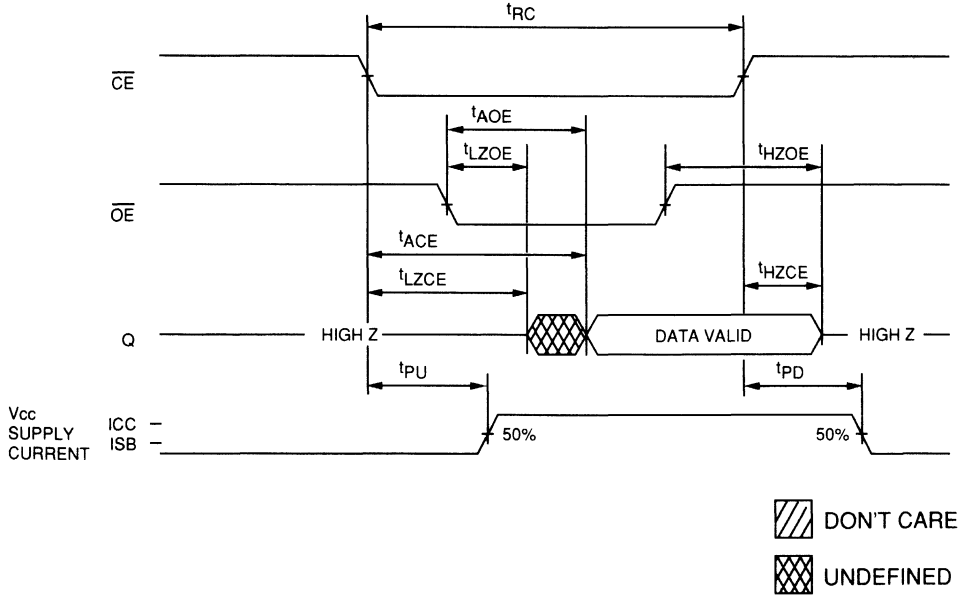
LOW Vcc DATA RETENTION WAVEFORM



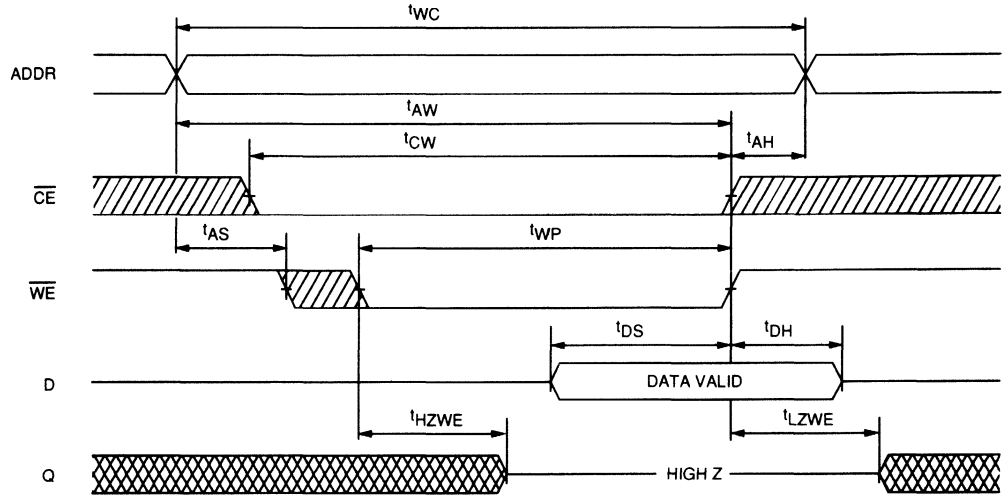
READ CYCLE NO. 1 (Notes 8, 9)



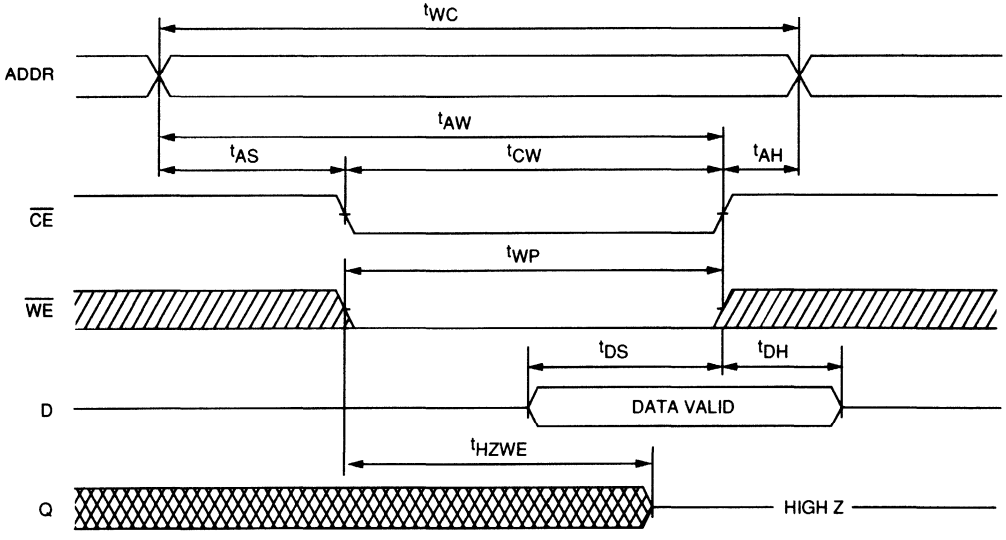
READ CYCLE NO. 2 (Notes 7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



DON'T CARE

UNDEFINED

SRAM MODULE

64K x 16 SRAM

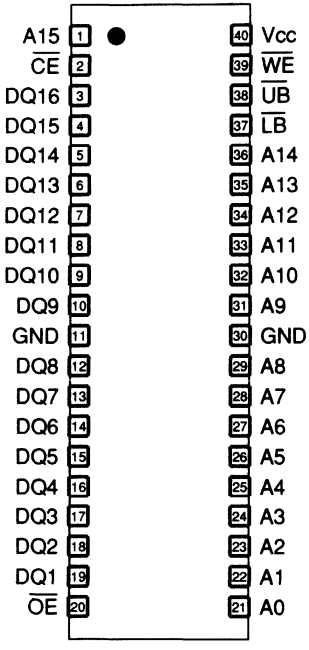
FEATURES

- High speed: 30ns, 35ns and 45ns
- High performance, low power, CMOS process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ function
- Upper and Lower Byte Select
- All inputs and outputs are TTL compatible

OPTIONS	MARKING
• Timing	
30ns access	-30
35ns access	-35
45ns access	-45
• Packages:	
40-pin DIP (600 mil)	None
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

40 PIN DIP
(MS)



GENERAL DESCRIPTION

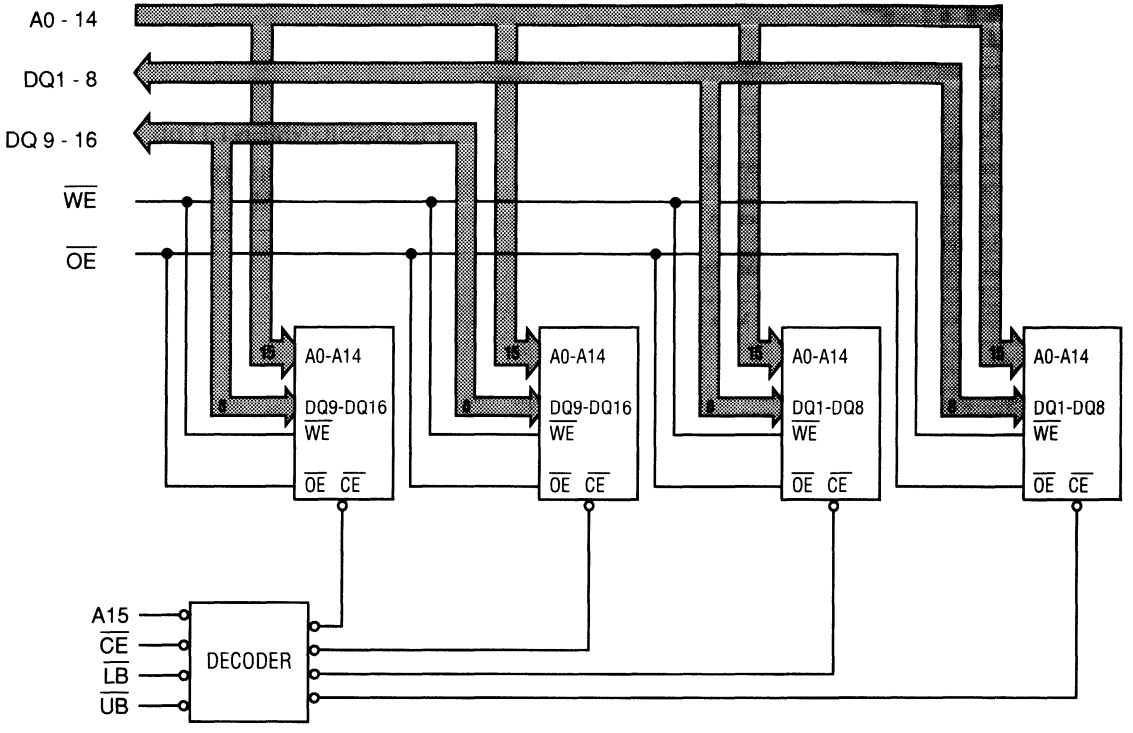
The MT85C1664 is a high speed SRAM memory module containing 65,536 words organized in a x16-bit configuration. The Micron DIP style module is manufactured using four 32Kx8 fast static RAMs together with a CMOS decoder mounted on a FR4 printed circuit board.

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. The CMOS decoder is used to interpret the high order address bit (A15) to select two of the four fast static RAMs. $\overline{LB}$ and $\overline{UB}$ control the lower and upper byte selection. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. $\overline{CE}$ can place the output in a high impedance state for additional flexibility in system design. Memory expansion is accomplished by use of the output enable ($\overline{OE}$) function.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible. The L option offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	DQ OPERATION	POWER
STANDBY	H	X	X	X	X	HIGH Z	STANDBY
STANDBY	L	H	H	X	X	HIGH Z	STANDBY
READ: WORD	L	L	L	L	H	Q (1-16)	ACTIVE (X16)
READ: LOWER BYTE	L	H	L	L	H	Q (1-8)	ACTIVE (X8)
READ: UPPER BYTE	L	L	H	L	H	Q (9-16)	ACTIVE (X8)
READ: WORD	L	L	L	H	H	HIGH Z	ACTIVE (X16)
READ: LOWER BYTE	L	H	L	H	H	HIGH Z	ACTIVE (X8)
READ: UPPER BYTE	L	L	H	H	H	HIGH Z	ACTIVE (X8)
WRITE: WORD	L	L	L	X	L	D (1-16)	ACTIVE (X16)
WRITE: LOWER BYTE	L	H	L	X	L	D (1-8)	ACTIVE (X8)
WRITE: UPPER BYTE	L	L	H	X	L	D (9-16)	ACTIVE (X8)

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Operating in x16 Mode	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CCx16}		290	mA	3
Power Supply Current: Operating in x8 Mode	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CCx8}		180	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max.	I_{SB1}		110	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}		20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		32	pF	4
Output Capacitance	V_{CC} = 5V	C_O		32	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	SYM	-30		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle									
READ cycle time	t_{RC}	30		35		45		ns	
Address access time	t_{AA}		30		35		45	ns	
Chip Enable access time	t_{ACE}		30		35		45	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip Enable LOW to output in low Z	t_{LZCE}	5		5		5		ns	7
Chip Enable to output in high Z	t_{HZCE}		20		20		25	ns	6, 7
Chip Enable LOW to power up time	t_{PU}	0		0		0		ns	
Chip Enable HIGH to power down time	t_{PD}		30		35		45	ns	
Output Enable Access Time	t_{AOE}		20		20		25	ns	
Output Enable LOW to output in low Z	t_{LZOE}	0		0		0		ns	
Output Enable HIGH to output in high Z	t_{HZOE}		20		20		30	ns	
WRITE Cycle									
WRITE cycle time	t_{WC}	30		35		45		ns	
Chip enable to end of write	t_{CW}	25		30		30		ns	
Address Valid to end of write	t_{AW}	25		25		30		ns	
Address set-up time	t_{AS}	0		0		0		ns	
Address hold from end of write	t_{AH}	2		2		2		ns	
Write pulse width	t_{WP}	25		25		30		ns	
Data set-up time	t_{DS}	15		15		18		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write Enable LOW to output in low Z	t_{LZWE}	0		0		0		ns	
Write Enable HIGH to output in high Z	t_{HZWE}	0	20	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

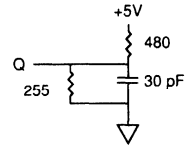


Fig. 1 OUTPUT LOAD EQUIVALENT

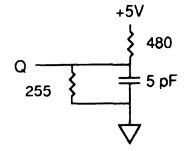


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

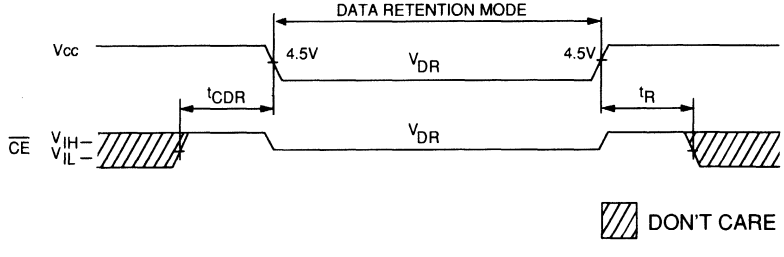
1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.

SRAM MODULE

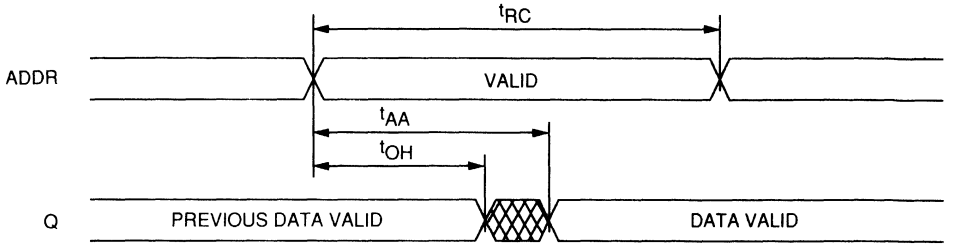
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) VIN ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	I_{CCDR}		0.9	4	mA	
		Vcc=3v			1.9	5	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4

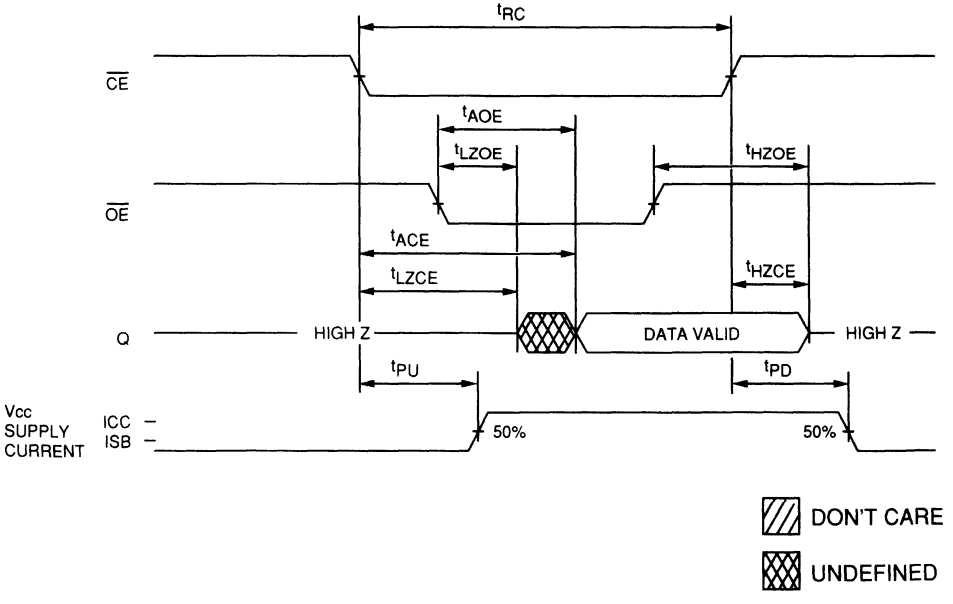
LOW Vcc DATA RETENTION WAVEFORM



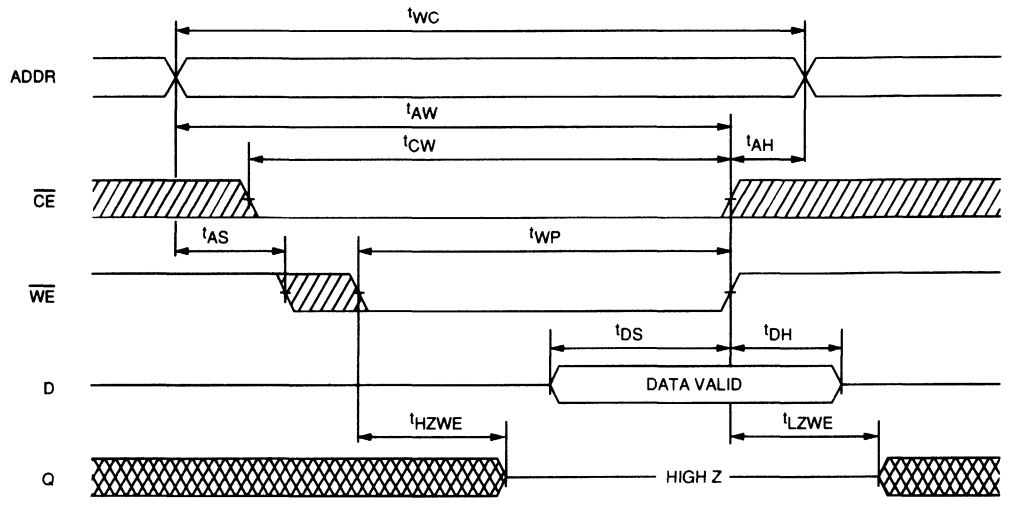
READ CYCLE NO. 1 (Notes 8, 9)



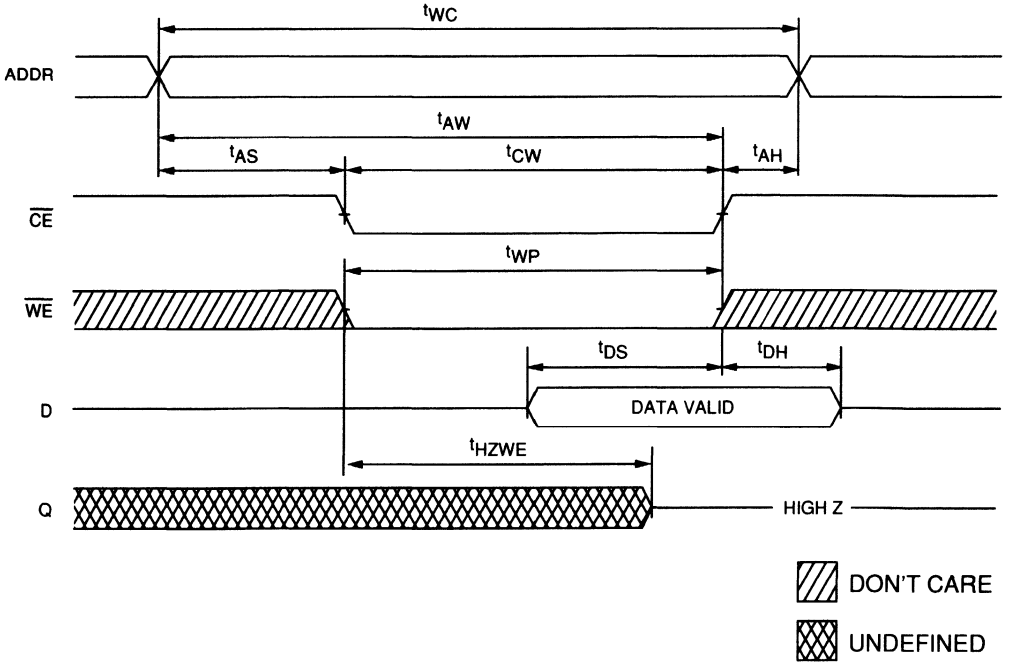
READ CYCLE NO. 2 (Notes 7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



SRAM MODULE

128K x 8 SRAM

FEATURES

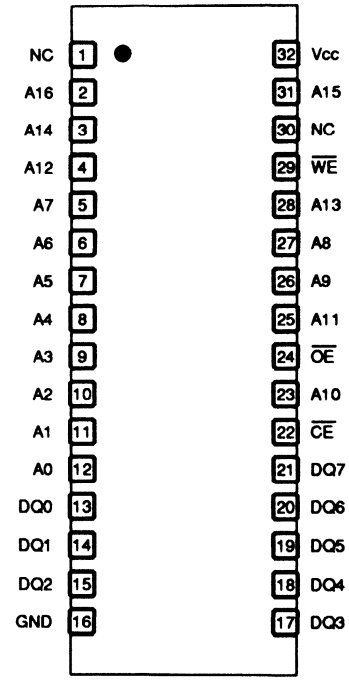
- High speed: 30ns, 35ns and 45ns
- High performance, low power, CMOS process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ function
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
30ns access	-30
35ns access	-35
45ns access	-45
• Packages:	
32-pin DIP (600 mil)	None
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

32 PIN DIP
(MR)



GENERAL DESCRIPTION

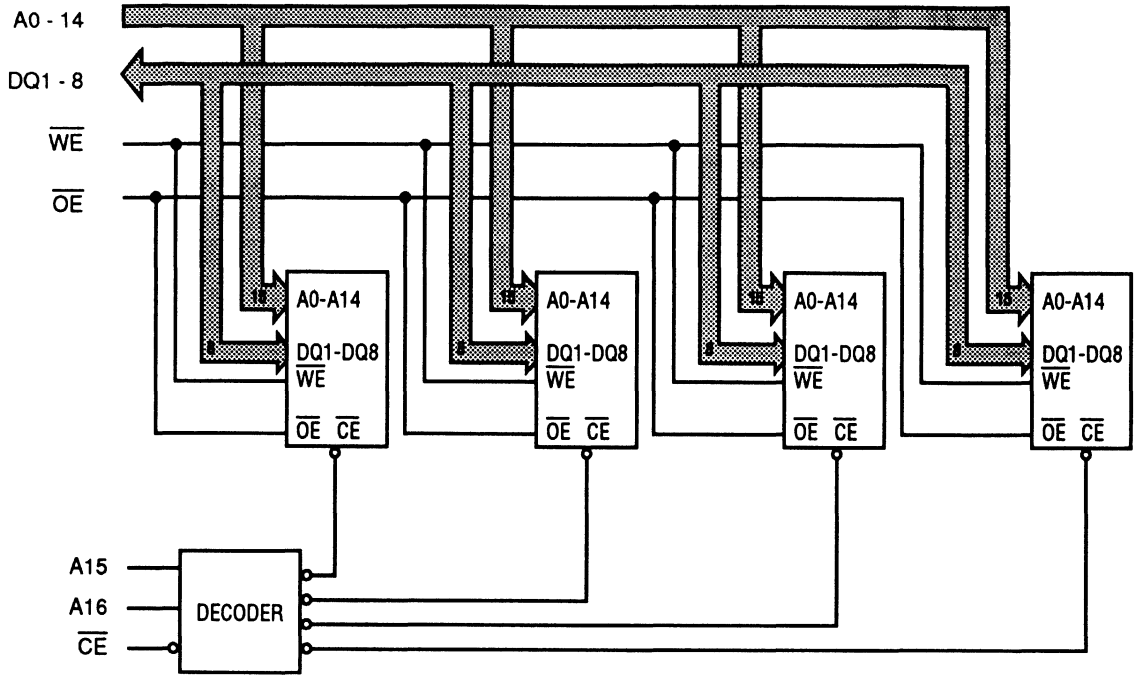
The MT85C8128 is a high speed SRAM memory module containing 131,072 words organized in a x8-bit configuration. The Micron DIP style module is manufactured using four 32Kx8 fast static RAMs together with a TTL (30ns and 35ns) or CMOS (45ns) decoder mounted on a FR4 printed circuit board.

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and chip enable $\overline{CE}$ inputs are both LOW. The CMOS decoder is used to interpret the higher order address bits (A15-16) to select one of the four fast static RAMs. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. $\overline{CE}$ can place the output in a high impedance state for additional flexibility in system design. Memory expansion is accomplished by use of the output enable ($\overline{OE}$) funtion.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible. The L option offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	-30, -35	-45	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.2	Vcc+1	Vcc+1	V	1
Input Low (Logic 0) Voltage			V_{IL}	-0.5	0.8	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	A0-A14	I_{LI}	-10	10	10	µA	
		A15, A16, $\overline{CE}$		-10	600	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$		I_{LO}	-10	10	10	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		10	V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	0.4	V	1

					MAX			
DESCRIPTION	CONDITIONS	SYMBOL	MIN	-30, -35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}		180	160	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max.	I_{SB1}		110	110	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max., $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}		40	20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		32	pF	4
Output Capacitance	V_{CC} = 5V	C_O		32	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \leq T_A \leq 70°C$, Vcc = 5V ± 10%)

DESCRIPTION	SYM	-30		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle									
READ cycle time	^tRC	30		35		45		ns	
Address access time	^tAA		30		35		45	ns	
Chip Enable access time	^tACE		30		35		45	ns	
Output hold from address change	^tOH	5		5		5		ns	
Chip Enable LOW to output in low Z	^tLZCE	5		5		5		ns	7
Chip Enable to output in high Z	^tHZCE		20		20		25	ns	6, 7
Chip Enable LOW to power up time	^tPU	0		0		0		ns	
Chip Enable HIGH to power down time	^tPD		30		35		45	ns	
Output Enable Access Time	^tAOE		20		20		25	ns	
Output Enable LOW to output in low Z	^tLZOE	0		0		0		ns	
Output Enable HIGH to output in high Z	^tHZOE		20		20		30	ns	
WRITE Cycle									
WRITE cycle time	^tWC	30		35		45		ns	
Chip enable to end of write	^tCW	25		30		30		ns	
Address Valid to end of write	^tAW	25		25		30		ns	
Address set-up time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	2		2		2		ns	
Write pulse width	^tWP	25		25		30		ns	
Data set-up time	^tDS	15		15		18		ns	
Data hold time	^tDH	0		0		0		ns	
Write Enable LOW to output in low Z	^tLZWE	0		0		0		ns	
Write Enable HIGH to output in high Z	^tHZWE	0	20	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

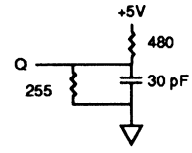


Fig. 1 OUTPUT LOAD EQUIVALENT

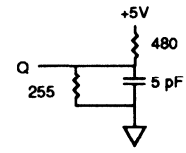


Fig. 2 OUTPUT LOAD EQUIVALENT

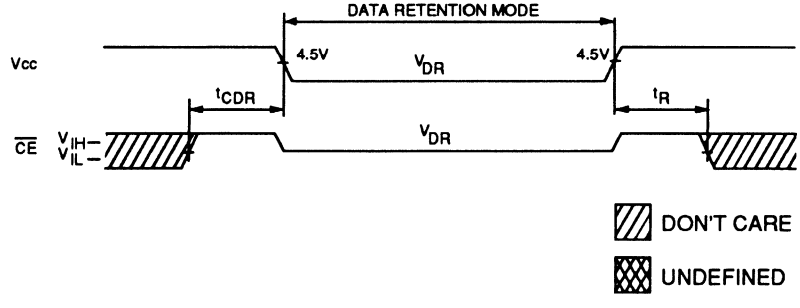
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.

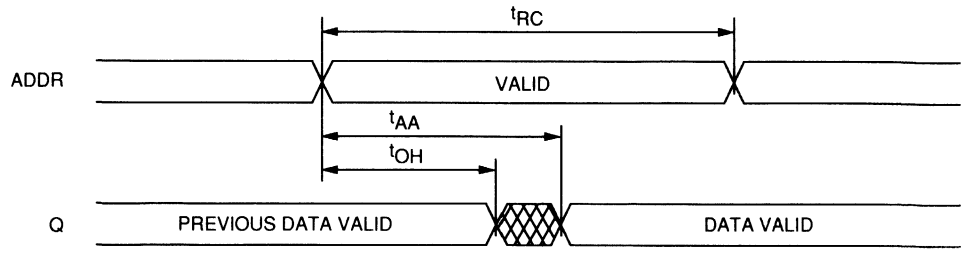
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) V_{IN} ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	I_{CCDR}		.9	4	mA	
		Vcc=3v			1.9	5	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 10

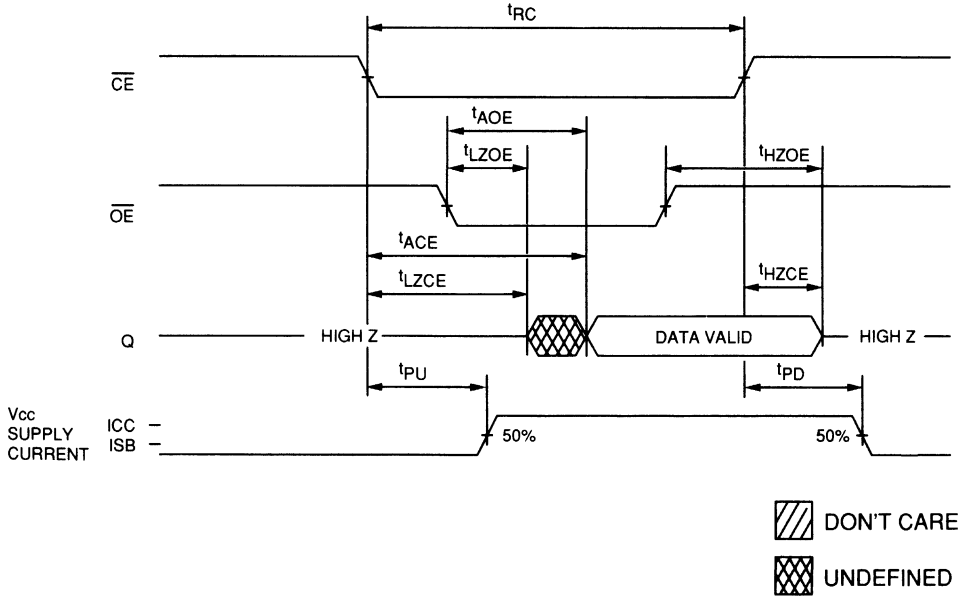
LOW Vcc DATA RETENTION WAVEFORM



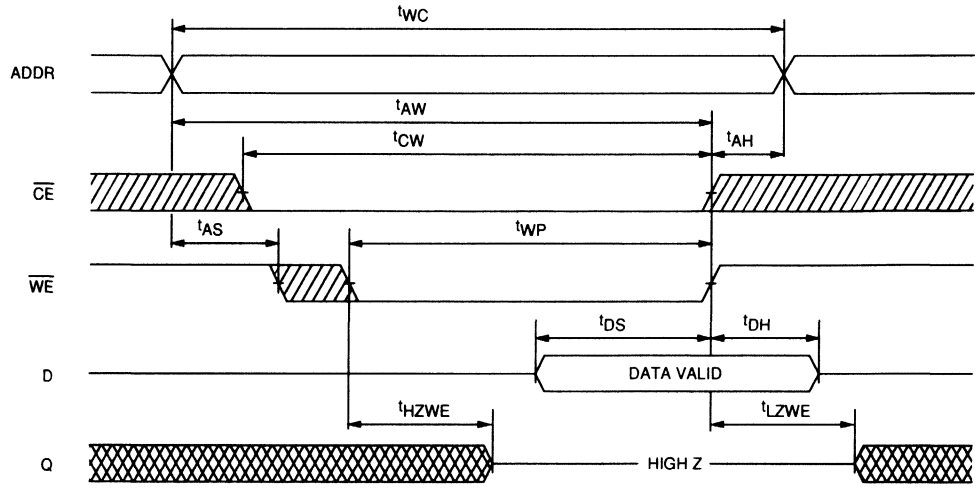
READ CYCLE NO. 1 (Notes 8, 9)



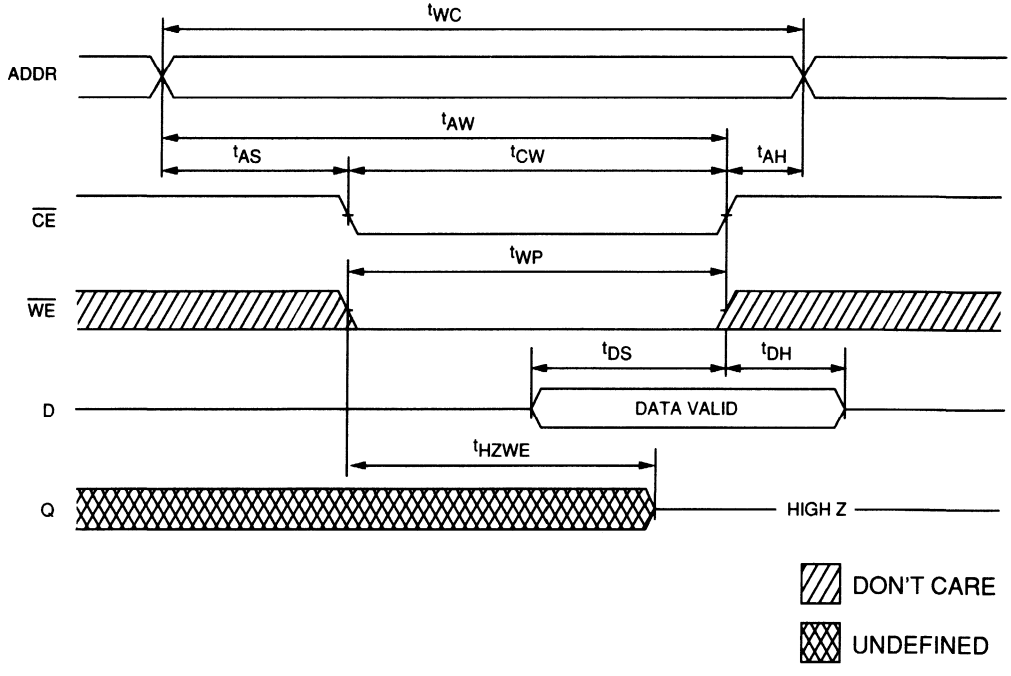
READ CYCLE NO. 2 (Notes 7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



MICRON

DYNAMIC RAMs 1

DYNAMIC RAM MODULES 2

MULTIPORT DYNAMIC RAMs 3

STATIC RAMs 4

STATIC RAM MODULES 5

CACHE DATA RAMs 6

FIFO MEMORIES 7

APPLICATION INFORMATION 8

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PACKAGE INFORMATION 10

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CACHE DATA RAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package PLCC	Process	Page
Dual 4K x 16 or Single 8K x 16	Mode, Byte Select CE, OE Address Latch	MT56C0816	25, 35, 45	52	CMOS	6-3
Dual 4K x 18 or Single 8K x 18	Mode, Byte Select CE, OE Address Latch	MT56C0818	25, 35, 45	52	CMOS	6-13

CACHE DATA STATIC RAM

DUAL 4K x 16 SRAM, SINGLE 8K x 16 SRAM

CONFIGURABLE CACHE DATA SRAM

FEATURES

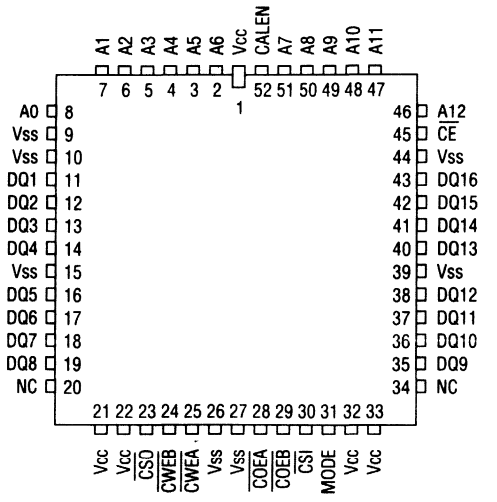
- Operates as two 4K x 16 SRAMs with common addresses and data; also configurable as a single 8K x 16 SRAM
- Built-in input address latches
- Separate upper and lower Byte Select
- Fast access times: 25ns, 35ns and 45ns allows operation with 33, 25, and 20 MHz microprocessor systems
- Fast output enable: 10ns
- Directly interfaces with the Intel 82385 cache memory controller and 80386 microprocessor

OPTIONS

	MARKING
• Timing	
25ns access (33 MHz)	-25
35ns access (25 MHz)	-35
45ns access (20 MHz)	-45
• Packages	
52-pin PLCC	EJ

PIN ASSIGNMENT (Top View)

52 Pin LCC
(EJB)



GENERAL DESCRIPTION

The MT56C0816 is one of a family of fast SRAM cache memories. It employs a high speed, low power design using a 4-transistor memory cell. It is fabricated using double layer polysilicon, double layer metal CMOS technology.

The MT56C0816 is a highly integrated cache data memory building block. It easily interfaces with the Intel 82385 cache controller in either the direct mapped or two-way set associative mode. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K word by 16 bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K word by 16 bit SRAM.

Input addresses are latched in the on-chip register on the negative edge of the CALEN signal. This register is functionally equivalent to a 74LS373.

The memory functions are controlled by the chip select ($\overline{CE}$, $\overline{CS0}$ and $\overline{CS1}$), output enable ($\overline{COEA}$ and $\overline{COEB}$) and write enable ($\overline{CWEA}$ and $\overline{CWEB}$) signals.

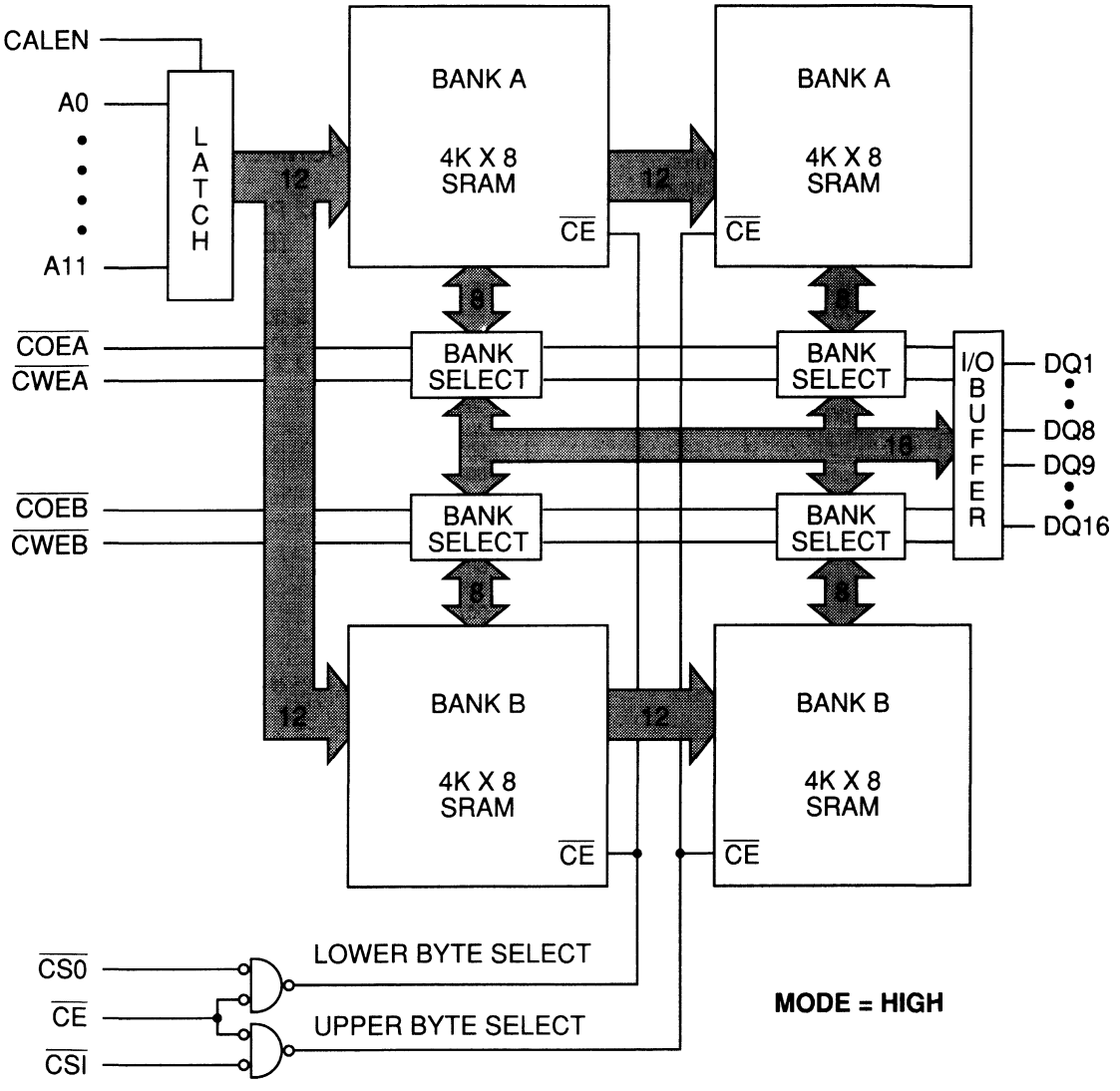
In either the direct mapped (direct) or two-way set associative (dual) operational modes, $\overline{CE}$ is a global chip enable, while $\overline{CS0}$ and $\overline{CS1}$ control lower and upper byte selection for READ and WRITE operations.

Outputs are enabled on a HIGH to LOW transition of $\overline{COEA}$ or $\overline{COEB}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{COEA}$ and $\overline{COEB}$ should be connected together externally and used as a single output enable.

Write enable is activated on a HIGH to LOW transition of $\overline{CWEA}$ or $\overline{CWEB}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{CWEA}$ and $\overline{CWEB}$ should be connected together externally and used as a single write enable.

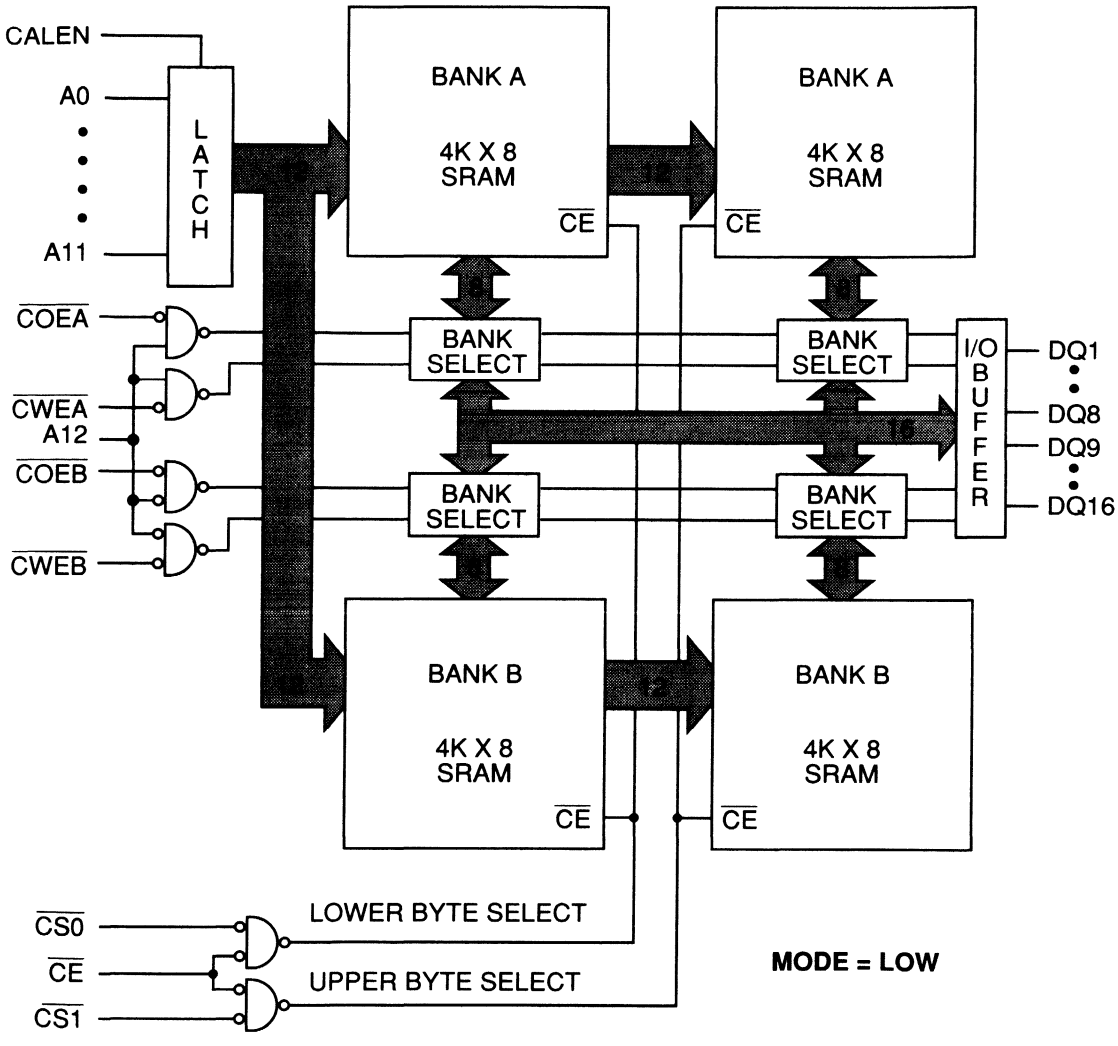
The MT56C0816 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



DUAL 4K X 16
(Two-Way Set Associative)

FUNCTIONAL BLOCK DIAGRAM



8K X 16
(Direct Map)

PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0 - A11	Input	Address Inputs: These inputs are clocked by CALEN and stored in a latch.
46	A12	Input	Address Input: This input is the high order address bit in the direct 8K X 16 configuration. It is not used in the dual 4K X 16 configuration.
52	CALEN	Input	Address Latch Enable: When CALEN is HIGH, the latch is transparent. The negative edge latches the current address inputs (A0-A11).
31	MODE	Input	MODE Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K X 16 configuration. When the pin is tied LOW, the device is configured as an 8K X 16 SRAM.
23, 30	$\overline{CS0}$, $\overline{CS1}$	Input	CHIP SELECTS: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{CS0}$ is LOW, DQ1-DQ8 are enabled. When $\overline{CS1}$ is LOW, DQ9-DQ16 are enabled.
45	$\overline{CE}$	Input	CHIP ENABLE: When $\overline{CE}$ is LOW, the device is enabled. It is a global control signal that activates both bank A and bank B for READ or WRITE operations.
28, 29	$\overline{COEA}$, $\overline{COEB}$	Input	OUTPUT ENABLE: In the dual configuration these signals, whichever is LOW enables bank A or B. Simultaneous LOW assertion will deselect both banks. In the direct mode, these signals should be externally connected and when asserted LOW allows A12 to determine which memory bank is enabled.
25, 24	$\overline{CWEA}$, $\overline{CWEB}$	Input	WRITE ENABLE: In the dual configuration these signals, whichever is LOW enables a data write to the addressed memory location. In the direct mode, these signals should be externally connected and when asserted LOW allows A12 to determine which memory bank is written.
11, 12, 13, 14, 16 17, 18, 19, 35, 36, 37 38, 40, 41, 42, 43	DQ1 - DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1 - DQ8; upper byte is DQ9 - DQ16.
1, 21, 22, 32, 33,	Vcc	Supply	Power Supply: +5V ± 5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE

DUAL 4K X 16 (MODE PIN = HIGH)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs high-Z, Write disabled	H	X	X	X	X	X	X
Outputs high-Z, Write disabled	X	H	H	X	X	X	X
Outputs high-Z	X	X	X	H	H	X	X
Outputs high-Z	X	X	X	L	L	X	X
Read DQ1 - DQ8 bank A	L	L	H	L	H	H	H
Read DQ1 - DQ8 bank B	L	L	H	H	L	H	H
Read DQ9 - DQ16 bank A	L	H	L	L	H	H	H
Read DQ9 - DQ16 bank B	L	H	L	H	L	H	H
Read DQ1 - DQ16 bank A	L	L	L	L	H	H	H
Read DQ1 - DQ16 bank B	L	L	L	H	L	H	H
Write DQ1 - DQ8 bank A	L	L	H	X	X	L	H
Write DQ1 - DQ8 bank B	L	L	H	X	X	H	L
Write DQ9 - DQ16 bank A	L	H	L	X	X	L	H
Write DQ9 - DQ16 bank B	L	H	L	X	X	H	L
Write DQ1 - DQ16 bank A	L	L	L	X	X	L	H
Write DQ1 - DQ16 bank B	L	L	L	X	X	H	L
Write DQ1 - DQ8 bank A & B	L	L	H	X	X	L	L
Write DQ9 - DQ16 bank A & B	L	H	L	X	X	L	L
Write DQ1 - DQ16 bank A & B	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ or $\overline{CWEB}$ remain active, allows a chip enable controlled WRITE to be performed.

TRUTH TABLE

8K X 16 (MODE PIN = LOW)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs high-Z, Write disabled	H	X	X	X	X	X	X
Outputs high-Z, Write disabled	X	H	H	X	X	X	X
Outputs high-Z	X	X	X	H	H	X	X
Read DQ1 - DQ8	L	L	H	L	L	H	H
Read DQ9 - DQ16	L	H	L	L	L	H	H
Read DQ1 - DQ16	L	L	L	L	L	H	H
Write DQ1 - DQ8	L	L	H	X	X	L	L
Write DQ9 - DQ16	L	H	L	X	X	L	L
Write DQ1 - DQ16	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ and $\overline{CWEB}$ remain active, allows a chip enable controlled WRITE to be performed.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1.2 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 5\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		V_{CC}	4.75	5.25	V	
Input High Voltage		V_{IH}	2.2	V_{CC}+0.3	V	1
Input Low Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	V_{IN} = GND to V_{CC}	I_{LI}	-10	10	µA	
Output Leakage Current	$V_{I/O}$ = GND to V_{CC} $\overline{CS0}$, $\overline{CS1}$ = V_{IL} or $\overline{COEA}$, $\overline{COEB}$ & $\overline{CWEA}$, $\overline{CWEB}$ = V_{IL}	I_{LO}	-10	10	µA	
Output Low Voltage	I_{OL} = 4.0mA	V_{OL}		0.4	V	1
Output High Voltage	I_{OH} = -1.0mA	V_{OH}	2.4		V	1

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty cycle V_{IN} = GND to V_{CC}	I_{CC1}		220	mA	
Power Supply Current: Average Operating Current	50% Duty cycle V_{IN} = GND to V_{CC}	I_{CC2}		120	mA	
Power Supply Current: CMOS Standby	$\overline{CS0}$ = $\overline{CS1} \ge V_{CC}$ - 0.2V V_{CC} = MAX.	I_{SB}		20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_{IN}		8	pF	3
Output Capacitance	V_{CC} = 5V	$C_{I/O}$		8	pF	3

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ±5%)

DESCRIPTION		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	25		35		45		ns	4, 5
Address access time (A0-A11)	^tAA		25		35		45	ns	
A12 address access time	^tA12A		17		25		30	ns	
Chip enable access time	^tACE		20		25		35	ns	
Chip select access time	^tACS		25		35		45	ns	
Output enable access time	^tAOE		10		13		16	ns	
Output hold from address change	^tOH	3		3		3		ns	
Chip select to output low-Z	^tLZCS	3		3		3		ns	
Output enable to output low-Z	^tLZOE	2		2		2		ns	
Chip deselect to output high-Z	^tHZCS		15		25		30	ns	6
Output disable to output high-Z	^tHZOE		10		14		14	ns	6
Address latch enable pulse width	^tCALEN	8		10		15		ns	
Address setup to latch low	^tASL	4		6		10		ns	
Address hold from latch low	^tAHL	5		5		5		ns	
WRITE Cycle									
WRITE cycle time	^tWC	25		35		45		ns	
Address valid to end of write	^tAW	18		25		40		ns	
A12 address valid to end of write	^tA12W	18		25		40		ns	
Chip select to end of write	^tCW	18		25		30		ns	
Data valid to end of write	^tDW	10		10		15		ns	
Data hold from end of write	^tDH	0		0		0		ns	
Write enable output in high-Z	^tHZWE		15		15		20	ns	6
Write disable to output in low-Z	^tLZWE	3		3		3		ns	
Write pulse width	^tWP	18		25		30		ns	
$\overline{CE}$ pulse width (during chip enable controlled write)	^tCP	18		25		30		ns	
Address setup time	^tAS	0		0		0		ns	
Write recovery time	^tWR	0		0		2		ns	
Address latch enable pulse width	^tCALEN	8		10		15		ns	
Address setup to latch low	^tASL	4		6		10		ns	
Address hold from latch low	^tAHL	5		5		5		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

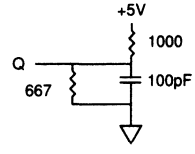


Fig. 1 OUTPUT LOAD EQUIVALENT

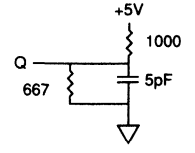
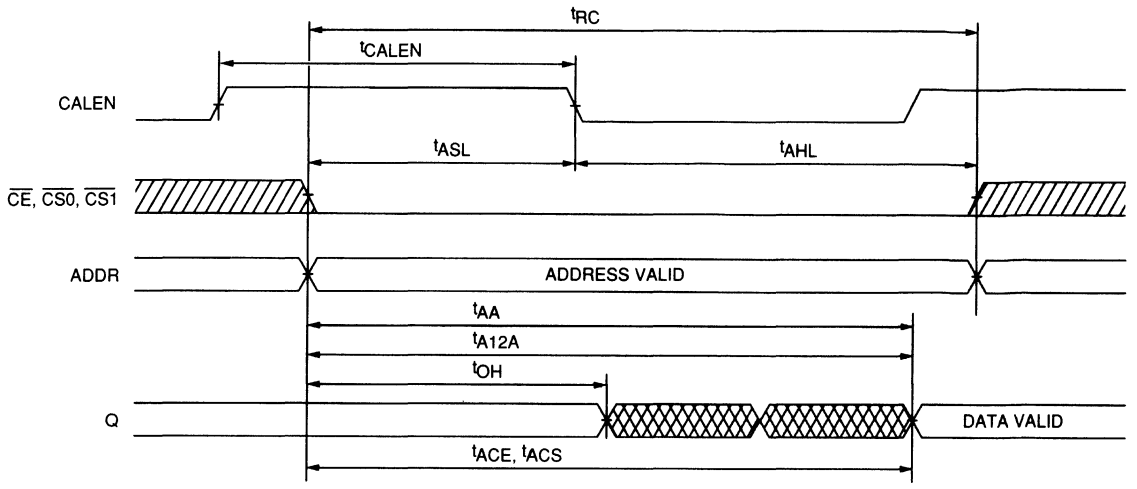


Fig. 2 OUTPUT LOAD EQUIVALENT

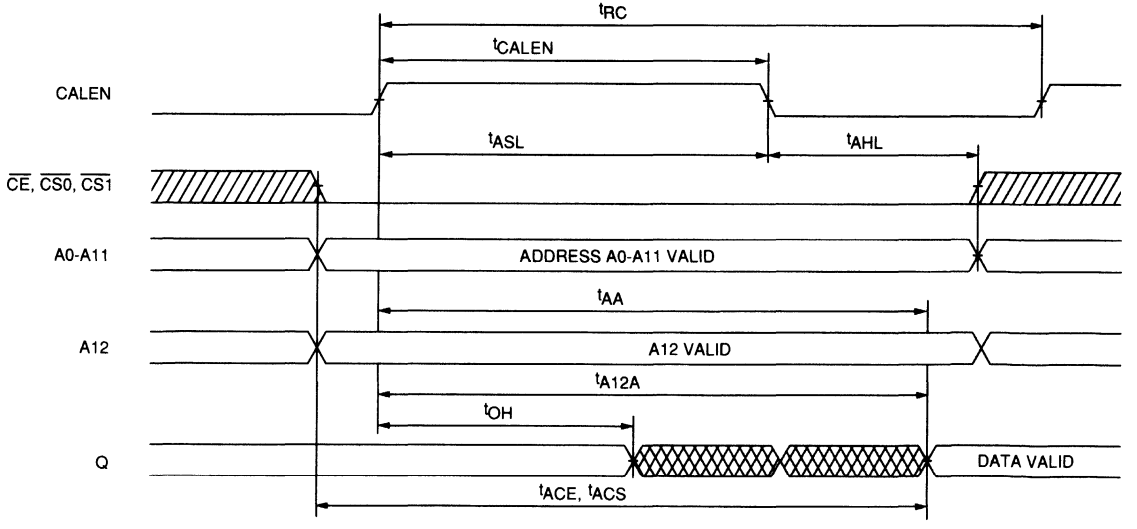
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. This parameter is sampled.
4. $\overline{CWE}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. ^tHZCS, ^tHZOE, and ^tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.

READ CYCLE NO. 1
(Address Controlled)



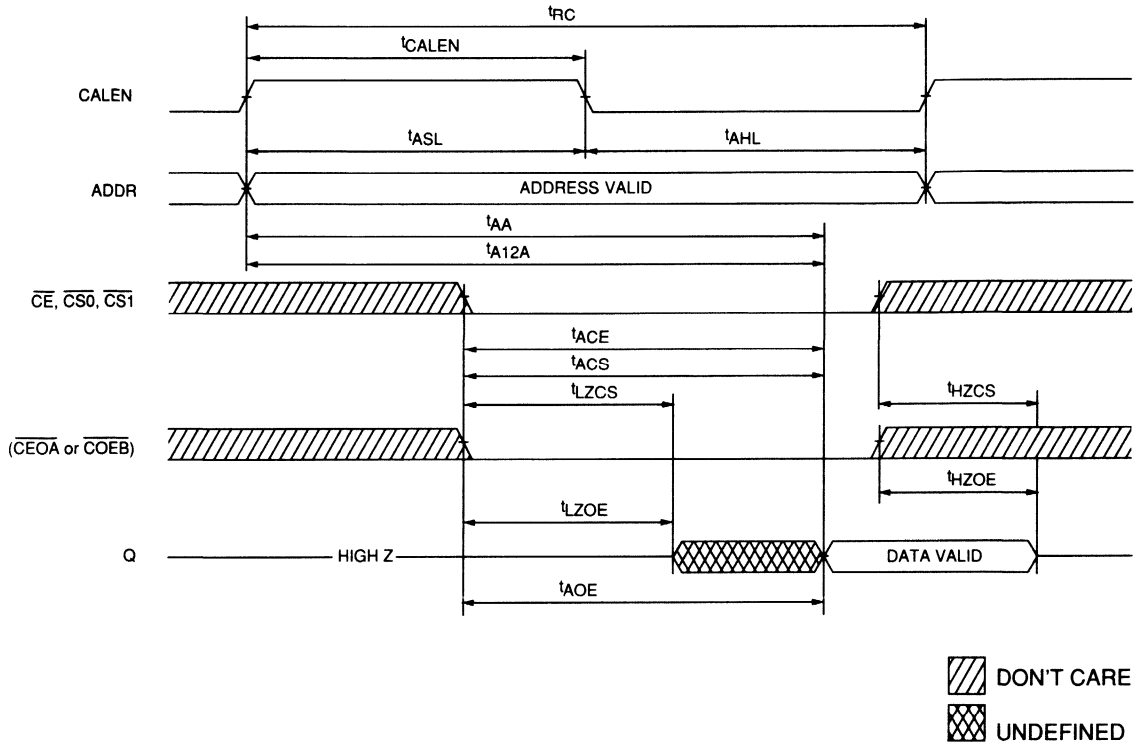
READ CYCLE NO. 2
(CALEN Controlled)



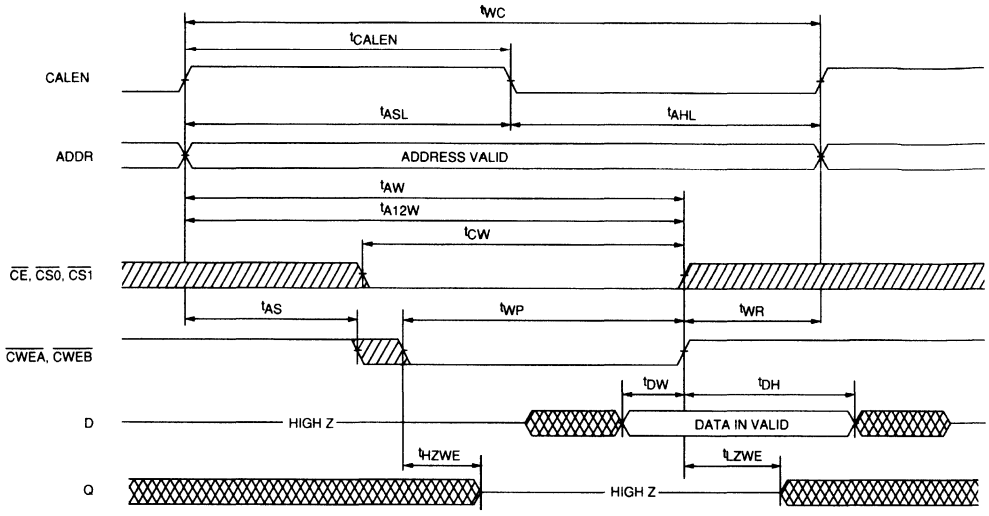
DON'T CARE

UNDEFINED

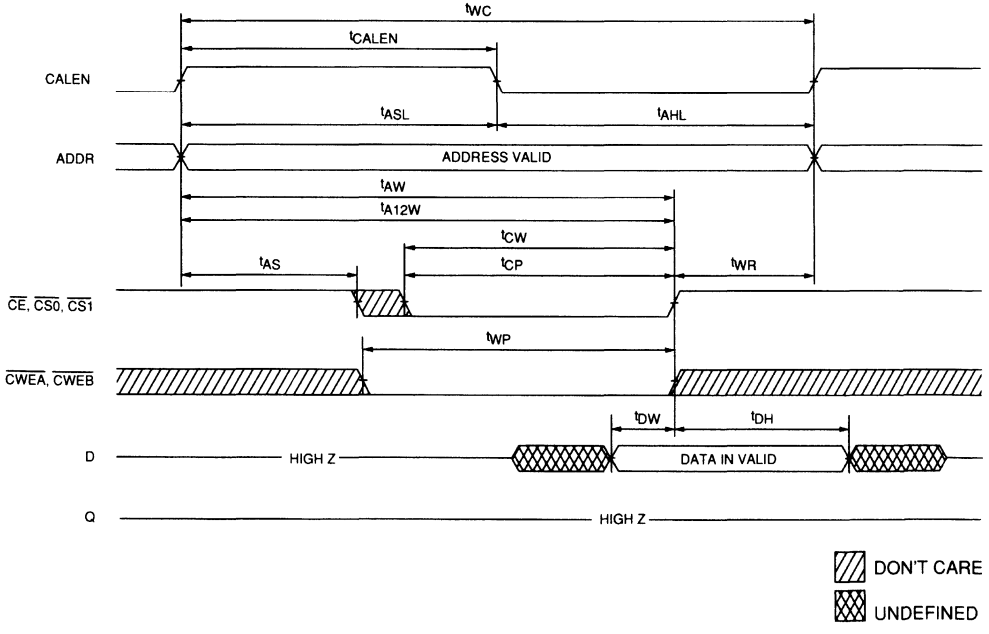
READ CYCLE NO. 3



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Select Controlled)



CACHE DATA STATIC RAM

DUAL 4K x 18 SRAM, SINGLE 8K x 18 SRAM

CONFIGURABLE CACHE DATA SRAM

FEATURES

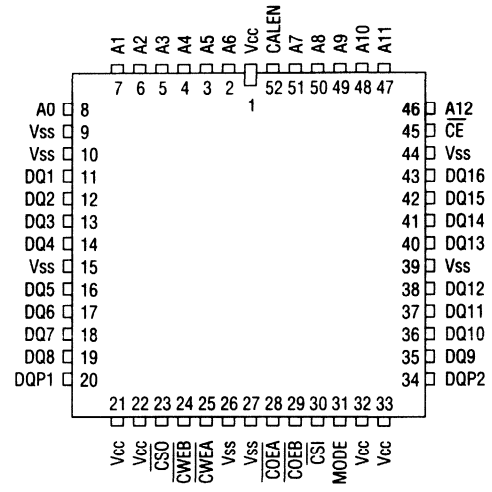
- Operates as two 4K x 18 SRAMs with common addresses and data; also configurable as a single 8K x 18 SRAM
- Built-in input address latches
- Separate upper and lower Byte Select
- Fast access times: 25ns, 35ns and 45ns allows operation with 33, 25, and 20 MHz microprocessor systems
- Fast output enable: 10ns
- Directly interfaces with the Intel 82385 cache memory controller and 80386 microprocessor
- Parity bits provided for large cache applications such as secondary cache for the 80486 microprocessor

OPTIONS

	MARKING
• Timing	
25ns access (33 MHz)	-25
35ns access (25 MHz)	-35
45ns access (20 MHz)	-45
• Packages	
52-pin PLCC	EJ

PIN ASSIGNMENT (Top View)

52 Pin LCC
(EJB)



GENERAL DESCRIPTION

The MT56C0818 is one of a family of fast SRAM cache memories. It employs a high speed, low power design using a 4-transistor memory cell. It is fabricated using double layer polysilicon, double layer metal CMOS technology.

The MT56C0818 is a highly integrated cache data memory building block. It easily interfaces with the Intel 82385 cache controller in either the direct mapped or two-way set associative mode. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K word by 18 bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K word by 18 bit SRAM.

Input addresses are latched in the on-chip register on the negative edge of the CALEN signal. This register is functionally equivalent to a 74LS373.

The memory functions are controlled by the chip select ($\overline{CE}$, $\overline{CS0}$ and $\overline{CS1}$), output enable ($\overline{COEA}$ and $\overline{COEB}$) and write enable ($\overline{CWEA}$ and $\overline{CWEB}$) signals.

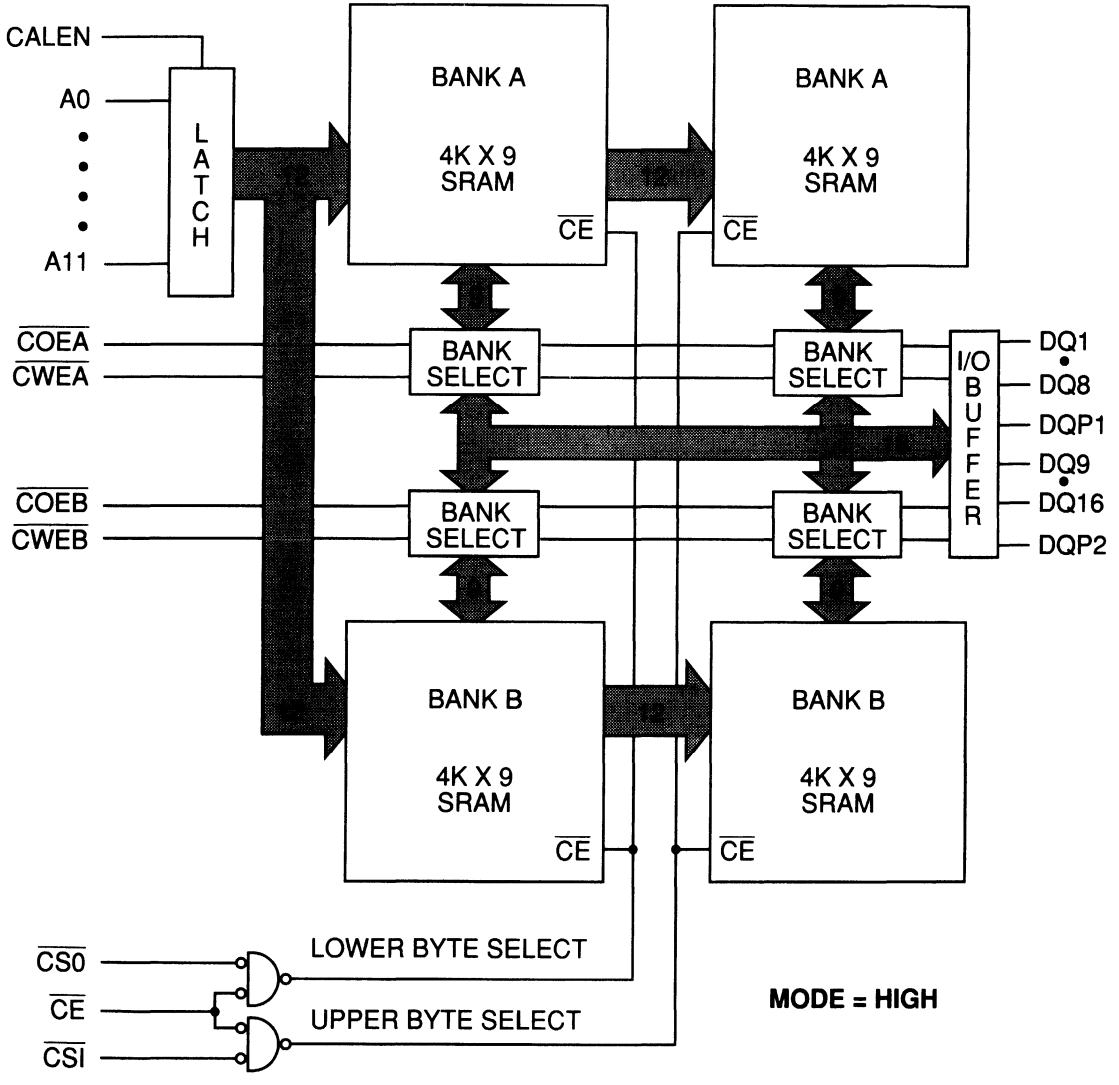
In either the direct mapped (direct) or two-way set associative (dual) operational modes, $\overline{CE}$ is a global chip enable, while $\overline{CS0}$ and $\overline{CS1}$ control lower and upper byte selection for READ and WRITE operations.

Outputs are enabled on a HIGH to LOW transition of $\overline{COEA}$ or $\overline{COEB}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{COEA}$ and $\overline{COEB}$ should be connected together externally and used as a single output enable.

Write enable is activated on a HIGH to LOW transition of $\overline{CWEA}$ or $\overline{CWEB}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{CWEA}$ and $\overline{CWEB}$ should be connected together externally and used as a single write enable.

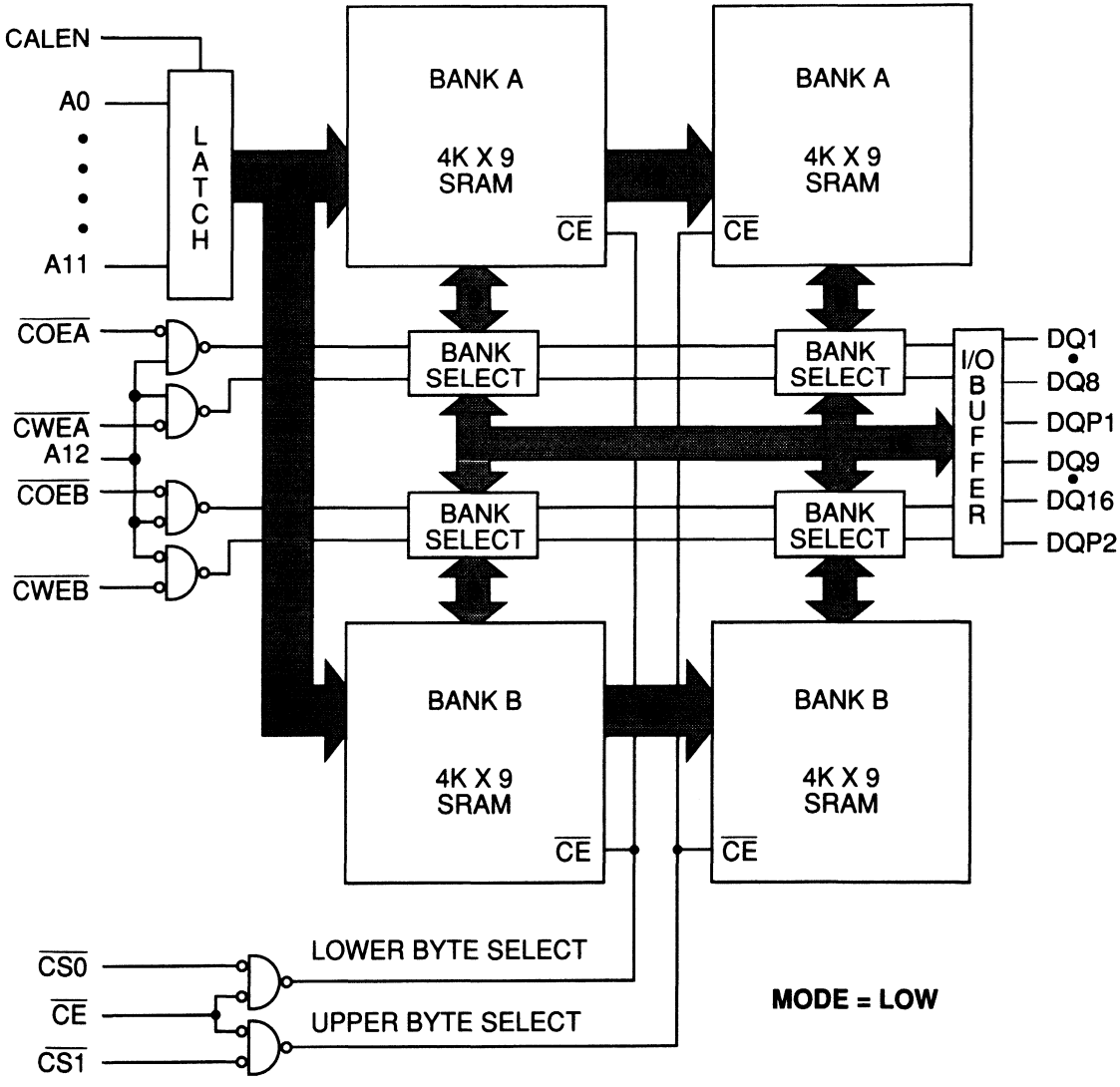
The MT56C0818 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



DUAL 4K X 18
(Two-Way Set Associative)

FUNCTIONAL BLOCK DIAGRAM



8K X 18
(Direct Map)

PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0 - A11	Input	Address Inputs: These inputs are clocked by CALEN and stored in a latch.
46	A12	Input	Address Input: This input is the high order address bit in the direct 8K X 18 configuration. It is not used in the dual 4K X 18 configuration.
52	CALEN	Input	Address Latch Enable: When CALEN is HIGH, the latch is transparent. The negative edge latches the current address inputs (A0-A11).
31	MODE	Input	MODE Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K X 18 configuration. When the pin is tied LOW, the device is configured as an 8K X 18 SRAM.
23, 30	$\overline{CS0}$, $\overline{CS1}$	Input	CHIP SELECTS: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{CS0}$ is LOW, DQ1-DQ8 and DQP1 are enabled. When $\overline{CS1}$ is LOW, DQ9-DQ16 and DQP2 are enabled.
45	$\overline{CE}$	Input	CHIP ENABLE: When $\overline{CE}$ is LOW, the device is enabled. It is a global control signal that activates both bank "A" and bank "B" for READ or WRITE operations.
28, 29	$\overline{COEA}$, $\overline{COEB}$	Input	OUTPUT ENABLE: In the dual configuration these signals, whichever is LOW enables bank "A" or "B". Simultaneous LOW assertion will deselect both banks. In the direct mode, these signals should be externally connected and when asserted LOW allows A12 to determine which memory bank is enabled.
25, 24	$\overline{CWEA}$, $\overline{CWEB}$	Input	WRITE ENABLE: In the dual configuration these signals, whichever is LOW enables a data write to the addressed memory location. In the direct mode, these signals should be externally connected and when asserted LOW allows A12 to determine which memory bank is written.
20, 34	DQP1, DQP2	Input/ Output	Parity Data I/O: DQP1 is the parity bit for the lower byte. DQP2 is the parity bit for the upper byte.
11, 12, 13, 14, 16 17, 18, 19, 35, 36, 37 38, 40, 41, 42, 43	DQ1 - DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1 - DQ8; upper byte is DQ9 - DQ16.
1, 21, 22, 32, 33,	Vcc	Supply	Power Supply: +5V ± 5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE

DUAL 4K X 18 (MODE PIN = HIGH)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs high-Z, Write disabled	H	X	X	X	X	X	X
Outputs high-Z, Write disabled	X	H	H	X	X	X	X
Outputs high-Z	X	X	X	H	H	X	X
Outputs high-Z	X	X	X	L	L	X	X
Read DQ1 - DQ8, DQP1 bank A	L	L	H	L	H	H	H
Read DQ1 - DQ8, DQP1 bank B	L	L	H	H	L	H	H
Read DQ9 - DQ16, DQP2 bank A	L	H	L	L	H	H	H
Read DQ9 - DQ16, DQP2 bank B	L	H	L	H	L	H	H
Read DQ1 - DQ16, DQP1, DQP2 bank A	L	L	L	L	H	H	H
Read DQ1 - DQ16, DQP1, DQP2 bank B	L	L	L	H	L	H	H
Write DQ1 - DQ8, DQP1 bank A	L	L	H	X	X	L	H
Write DQ1 - DQ8, DQP1 bank B	L	L	H	X	X	H	L
Write DQ9 - DQ16, DQP2 bank A	L	H	L	X	X	L	H
Write DQ9 - DQ16, DQP2 bank B	L	H	L	X	X	H	L
Write DQ1 - DQ16, DQP1, DQP2 bank A	L	L	L	X	X	L	H
Write DQ1 - DQ16, DQP1, DQP2 bank B	L	L	L	X	X	H	L
Write DQ1 - DQ8, DQP1 bank A & B	L	L	H	X	X	L	L
Write DQ9 - DQ16, DQP2 bank A & B	L	H	L	X	X	L	L
Write DQ1 - DQ16, DQP1, DQP2 bank A & B	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ or $\overline{CWEB}$ remain active, allows a chip enable controlled WRITE to be performed.

TRUTH TABLE

8K X 18 (MODE PIN = LOW)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs high-Z, Write disabled	H	X	X	X	X	X	X
Outputs high-Z, Write disabled	X	H	H	X	X	X	X
Outputs high-Z	X	X	X	H	H	X	X
Read DQ1 - DQ8, DQP1	L	L	H	L	L	H	H
Read DQ9 - DQ16, DQP2	L	H	L	L	L	H	H
Read DQ1 - DQ16, DQP1, DQP2	L	L	L	L	L	H	H
Write DQ1 - DQ8, DQP1	L	L	H	X	X	L	L
Write DQ9 - DQ16, DQP2	L	H	L	X	X	L	L
Write DQ1 - DQ16, DQP1, DQP2	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ and $\overline{CWEB}$ remain active, allows a chip enable controlled WRITE to be performed.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1.2 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, Vcc = 5.0V ± 5%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		Vcc	4.75	5.25	V	
Input High Voltage		VIH	2.2	Vcc+0.3	V	1
Input Low Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	VIN = GND to Vcc	ILI	-10	10	µA	
Output Leakage Current	VI/O = GND to Vcc $\overline{CS0}$, $\overline{CS1}$ = VIL or $\overline{COEA}$, $\overline{COEB}$ & $\overline{CWEA}$, $\overline{CWEB}$ = VIL	ILO	-10	10	µA	
Output Low Voltage	IOL = 4.0mA	VOL		0.4	V	1
Output High Voltage	IOH = -1.0mA	VOH	2.4		V	1

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty cycle VIN = GND to Vcc	ICC1		220	mA	
Power Supply Current: Average Operating Current	50% Duty cycle VIN = GND to Vcc	ICC2		120	mA	
Power Supply Current: CMOS Standby	$\overline{CS0}$ = $\overline{CS1}$ ≥ Vcc - 0.2V Vcc = MAX.	ISB		20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	CIN		8	pF	3
Output Capacitance	Vcc = 5V	CI/O		8	pF	3

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le +70°C$, V_{CC} = 5.0V ±5%)

DESCRIPTION	SYM	-25		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle									
READ cycle time	^tRC	25		35		45		ns	4, 5
Address access time (A0-A11)	^tAA		25		35		45	ns	
A12 address access time	^tA12A		17		25		30	ns	
Chip enable access time	^tACE		20		25		35	ns	
Chip select access time	^tACS		25		35		45	ns	
Output enable access time	^tAOE		10		13		16	ns	
Output hold from address change	^tOH	3		3		3		ns	
Chip select to output low-Z	^tLZCS	3		3		3		ns	
Output enable to output low-Z	^tLZOE	2		2		2		ns	
Chip deselect to output high-Z	^tHZCS		15		25		30	ns	6
Output disable to output high-Z	^tHZOE		10		14		14	ns	6
Address latch enable pulse width	^tCALEN	8		10		15		ns	
Address setup to latch low	^tASL	4		6		10		ns	
Address hold from latch low	^tAHL	5		5		5		ns	
WRITE Cycle									
WRITE cycle time	^tWC	25		35		45		ns	
Address valid to end of write	^tAW	18		25		40		ns	
A12 address valid to end of write	^tA12W	18		25		40		ns	
Chip select to end of write	^tCW	18		25		30		ns	
Data valid to end of write	^tDW	10		10		15		ns	
Data hold from end of write	^tDH	0		0		0		ns	
Write enable output in high-Z	^tHZWE		15		15		20	ns	6
Write disable to output in low-Z	^tLZWE	3		3		3		ns	
Write pulse width	^tWP	18		25		30		ns	
$\overline{CE}$ pulse width (during chip enable controlled write)	^tCP	18		25		30		ns	
Address setup time	^tAS	0		0		0		ns	
Write recovery time	^tWR	0		0		2		ns	
Address latch enable pulse width	^tCALEN	8		10		15		ns	
Address setup to latch low	^tASL	4		6		10		ns	
Address hold from latch low	^tAHL	5		5		5		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

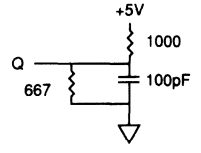


Fig. 1 OUTPUT LOAD EQUIVALENT

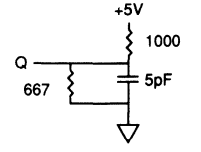
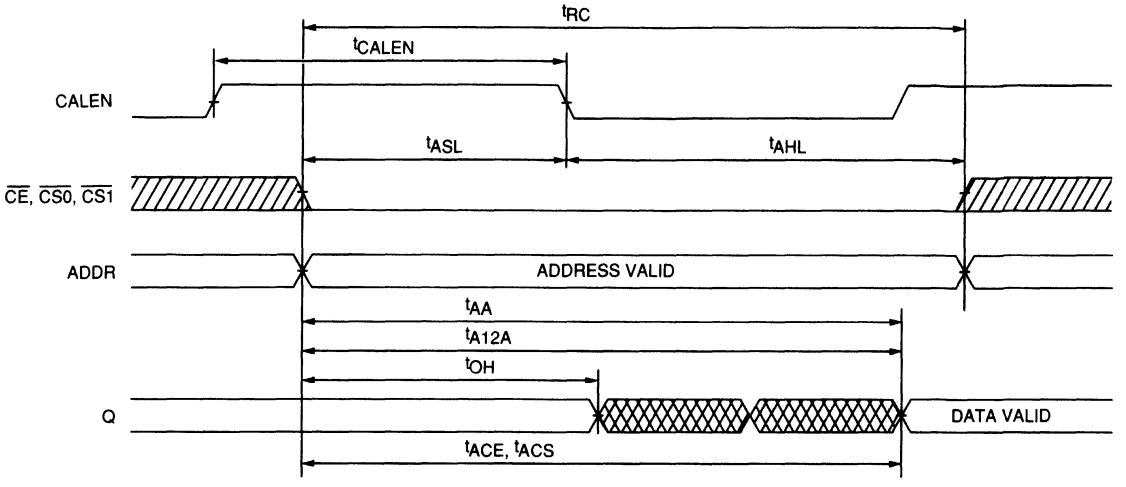


Fig. 2 OUTPUT LOAD EQUIVALENT

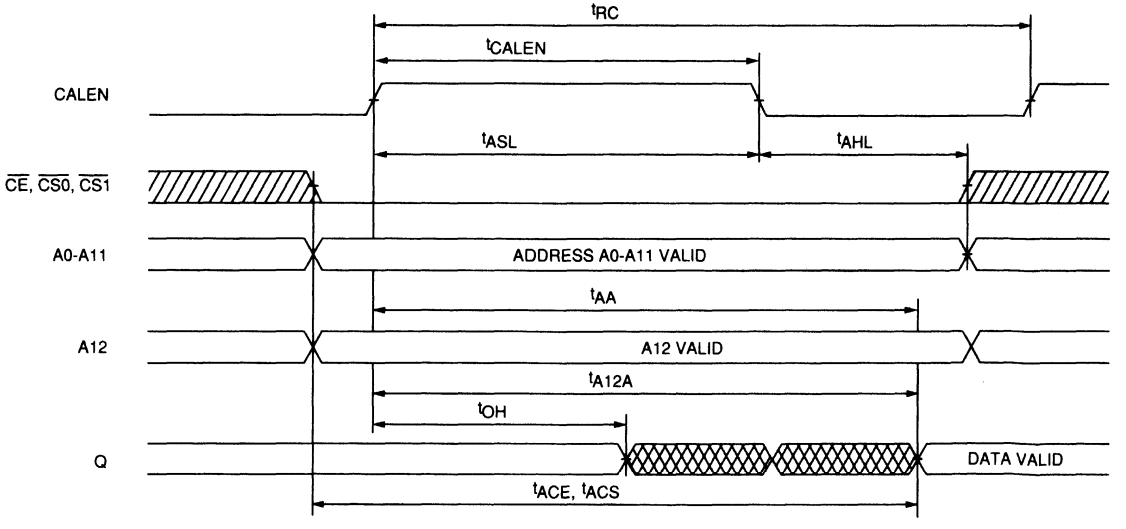
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. This parameter is sampled.
4. $\overline{CWE}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. ^tHZCS, ^tHZOE, and ^tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.

READ CYCLE NO. 1
(Address Controlled)



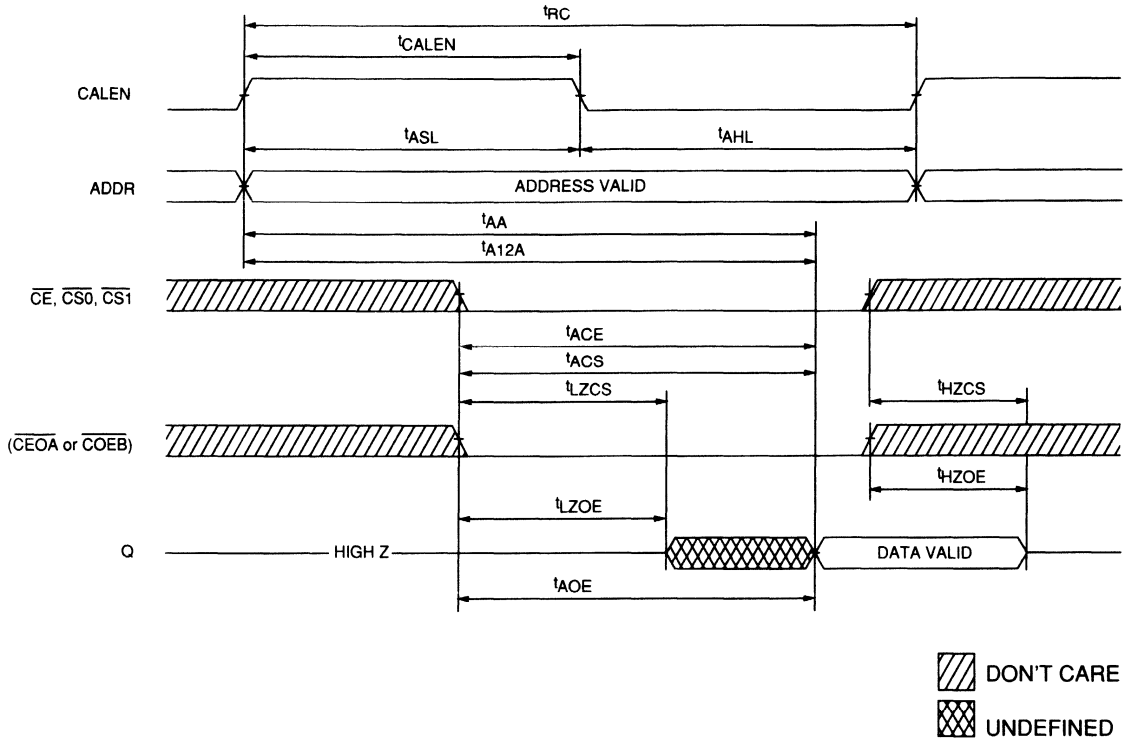
READ CYCLE NO. 2
(CALEN Controlled)



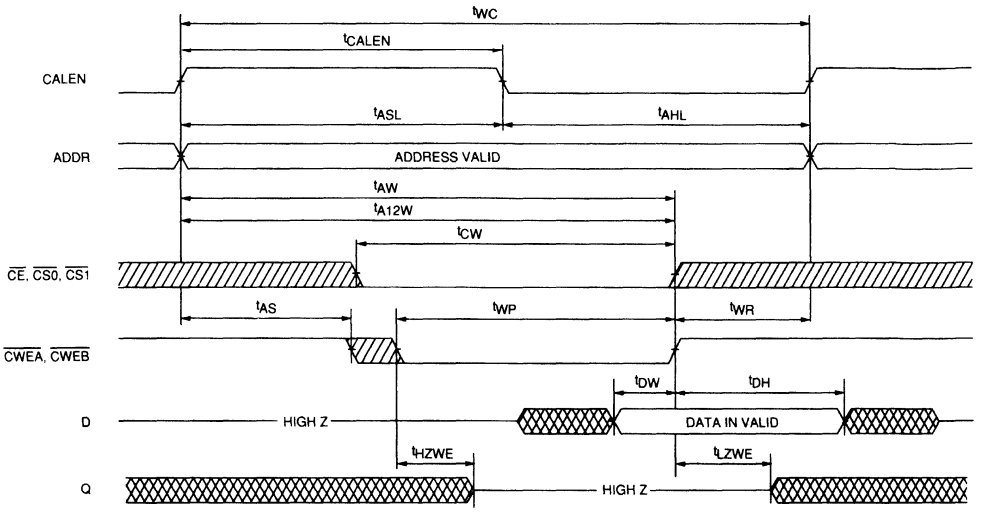
DON'T CARE

UNDEFINED

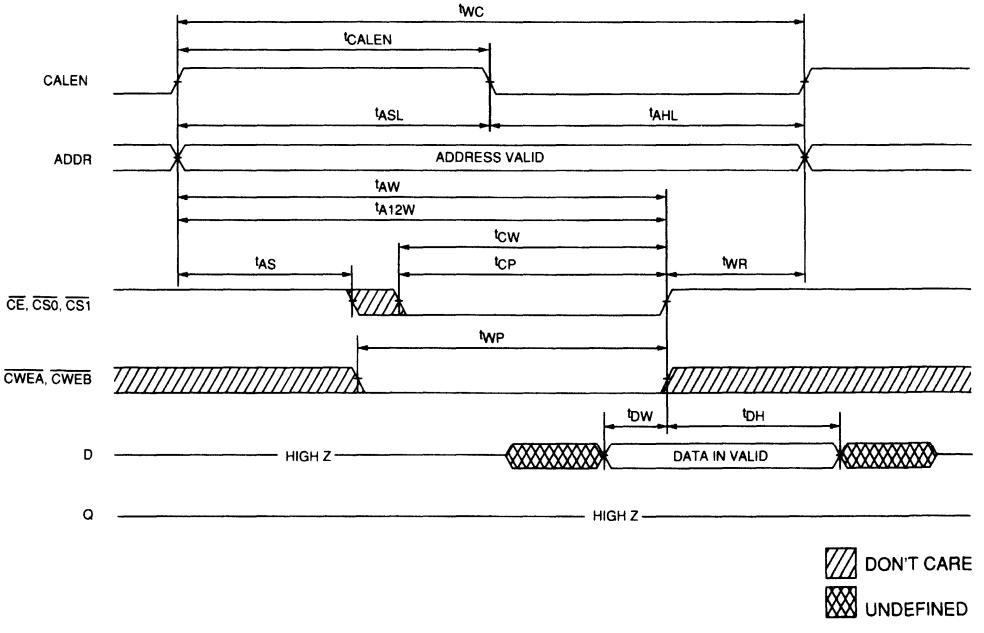
READ CYCLE NO. 3



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Select Controlled)



DYNAMIC RAMs 1

DYNAMIC RAM MODULES 2

MULTIPORT DYNAMIC RAMs 3

STATIC RAMs 4

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FIFO PRODUCT SELECTION GUIDE

Memory Configuration	Control Function	Part Number	Cycle Time (ns)	Package & Number of Pins				Page
				PDIP	CDIP	LCC	PLCC	
512 x 8	MB, VF	MT52C8006	25, 30, 35	28	28	-	-	7-3
512 x 9	E	MT52C9005	25, 30, 35	28	28	32	32	7-5
512 x 9	MB	MT52C9006	25, 30, 35	28	28	32	32	7-17
512 x 9	VF	MT52C9007	25, 30, 35	28	28	32	32	7-19
512 x 16	E, MB, VF	MT52C1605	25, 30, 35	48	48	-	-	7-21
512 x 16/8	E, MB, VF	MT52C1607	25, 30, 35	40	40	-	-	7-23
1K x 8	MB, VF	MT52C8011	25, 30, 35	28	28	-	-	7-25
1K x 9	E	MT52C9010	25, 30, 35	28	28	32	32	7-27
1K x 9	MB	MT52C9011	25, 30, 35	28	28	32	32	7-39
1K x 9	VF	MT52C9012	25, 30, 35	28	28	32	32	7-41
1K x 16	E, MB, VF	MT52C1610	25, 30, 35	48	48	-	-	7-43
1K x 16/8	E, MB, VF	MT52C1612	25, 30, 35	40	40	-	-	7-45
2K x 8	MB, VF	MT52C8021	25, 30, 35	28	28	-	-	7-47
2K x 9	E	MT52C9020	25, 30, 35	28	28	32	32	7-49
2K x 9	MB	MT52C9021	25, 30, 35	28	28	32	32	7-61
2K x 9	VF	MT52C9022	25, 30, 35	28	28	32	32	7-63
2K x 16	E, MB, VF	MT52C1620	25, 30, 35	48	48	-	-	7-65
2K x 16/8	E, MB, VF	MT52C1622	25, 30, 35	40	40	-	-	7-67
4K x 8	E, MB, VF	MT52C8041	25, 30, 35	28	28	-	-	7-69
4K x 9	E	MT52C9040	25, 30, 35	28	28	32	32	7-71
4K x 9	MB	MT52C9041	25, 30, 35	28	28	32	32	7-83
4K x 9	VF	MT52C9042	25, 30, 35	28	28	32	32	7-85

MB ..... Mailbox Register
VF ..... Variable Flags
E ..... Depth and Width Expandable

FIFO

512 x 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

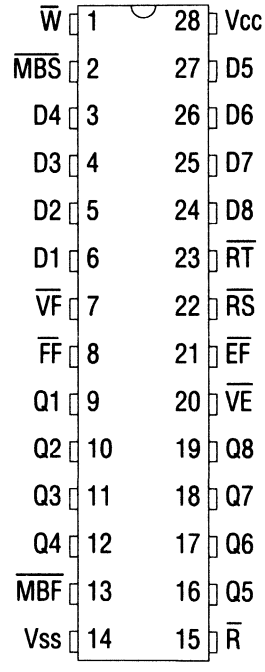
- High speed: 25ns access, 35ns cycle time
- Asynchronous and simultaneous READ and WRITE
- Empty and Full Flags
- Automatic retransmit
- Transistor loads for maximum data integrity
- Low power
- Programmable Mailbox register
- Programmable Empty/Full Flags (128 increments)

OPTIONS

	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

28L DIP



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 6-transistor memory cell with resistive loads. They are fabricated using silicon gate CMOS technology.

There are three major user options that are available separately or in combination: expandable, mailbox register, and variable flags. Expandable FIFOs are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFOs have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFOs allow the user to program the level of two additional full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO 512 x 9 FIFO

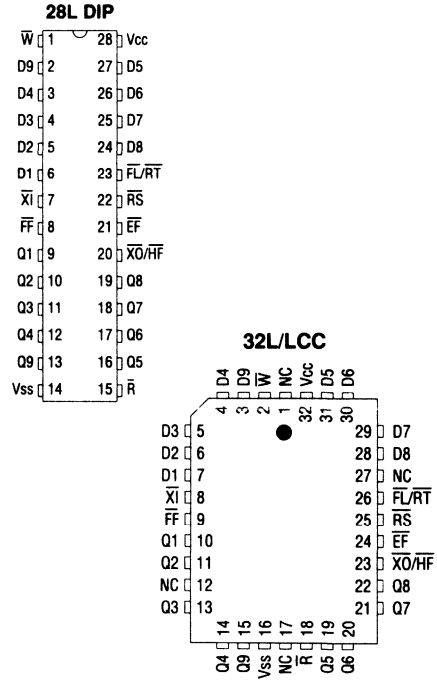
FEATURES

- Very high speed: 25, 30, and 35ns access
- High performance, low power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby); 350mW typ. (active)
- TTL compatible inputs and outputs
- Asynchronous and simultaneous READ and WRITE
- Empty, Half-Full and Full Flags
- Auto-retransmit capability
- Fully expandable width and depth
- Pin function compatible with higher density FIFOs

OPTIONS MARKING

• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP (600 mil)	None
Ceramic DIP (600 mil)	C
PLCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)



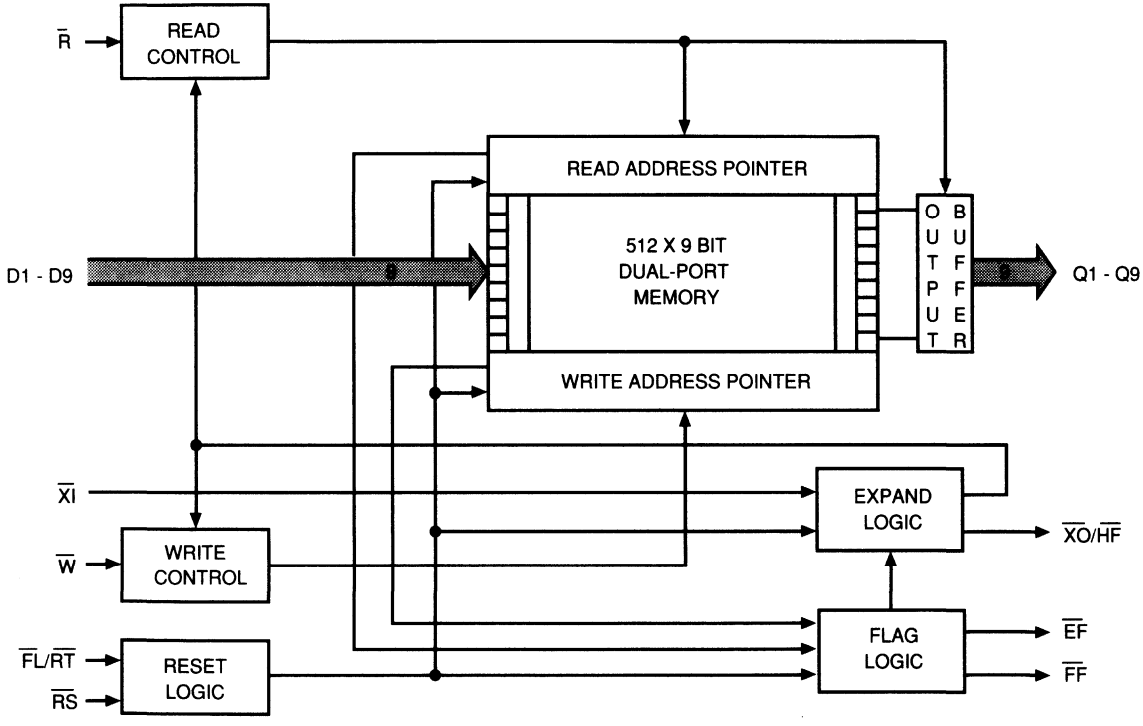
GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port, 6-transistor memory cell with resistive loads.

These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information can be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates. Visibility of the memory volume is given through empty, half-full, and full flags. While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain high impedance. Expansion out, expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the stand alone mode.

The depth of the FIFO can be expanded by cascading multiple devices in the depth expansion mode. Also, the MT52C9005 is speed, function and pin compatible with higher density FIFOs from Micron. This upward compatibility with 1K, 2K and 4K x 9 FIFOs provides a single chip depth expansion solution.

FIFO



FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: Taking $\overline{RS}$ LOW will reset the FIFO by initializing the read and write pointers and all flags. After the device is powered up, it must be reset before any writes can take place. Reset also samples $\overline{XI}$ and $\overline{FL/RT}$ to set the depth expansion mode.
2	1	$\overline{W}$	Input	Write Strobe: $\overline{W}$ is taken LOW to write data from the input port (D1 - D9) into the FIFO memory array.
18	15	$\overline{R}$	Input	Read Strobe: $\overline{R}$ is taken LOW to read data from the FIFO memory array to the output port (Q1 - Q9).
8	7	$\overline{XI}$	Input	Expansion In: Sets mode of operation on the L→H transition of $\overline{RS}$; stand alone when LOW; depth expansion when HIGH. When in depth expansion, $\overline{XI}$ will be pulsed LOW once to enable write pointer, then again to enable read pointer.
26	23	$\overline{FL/RT}$	Input	First Load: In depth expansion mode, $\overline{FL}$ will enable the device as the first to be loaded, (enables read and write pointers) when LOW during the L→H transition of $\overline{RS}$. Retransmit: In stand alone mode, $\overline{RT}$ is used to enable the RETRANSMIT cycle. When taken LOW, $\overline{RT}$ resets the read pointer to the first data location and the FIFO is then ready to retransmit data on the following READ operation(s). The flags will be affected according to specific data conditions.
3, 4, 5, 6, 7 28, 29, 30,31	2, 3, 4, 5, 6 24, 25, 26,27	D1 - D9	Input	Data Inputs
24	21	$\overline{EF}$	Output	Empty Flag: Indicates empty FIFO memory when LOW, inhibiting further READ cycles.
9	8	$\overline{FF}$	Output	Full Flag: Indicates full FIFO memory when LOW, inhibiting further WRITE cycles.
23	20	$\overline{XO/HF}$	Output	Expansion Out: During depth expansion, $\overline{XO}$ will pulse LOW on the last physical WRITE and READ operations, disabling writes then reads to the FIFO. Half-full Flag: During stand alone operation $\overline{HF}$ indicates when the (Half-full + 1) memory location is written; will stay LOW until the (Half-full + 1) location is read.
10,11,13,14 15, 19, 20,21,22	9,10,11,12,13 16, 17, 18,19	Q1 - Q9	Output	Data Output: Output or high impedance.
32	28	Vcc	Supply	Power Supply: +5V 10%
16	14	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9005 uses a dual-port SRAM memory cell with separate read and write pointers that results in a flexible length FIFO buffer memory, with independent, asynchronous READ and WRITE capabilities and with no fallthrough or bubblethrough time constraints.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing half-full flags the $\overline{XO}/\overline{HF}$ pin will be shown as $(\overline{XO})/\overline{HF}$.*

RESET

After Vcc is stable, RESET ($\overline{RS}$) must be taken LOW to initialize the read and write pointers and flags. RESET also sets the mode of operation, stand alone or expanded. During the RESET pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the stand alone or depth expansion mode. The stand alone mode is entered when $\overline{XI}$ is LOW during the RESET cycle. When $\overline{XI}$ is HIGH or is connected to $\overline{XO}/(\overline{HF})$ of another FIFO, the depth expansion mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW, while $\overline{FF}$ is HIGH. The WRITE cycle is initiated by the falling edge of $\overline{W}$ and data on the D1-D9 pins is latched on the rising edge. If the location to be written is the last empty location in the FIFO, the $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is LOW, any attempted writes will be inhibited, with no loss of data already stored in the FIFO. When a device is used in the stand alone mode, $(\overline{XO})/\overline{HF}$ is asserted when the half-full-plus-one location (512/2+1) is written. It will stay asserted until the half-full-plus-one location is read or the FIFO is reset. The first write to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the depth expansion mode, the last write to a FIFO will cause $\overline{FF}$ to go LOW and will cause $\overline{XI}$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and data is available ($\overline{EF}$ is HIGH). The data-out (Q1 - Q9) pins will go active (low Z) ^{t}RLZ after the falling edge of $\overline{R}$ and valid data will appear ^{t}A after the falling edge of $\overline{R}$. When the last data word is read, $\overline{EF}$ will go LOW after the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (high Z). When the FIFO is being used in the single device mode and the half-full-plus-one location is read, $(\overline{XO})/\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$. When the FIFO is full ($\overline{FF}$ asserted) and a read is initiated, $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the expanded mode, the last read to a FIFO will cause the $\overline{EF}$ to go LOW and will cause $\overline{XI}$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the stand alone mode, the MT52C9005 allows the receiving device to request that data just read from the FIFO to be repeated. When the $(\overline{FL})/\overline{RT}$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may again start reading the data from the beginning of the FIFO ^{t}RTR after $(\overline{FL})/\overline{RT}$ is taken HIGH. The empty, half-full and full flags will be affected as specified for the data volume.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty points, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a flow-through write. Flow-through writes are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a flow-through read can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. Flow-through reads are initiated from the rising edge of $\overline{W}$ and access time measured from the rising edge of $\overline{EF}$.

FIFO

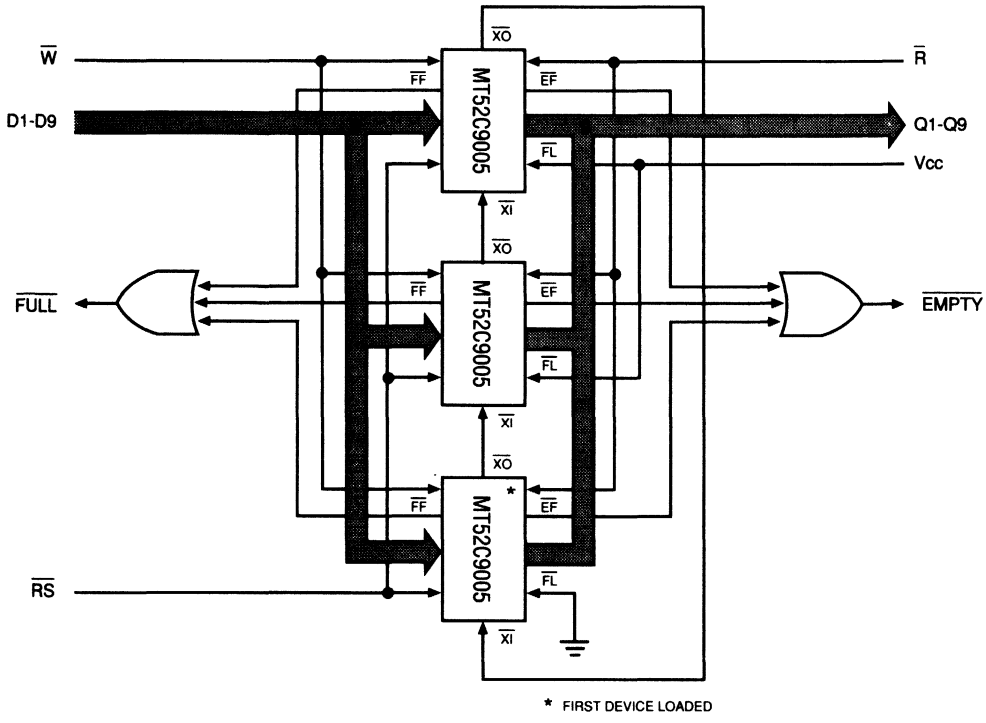


Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the stand alone or groups of expanded depth mode FIFOs. Expanded width operation is acheived by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1), when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9005s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}$/($\overline{HF}$) and $\overline{FL}$/($\overline{RT}$). Figure 1 illustrates a typical three device expansion. The depth expansion mode is entered during a RESET cycle, by tying the $\overline{XO}$/($\overline{HF}$) pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}$/($\overline{RT}$) pin grounded. The remaining devices in the chain will have $\overline{FL}$/($\overline{RT}$) tied HIGH. During RESET cycle, $\overline{XO}$/($\overline{HF}$) of each device goes HIGH, disabling the read and write pointers of every FIFO, except the first load device. When the last physical location of the first device is written, the $\overline{XO}$/($\overline{HF}$) pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling the first. The writes will continue to go to the second device until it is full. Then it will "pass" the write pointer to the third device. This process continues until all devices are full. When the entire FIFO array is written, the full condition is signaled by ORing all the $\overline{FF}$ pins, further writes are inhibited. On the last physical read of the first device, its $\overline{XO}$/($\overline{HF}$) will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. On the last read, an empty condition is signaled by "ORing" all of the $\overline{EF}$ pins. This inhibits further reads. While in the depth expansion mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE

MODE	INPUTS						OUTPUTS				NOTES
	$\overline{W}$	$\overline{R}$	$\overline{RS}$	$\overline{FL/RT}$	$\overline{XI}$	D1-D9	$\overline{EF}$	$\overline{FF}$	$\overline{XO/HF}$	Q1-Q9	
RESET	H	H	L	X	X	X	L	H	X	X	
WRITE	L	X	H	X	X	Data In	X	H	X	X	1
READ	X	L	H	X	X	X	H	X	X	Data Out	2
EMPTY (LAST READ)	X	H→L	H	X	X	X	H→L	X	X	Data Out	
FULL (LAST WRITE)	H→L	X	H	X	X	Data In	X	H→L	L	X	
HALF-FULL	H→L	X	H	X	X	Data In	X	H	H→L	X	3, 4
RETRANSMIT	H	H	H	L	X	X	H	X	X	X	4

FIFO

NOTES:

1. WRITE operations are independent of READ operations.
2. READ operations are independent of WRITE operations.
3. The half-full location is (512/2 + 1) or 257.
4. Functional in stand alone mode only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -0.5V to +7.0V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All inputs	V_{IL}	-0.5	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}$, $\overline{R} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}		100	mA	3
Power Supply Current: Standby	$\overline{W}$, $\overline{R} \ge V_{IH}$, V_{CC} = Max.	I_{SB1}		10	mA	
	$\overline{W}$, $\overline{R} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}		1	mA	
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		8	pF	4
Output Capacitance	V_{CC} = 5V	C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-25		-30		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access Time	t_A		25		30		35	ns	
READ Cycle Time	t_{RC}	35		40		45		ns	
READ Recovery Time	t_{RR}	10		10		10		ns	
Read Pulse Width	t_{RPW}	25		30		35		ns	
Read LOW to low Z	t_{RLZ}	5		5		5		ns	
Read to HIGH to high Z	t_{RHZ}		18		20		20	ns	
Read HIGH to Data Valid	t_{DV}		18		20		20	ns	
WRITE Cycle Time	t_{WC}	35		40		45		ns	
Write Pulse Width	t_{WPW}	25		30		35		ns	
WRITE Recovery Time	t_{WR}	10		10		10		ns	
Write HIGH to LOW Z	t_{WLZ}	5		5		5		ns	5
Data Set-up Time	t_{DS}	15		18		20		ns	
Data Hold Time	t_{DH}	0		0		0		ns	
RESET Cycle Time	t_{RCS}	35		40		45		ns	
Reset Pulse Width	t_{RSP}	25		30		35		ns	6
RESET Recovery Time	t_{RSR}	10		10		10		ns	
Read HIGH to Reset HIGH	t_{RRS}	25		30		35		ns	
Write HIGH to Reset HIGH	t_{WRS}	25		30		35		ns	
RETRANSMIT Cycle Time	t_{RTC}	35		40		45		ns	
Retransmit Pulse Width	t_{RT}	25		30		35		ns	
RETRANSMIT Recovery Time	t_{RTR}	10		10		12		ns	
Retransmit Set-up Time	t_{RTS}	25		30		35		ns	
Reset to $\overline{EF}$ LOW	t_{EFL}		35		40		45	ns	
Reset to $\overline{FF}$ HIGH	t_{FFH}		35		40		45	ns	
Reset to $\overline{HF}$ HIGH	t_{HFH}		35		40		45	ns	
Read LOW to $\overline{EF}$ LOW	t_{REF}		25		30		35	ns	
Read HIGH to $\overline{FF}$ HIGH	t_{RFF}		25		30		35	ns	
Write LOW to $\overline{FF}$ LOW	t_{WFF}		25		30		35	ns	
Write HIGH to $\overline{EF}$ HIGH	t_{WEF}		25		30		35	ns	
Write LOW to $\overline{HF}$ LOW	t_{WHF}		35		40		45	ns	
Read HIGH to $\overline{HF}$ HIGH	t_{RHF}		35		40		45	ns	
Read Pulse after $\overline{EF}$ HIGH	t_{RPE}	25		30		35		ns	5
Write Pulse Width after $\overline{FF}$ HIGH	t_{WPF}	25		30		35		ns	
Read/Write to $\overline{XO}$ LOW	t_{XOL}		25		30		35	ns	
Read/Write to $\overline{XO}$ HIGH	t_{XOH}		25		30		35	ns	
$\overline{XI}$ Pulse Width	t_{XIP}	25		30		35		ns	
$\overline{XI}$ Set-up Time	t_{XIS}	15		15		15		ns	
$\overline{XI}$ Recovery Time	t_{XIR}	10		10		10		ns	

FIFO

NOTES

1. All voltages referenced to V_{SS} (GND).
2. -3.0V for pulse width < 20ns.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through data mode only.
6. Pulse widths less than minimum are not allowed.

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 1

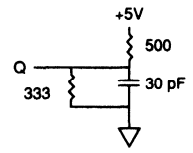
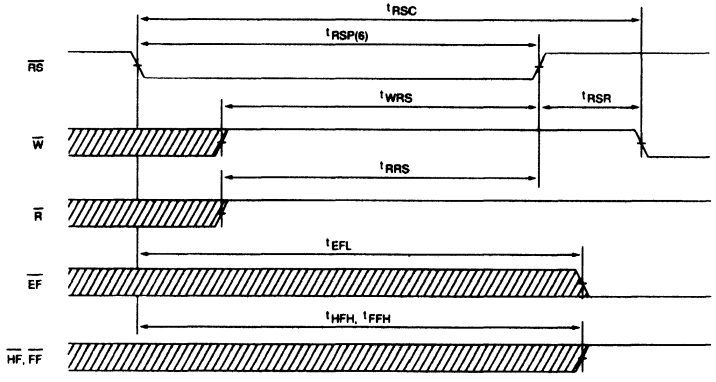
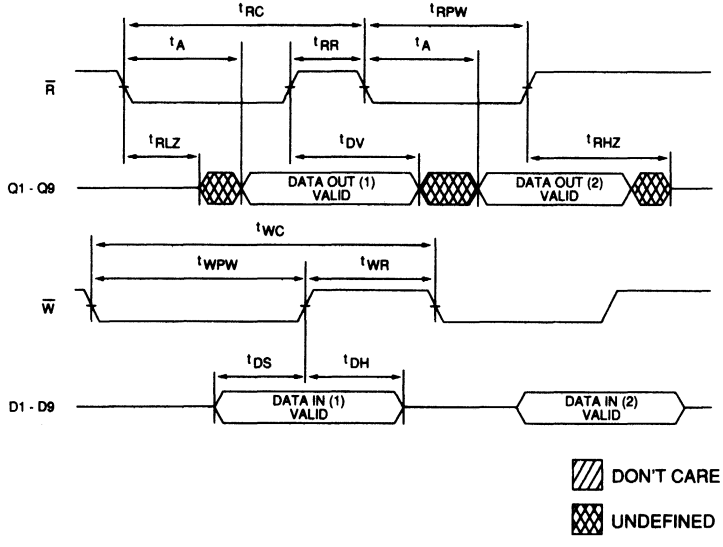


Fig. 1 OUTPUT LOAD EQUIVALENT

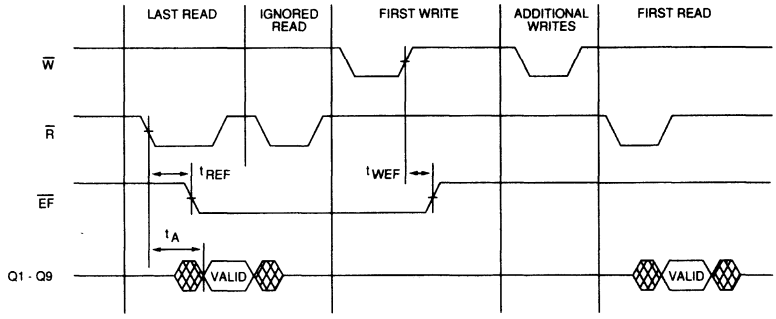
RESET



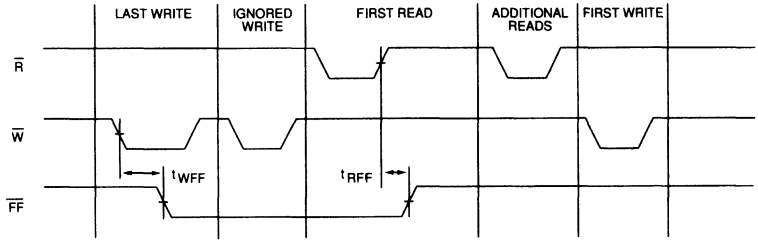
ASYNCHRONOUS READ AND WRITE



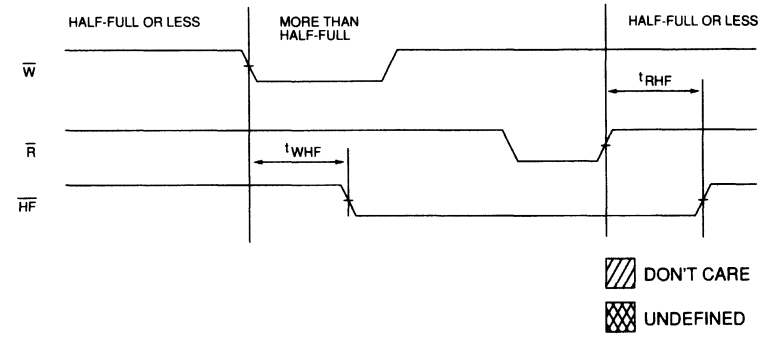
EMPTY FLAG



FULL FLAG

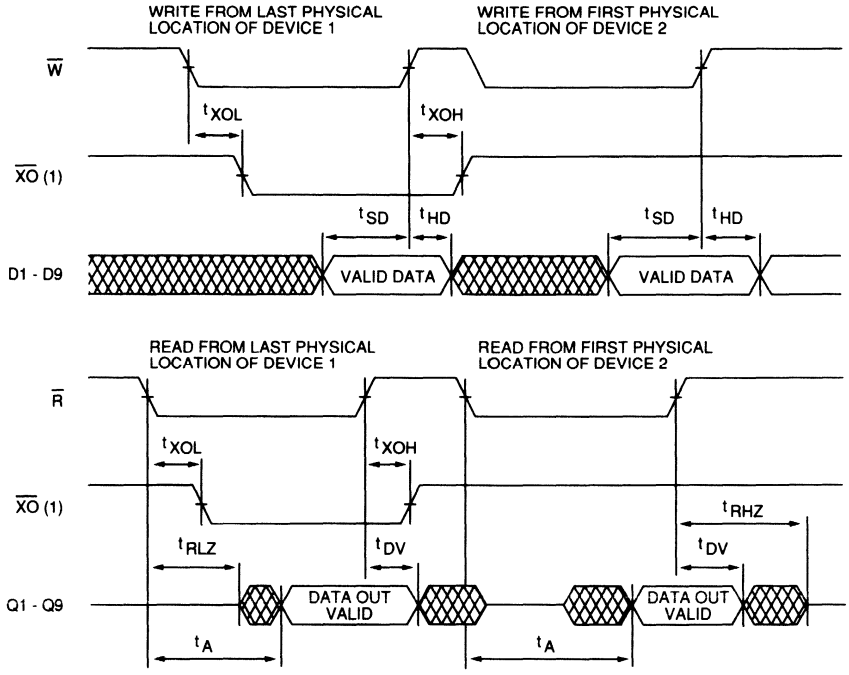


HALF-FULL FLAG



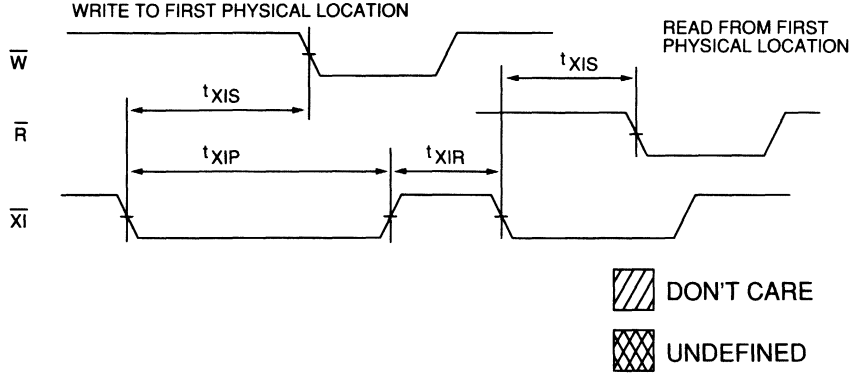
FIFO

EXPANSION MODE ($\overline{XO}$)



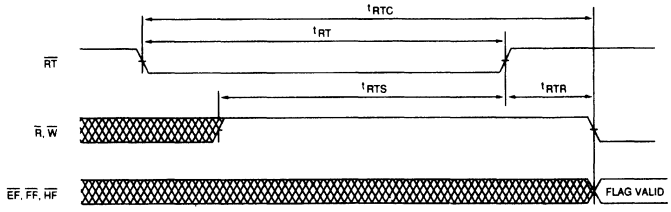
Note 1: $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

EXPANSION MODE ($\overline{XI}$)

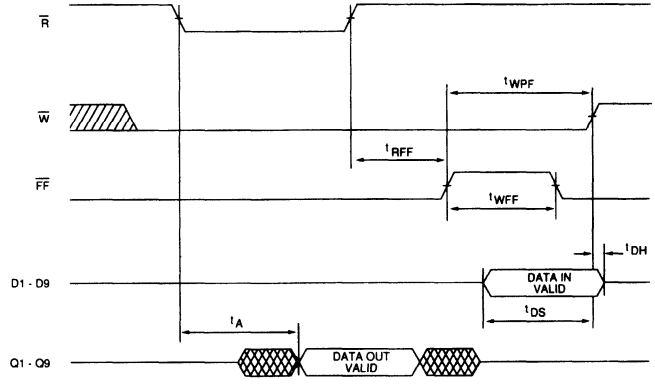


FIFO

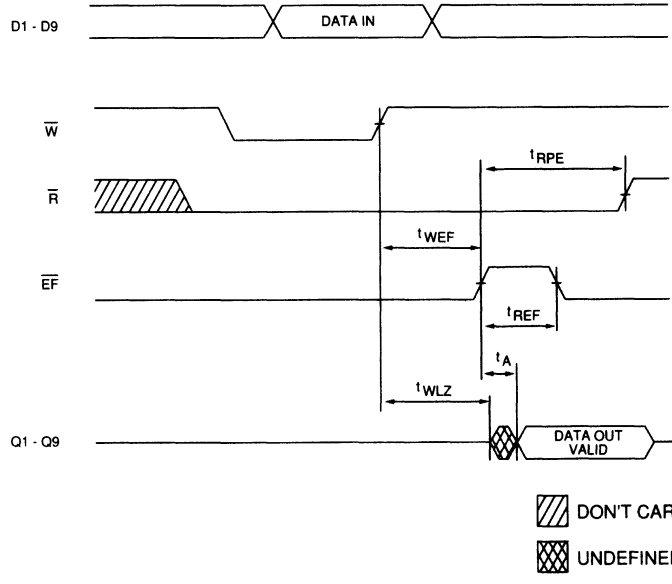
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH



FIFO

FIFO

512 x 9 FIFO

MAILBOX REGISTER

FEATURES

- High speed: 25ns access, 35ns cycle time
- Asynchronous and simultaneous READ and WRITE
- Empty and Full Flags
- Automatic retransmit
- Transistor loads for maximum data integrity
- Low power
- Programmable Mailbox register

OPTIONS — MARKING

- Timing

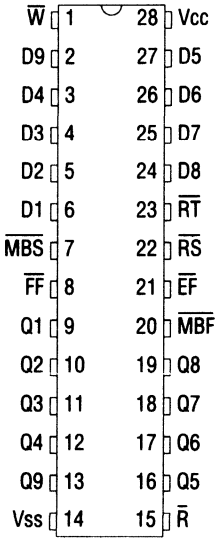
25ns access time	-25
30ns access time	-30
35ns access time	-35

- Packages

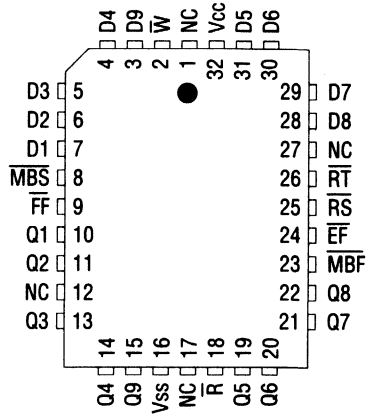
Plastic DIP	None
Ceramic DIP	C
PLCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 6-transistor memory cell with resistive loads. They are fabricated using silicon gate CMOS technology.

There are three major user options that are available separately or in combination: expandable, mailbox register, and variable flags. Expandable FIFOs are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFOs have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFOs allow the user to program the level of two additional full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

512 x 9 FIFO

VARIABLE FLAGS

FEATURES

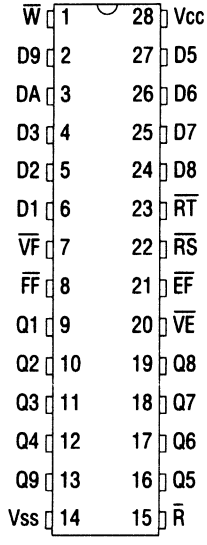
- High speed: 25ns access, 35ns cycle time
- Asynchronous and simultaneous READ and WRITE
- Empty and Full Flags
- Automatic retransmit
- Transistor loads for maximum data integrity
- Low power
- Programmable Empty/Full Flags (128 increments)

OPTIONS — MARKING

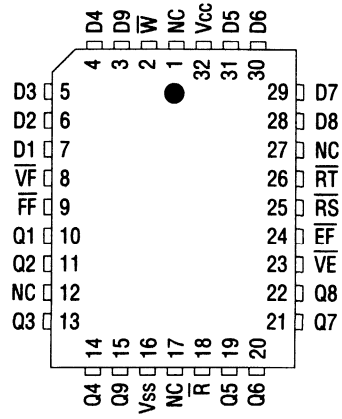
- Timing
  - 25ns access time — -25
  - 30ns access time — -30
  - 35ns access time — -35
- Packages
  - Plastic DIP — None
  - Ceramic DIP — C
  - PLCC — EJ
  - Ceramic LCC — EC

PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 6-transistor memory cell with resistive loads. They are fabricated using silicon gate CMOS technology.

There are three major user options that are available separately or in combination: expandable, mailbox register, and variable flags. Expandable FIFOs are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFOs have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFOs allow the user to program the level of two additional full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

512 x 16 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

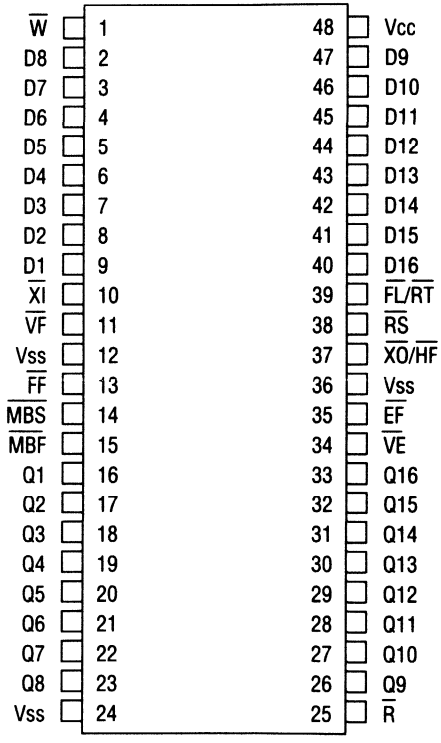
- High speed: 25ns access, 35ns cycle time
- 16-bit word width
- Asynchronous and simultaneous READ and WRITE
- Empty and Full Flags
- Easy expansion capability
- Automatic retransmit
- Transistor loads for maximum data integrity
- Low power
- Programmable Mailbox register
- Programmable Empty/Full Flags (128 increments)

OPTIONS

	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

48L DIP



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 6-transistor memory cell with resistive loads. They are fabricated using silicon gate CMOS technology.

There are three major user options that are available separately or in combination: expandable, mailbox register, and variable flags. Expandable FIFOs are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFOs have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFOs allow the user to program the level of two additional full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

512 x 16 to 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

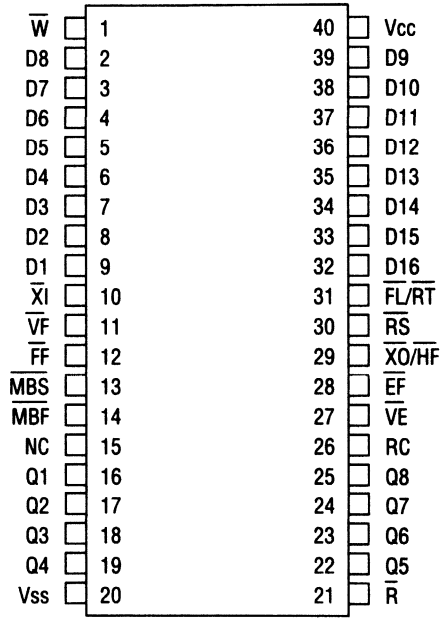
- High speed: 25ns access, 35ns cycle time
- Asynchronous and simultaneous READ and WRITE
- Empty and Full Flags
- Easy expansion capability
- Automatic retransmit
- Transistor loads for maximum data integrity
- Low power
- One chip interface between a 16 bit bus and an 8 bit bus
- Programmable Mailbox register
- Programmable Empty/Full Flags (128 increments)

OPTIONS

	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

40L DIP



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 6-transistor memory cell with resistive loads. They are fabricated using silicon gate CMOS technology.

There are three major user options that are available separately or in combination: expandable, mailbox register, and variable flags. Expandable FIFOs are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFOs have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFOs allow the user to program the level of two additional full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

1K x 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

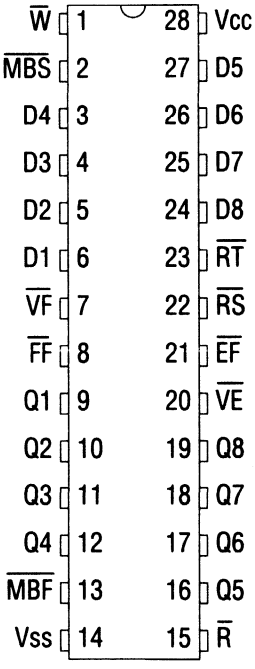
- High speed: 25ns access, 35ns cycle time
- Asynchronous and simultaneous READ and WRITE
- Empty and Full Flags
- Automatic retransmit
- Transistor loads for maximum data integrity
- Low power
- Programmable Mailbox register
- Programmable Empty/Full Flags (128 increments)

OPTIONS

OPTIONS	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

28L DIP



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 6-transistor memory cell with resistive loads. They are fabricated using silicon gate CMOS technology.

There are three major user options that are available separately or in combination: expandable, mailbox register, and variable flags. Expandable FIFOs are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFOs have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFOs allow the user to program the level of two additional full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO 1K x 9 FIFO

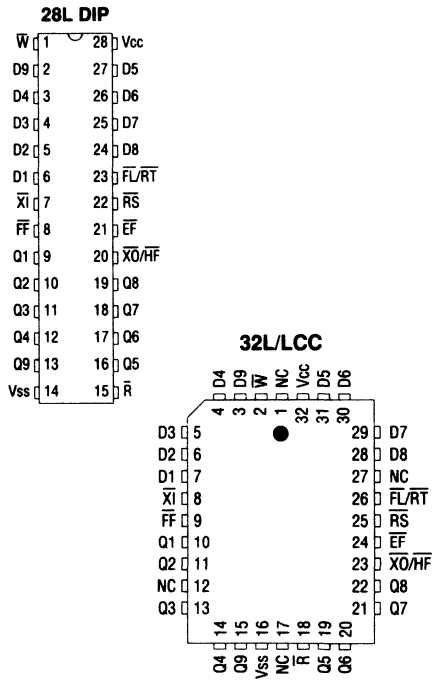
FEATURES

- Very high speed: 25, 30, and 35ns access
- High performance, low power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby); 350mW typ. (act.)
- TTL compatible inputs and outputs
- Asynchronous and simultaneous READ and WRITE
- Empty, Half-Full and Full Flags
- Auto-retransmit capability
- Fully expandable width and depth
- Pin function compatible with higher density 9000 series FIFOs

OPTIONS MARKING

• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP (600 mil)	None
Ceramic DIP (600 mil)	C
PLCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

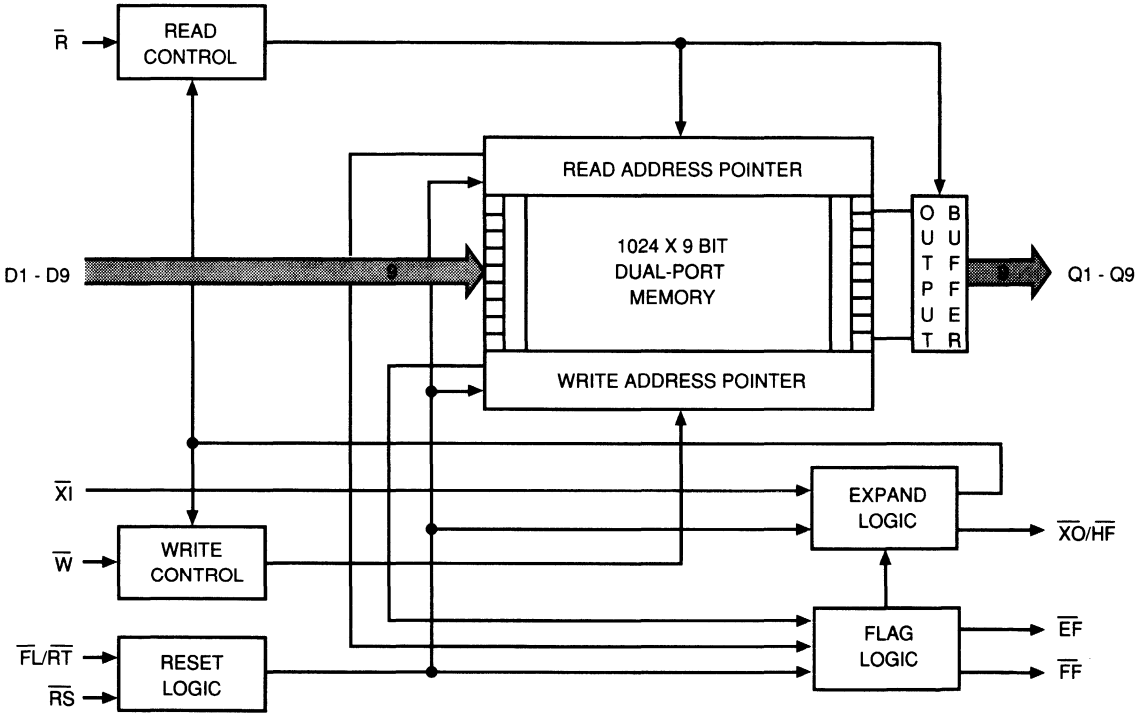


GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port, 6-transistor memory cell with resistive loads.

These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information can be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates. Visibility of the memory volume is given through empty, half-full, and full flags. While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain high impedance. Expansion out, expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the stand alone mode.

The depth of the FIFO can be expanded by cascading multiple devices in the depth expansion mode. Also, the MT52C9010 is speed, function and pin compatible with higher density FIFOs from Micron. This upward compatibility with 2K and 4K x 9 FIFOs provides a single chip depth expansion solution.



FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: Taking $\overline{RS}$ LOW will reset the FIFO by initializing the read and write pointers and all flags. After the device is powered up, it must be reset before any writes can take place. Reset also samples $\overline{XI}$ and $\overline{FL}/\overline{RT}$ to set the depth expansion mode.
2	1	$\overline{W}$	Input	Write Strobe: $\overline{W}$ is taken LOW to write data from the input port (D1 - D9) into the FIFO memory array.
18	15	$\overline{R}$	Input	Read Strobe: $\overline{R}$ is taken LOW to read data from the FIFO memory array to the output port (Q1 - Q9).
8	7	$\overline{XI}$	Input	Expansion In: Sets mode of operation on the L→H transition of $\overline{RS}$; stand alone when LOW; depth expansion when HIGH. When in depth expansion, $\overline{XI}$ will be pulsed LOW once to enable write pointer, then again to enable read pointer.
26	23	$\overline{FL}/\overline{RT}$	Input	First Load: In depth expansion mode, $\overline{FL}$ will enable the device as the first to be loaded, (enables read and write pointers) when LOW during the L→H transition of $\overline{RS}$. Retransmit: In stand alone mode, $\overline{RT}$ is used to enable the RETRANSMIT cycle. When taken LOW, $\overline{RT}$ resets the read pointer to the first data location and the FIFO is then ready to retransmit data on the following READ operation(s). The flags will be affected according to specific data conditions.
3, 4, 5, 6, 7 28, 29, 30,31	2, 3, 4, 5, 6 24, 25, 26,27	D1 - D9	Input	Data Inputs
24	21	$\overline{EF}$	Output	Empty Flag: Indicates empty FIFO memory when LOW, inhibiting further READ cycles.
9	8	$\overline{FF}$	Output	Full Flag: Indicates full FIFO memory when LOW, inhibiting further WRITE cycles.
23	20	$\overline{XO}/\overline{HF}$	Output	Expansion Out: During depth expansion, $\overline{XO}$ will pulse LOW on the last physical WRITE and READ operations, disabling writes then reads to the FIFO. Half-full Flag: During stand alone operation $\overline{HF}$ indicates when the (Half-full + 1) memory location is written; will stay LOW until the (Half-full + 1) location is read.
10,11,13,14 15, 19, 20,21,22	9,10,11,12,13 16, 17, 18,19	Q1 - Q9	Output	Data Output: Output or high impedance.
32	28	Vcc	Supply	Power Supply: +5V 10%
16	14	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9010 uses a dual-port SRAM memory cell with separate read and write pointers that results in a flexible length FIFO buffer memory, with independent, asynchronous READ and WRITE capabilities and with no fallthrough or bubblethrough time contraints.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing half-full flags the $\overline{XO}/\overline{HF}$ pin will be shown as $(\overline{XO})/\overline{HF}$.*

RESET

After Vcc is stable, RESET ($\overline{RS}$) must be taken LOW to initialize the read and write pointers and flags. RESET also sets the mode of operation, stand alone or expanded. During the RESET pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the stand alone or depth expansion mode. The stand alone mode is entered when $\overline{XI}$ is LOW during the RESET cycle. When $\overline{XI}$ is HIGH or is connected to $\overline{XO}/(\overline{HF})$ of another FIFO, the depth expansion mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW, while $\overline{FF}$ is HIGH. The WRITE cycle is initiated by the falling edge of $\overline{W}$ and data on the D1-D9 pins is latched on the rising edge. If the location to be written is the last empty location in the FIFO, the $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is LOW, any attempted writes will be inhibited, with no loss of data already stored in the FIFO. When a device is used in the stand alone mode, $(\overline{XO})/\overline{HF}$ is asserted when the half-full-plus-one location (1024/2 + 1) is written. It will stay asserted until the half-full-plus-one location is read or the FIFO is reset. The first write to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the depth expansion mode, the last write to a FIFO will cause $\overline{FF}$ to go LOW and will cause $\overline{XI}$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and data is available ($\overline{EF}$ is HIGH). The data-out (Q1 - Q9) pins will go active (low Z) ^tRLZ after the falling edge of $\overline{R}$ and valid data will appear ^tA after the falling edge of $\overline{R}$. When the last data word is read, $\overline{EF}$ will go LOW after the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (high Z). When the FIFO is being used in the single device mode and the half-full-plus-one location is read, $(\overline{XO})/\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$. When the FIFO is full ($\overline{FF}$ asserted) and a read is initiated, $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the expanded mode, the last read to a FIFO will cause the $\overline{EF}$ to go LOW and will cause $\overline{XI}$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the stand alone mode, the MT52C9010 allows the receiving device to request that data just read from the FIFO to be repeated. When the $(\overline{FL})/\overline{RT}$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may again start reading the data from the beginning of the FIFO ^tRTR after $(\overline{FL})/\overline{RT}$ is taken HIGH. The empty, half-full and full flags will be affected as specified for the data volume.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty points, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a flow-through write. Flow-through writes are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a flow-through read can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. Flow-through reads are initiated from the rising edge of $\overline{W}$ and access time measured from the rising edge of $\overline{EF}$.

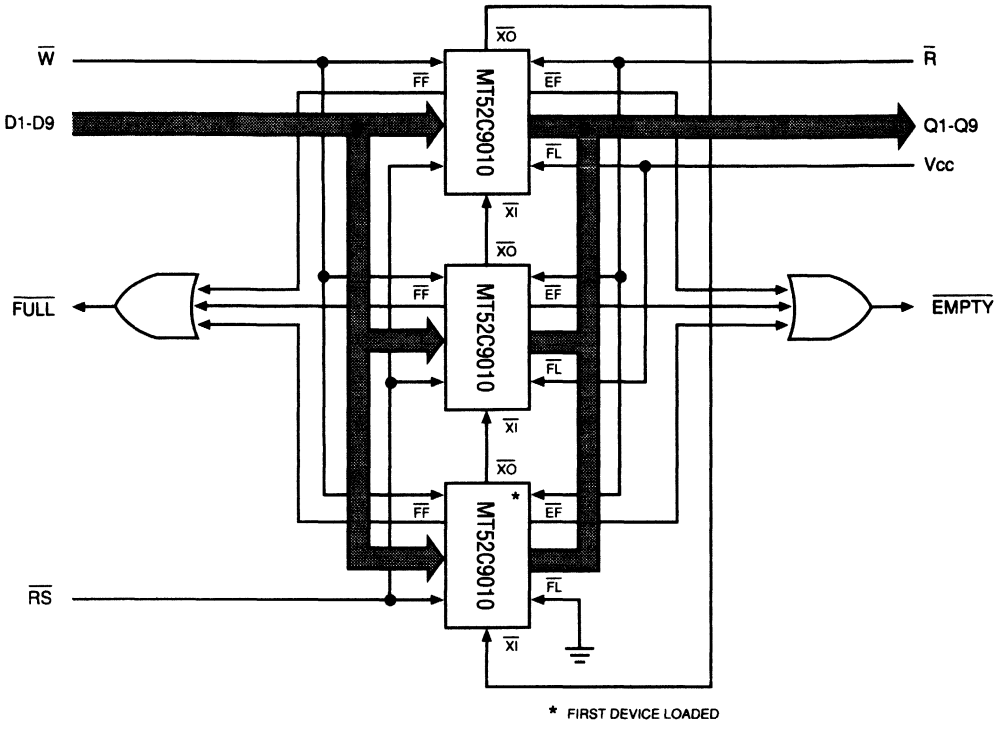


Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the stand alone or groups of expanded depth mode FIFOs. Expanded width operation is acheived by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1), when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9010s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}$/($\overline{HF}$) and $\overline{FL}$/($\overline{RT}$). Figure 1 illustrates a typical three device expansion. The depth expansion mode is entered during a RESET cycle, by tying the $\overline{XO}$/($\overline{HF}$) pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}$/($\overline{RT}$) pin grounded. The remaining devices in the chain will have $\overline{FL}$/($\overline{RT}$) tied HIGH. During RESET cycle, $\overline{XO}$/($\overline{HF}$) of each device goes HIGH, disabling the read and write pointers of every FIFO, except the first load device. When the last physical location of the first device is written, the $\overline{XO}$/($\overline{HF}$) pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling the first. The writes will continue to go to the second device until it is full. Then it will "pass" the write pointer to the third device. This process continues until all devices are full. When the entire FIFO array is written, the full condition is signaled by ORing all the $\overline{FF}$ pins, further writes are inhibited. On the last physical read of the first device, its $\overline{XO}$/($\overline{HF}$) will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. On the last read, an empty condition is signaled by "ORing" all of the $\overline{EF}$ pins. This inhibits further reads. While in the depth expansion mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE

MODE	INPUTS						OUTPUTS				NOTES
	$\overline{W}$	$\overline{R}$	$\overline{RS}$	$\overline{FL/RT}$	$\overline{XI}$	D1-D9	$\overline{EF}$	$\overline{FF}$	$\overline{XO/HF}$	Q1-Q9	
RESET	H	H	L	X	X	X	L	H	X	X	
WRITE	L	X	H	X	X	Data In	X	H	X	X	1
READ	X	L	H	X	X	X	H	X	X	Data Out	2
EMPTY (LAST READ)	X	H→L	H	X	X	X	H→L	X	X	Data Out	
FULL (LAST WRITE)	H→L	X	H	X	X	Data In	X	H→L	L	X	
HALF-FULL	H→L	X	H	X	X	Data In	X	H	H→L	X	3, 4
RETRANSMIT	H	H	H	L	X	X	H	X	X	X	4

FIFO

NOTES:
1. WRITE operations are independent of READ operations.
2. READ operations are independent of WRITE operations.
3. The half-full location is (1024/2 + 1) or 513.
4. Functional in stand alone mode only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -0.5V to +7.0V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All inputs	V_{IL}	-0.5	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}$, $\overline{R} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}		100	mA	3
Power Supply Current: Standby	$\overline{W}$, $\overline{R} \ge V_{IH}$, V_{CC} = Max.	I_{SB1}		10	mA	
	$\overline{W}$, $\overline{R} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}		1	mA	
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		8	pF	4
Output Capacitance	V_{CC} = 5V	C_O		8	pF	4

FIFO

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

A.C. CHARACTERISTICS		-25		-30		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access Time	t_A		25		30		35	ns	
READ Cycle Time	t_{RC}	35		40		45		ns	
READ Recovery Time	t_{RR}	10		10		10		ns	
Read Pulse Width	t_{RPW}	25		30		35		ns	
Read LOW to low Z	t_{RLZ}	5		5		5		ns	
Read to HIGH to high Z	t_{RHZ}		18		20		20	ns	
Read HIGH to Data Valid	t_{DV}		18		20		20	ns	
WRITE Cycle Time	t_{WC}	35		40		45		ns	
Write Pulse Width	t_{WPW}	25		30		35		ns	
WRITE Recovery Time	t_{WR}	10		10		10		ns	
Write HIGH to LOW Z	t_{WLZ}	5		5		5		ns	5
Data Set-up Time	t_{DS}	15		18		20		ns	
Data Hold Time	t_{DH}	0		0		0		ns	
RESET Cycle Time	t_{RCS}	35		40		45		ns	
Reset Pulse Width	t_{RSP}	25		30		35		ns	6
RESET Recovery Time	t_{RSR}	10		10		10		ns	
Read HIGH to Reset HIGH	t_{RRS}	25		30		35		ns	
Write HIGH to Reset HIGH	t_{WRS}	25		30		35		ns	
RETRANSMIT Cycle Time	t_{RTC}	35		40		45		ns	
Retransmit Pulse Width	t_{RT}	25		30		35		ns	
RETRANSMIT Recovery Time	t_{RTR}	10		10		12		ns	
Retransmit Set-up Time	t_{RTS}	25		30		35		ns	
Reset to $\overline{EF}$ LOW	t_{EFL}		35		40		45	ns	
Reset to $\overline{FF}$ HIGH	t_{FFH}		35		40		45	ns	
Reset to $\overline{HF}$ HIGH	t_{HFH}		35		40		45	ns	
Read LOW to $\overline{EF}$ LOW	t_{REF}		25		30		35	ns	
Read HIGH to $\overline{FF}$ HIGH	t_{RFF}		25		30		35	ns	
Write LOW to $\overline{FF}$ LOW	t_{WFF}		25		30		35	ns	
Write HIGH to $\overline{EF}$ HIGH	t_{WEF}		25		30		35	ns	
Write LOW to $\overline{HF}$ LOW	t_{WHF}		35		40		45	ns	
Read HIGH to $\overline{HF}$ HIGH	t_{RHF}		35		40		45	ns	
Read Pulse after $\overline{EF}$ HIGH	t_{RPE}	25		30		35		ns	5
Write Pulse Width after $\overline{FF}$ HIGH	t_{WPF}	25		30		35		ns	
Read/Write to $\overline{XO}$ LOW	t_{XOL}		25		30		35	ns	
Read/Write to $\overline{XO}$ HIGH	t_{XOH}		25		30		35	ns	
$\overline{XI}$ Pulse Width	t_{XIP}	25		30		35		ns	
$\overline{XI}$ Set-up Time	t_{XIS}	15		15		15		ns	
$\overline{XI}$ Recovery Time	t_{XIR}	10		10		10		ns	

FIFO

NOTES

1. All voltages referenced to V_{SS} (GND).
2. -3.0V for pulse width < 20ns.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through data mode only.
6. Pulse widths less than minimum are not allowed.

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 1

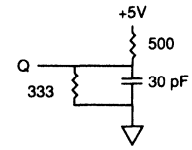
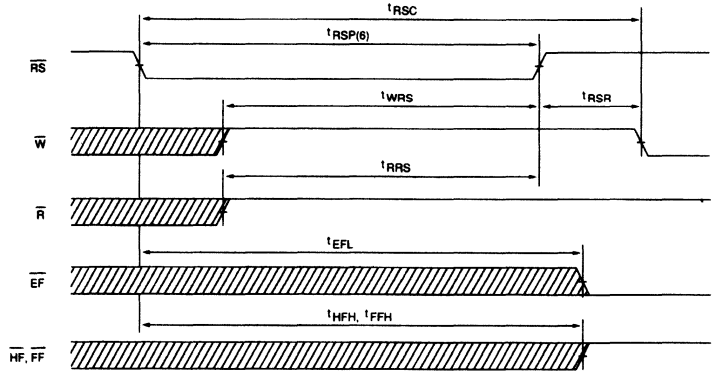
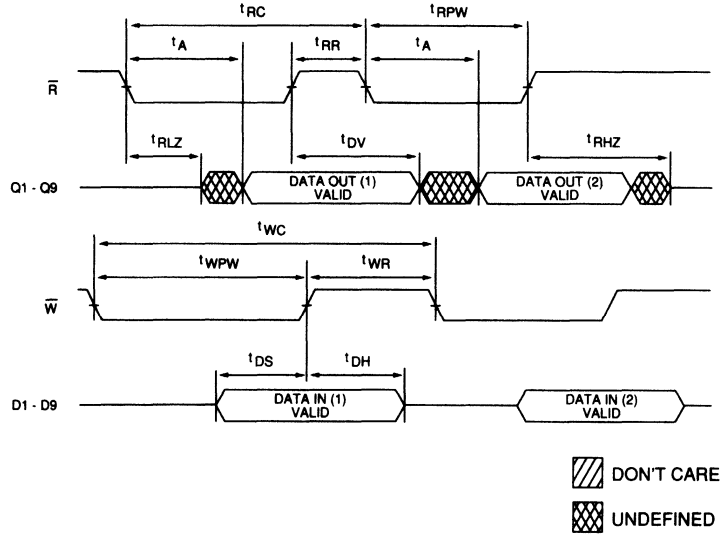


Fig. 1 OUTPUT LOAD EQUIVALENT

RESET

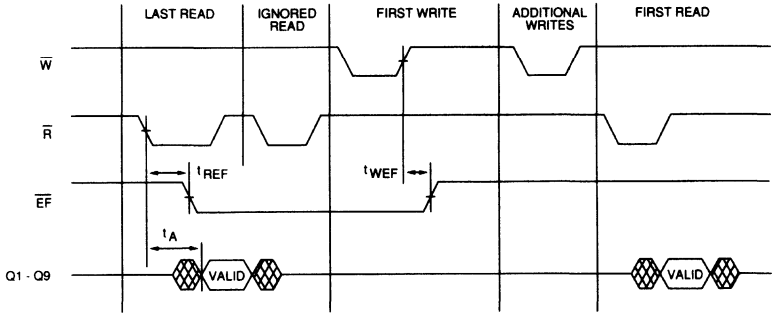


ASYNCHRONOUS READ AND WRITE

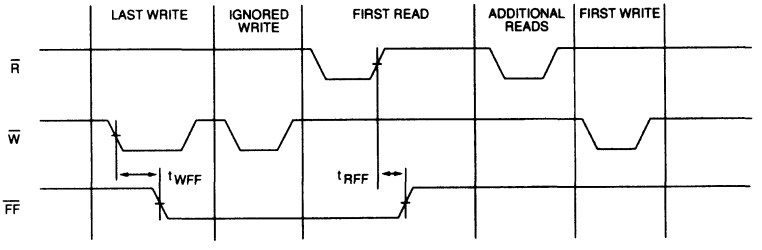


FIFO

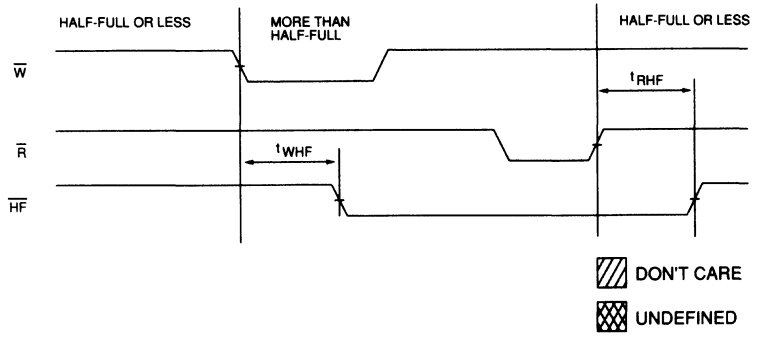
EMPTY FLAG



FULL FLAG

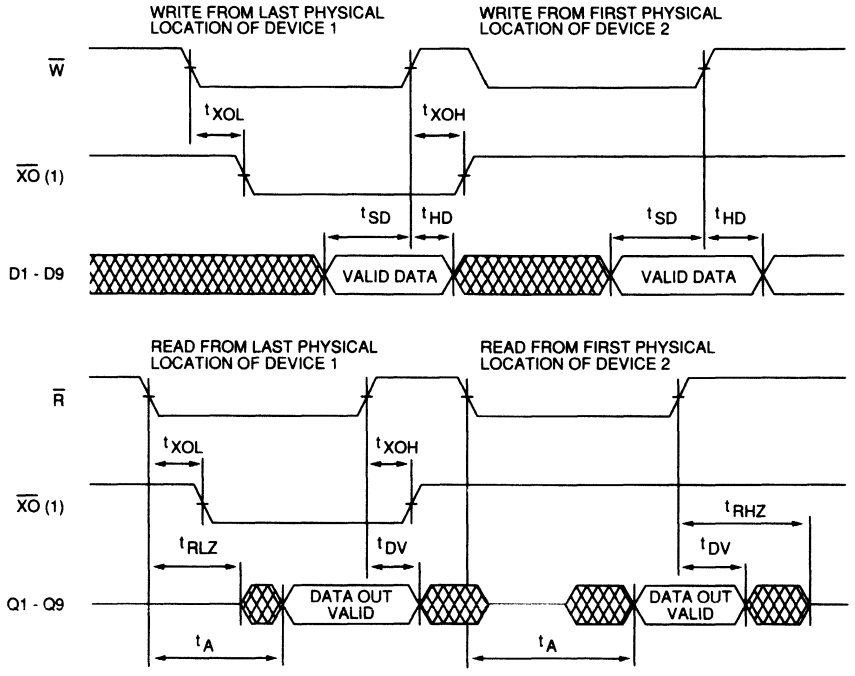


HALF-FULL FLAG



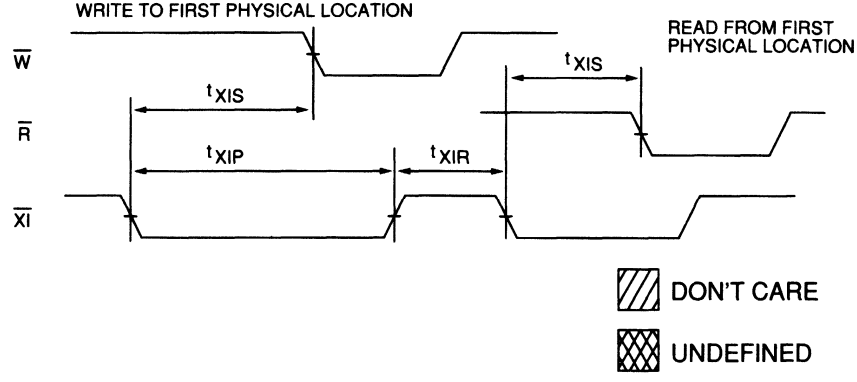
FIFO

EXPANSION MODE ($\overline{XO}$)



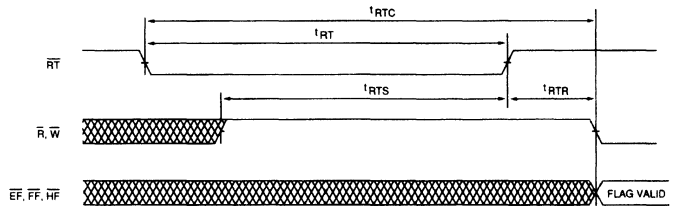
Note 1: $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

EXPANSION MODE ($\overline{XI}$)

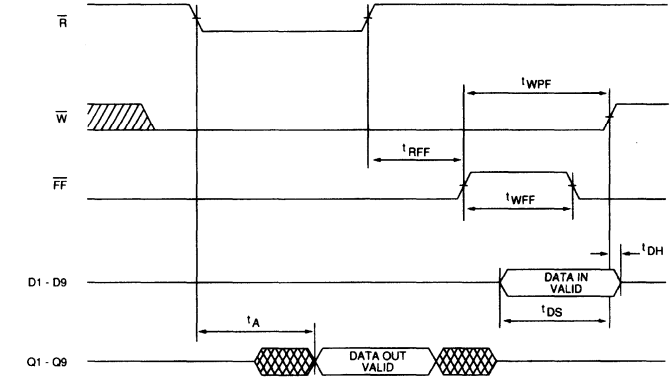


FIFO

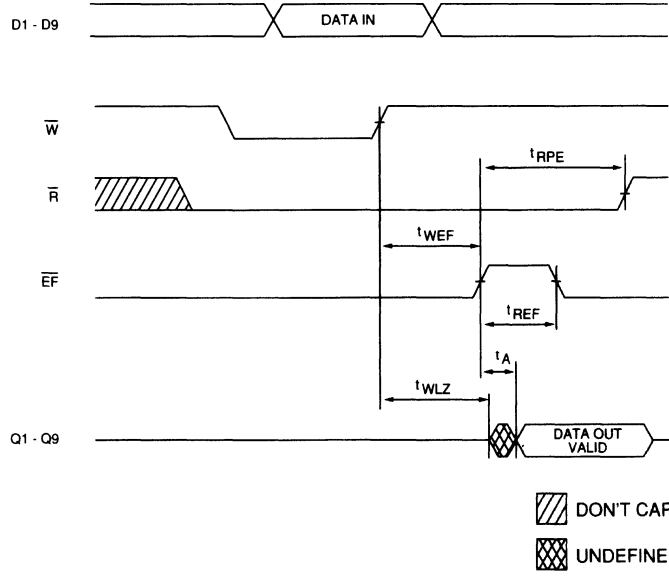
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH



FIFO

FIFO

1K x 9 FIFO

MAILBOX REGISTER

FEATURES

- High speed: 25ns access, 35ns cycle time
- Asynchronous and simultaneous READ and WRITE
- Empty and Full Flags
- Automatic retransmit
- Transistor loads for maximum data integrity
- Low power
- Programmable Mailbox register

OPTIONS — MARKING

- Timing

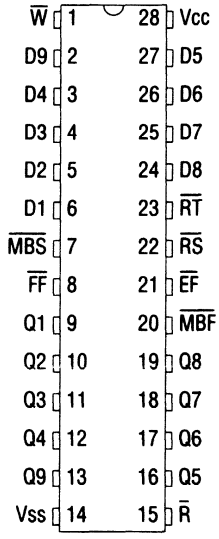
25ns access time	-25
30ns access time	-30
35ns access time	-35

- Packages

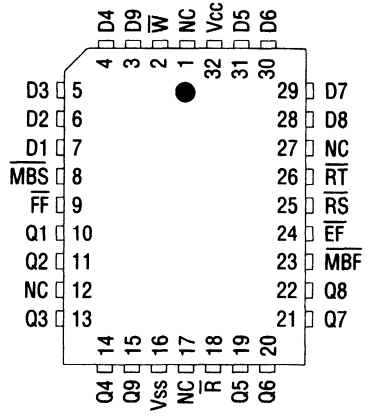
Plastic DIP	None
Ceramic DIP	C
PLCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 6-transistor memory cell with resistive loads. They are fabricated using silicon gate CMOS technology.

There are three major user options that are available separately or in combination: expandable, mailbox register, and variable flags. Expandable FIFOs are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFOs have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFOs allow the user to program the level of two additional full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

1K x 9 FIFO

VARIABLE FLAGS

FEATURES

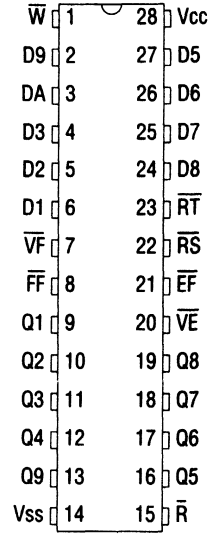
- High speed: 25ns access, 35ns cycle time
- Asynchronous and simultaneous READ and WRITE
- Empty and Full Flags
- Automatic retransmit
- Transistor loads for maximum data integrity
- Low power
- Programmable Empty/Full Flags (128 increments)

OPTIONS — MARKING

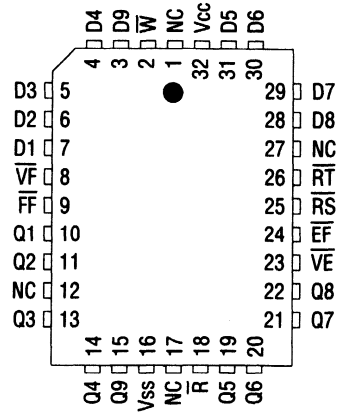
- Timing
  - 25ns access time — -25
  - 30ns access time — -30
  - 35ns access time — -35
- Packages
  - Plastic DIP — None
  - Ceramic DIP — C
  - PLCC — EJ
  - Ceramic LCC — EC

PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 6-transistor memory cell with resistive loads. They are fabricated using silicon gate CMOS technology.

There are three major user options that are available separately or in combination: expandable, mailbox register, and variable flags. Expandable FIFOs are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFOs have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFOs allow the user to program the level of two additional full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

1K x 16 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

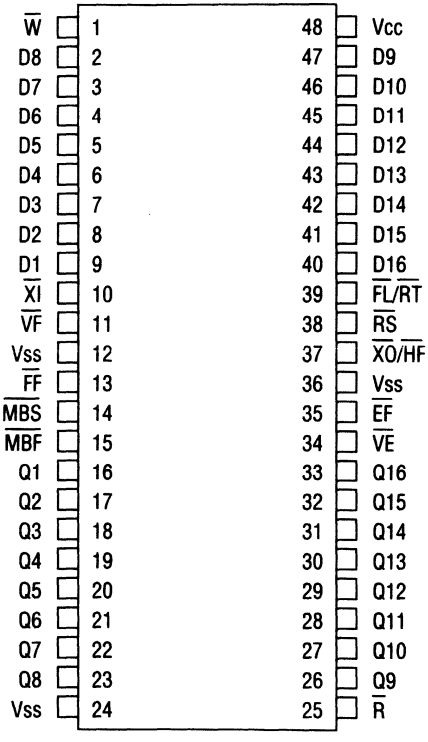
- High speed: 25ns access, 35ns cycle time
- 16-bit word width
- Asynchronous and simultaneous READ and WRITE
- Empty and Full Flags
- Easy expansion capability
- Automatic retransmit
- Transistor loads for maximum data integrity
- Low power
- Programmable Mailbox register
- Programmable Empty/Full Flags (128 increments)

OPTIONS

	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

48L DIP



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 6-transistor memory cell with resistive loads. They are fabricated using silicon gate CMOS technology.

There are three major user options that are available separately or in combination: expandable, mailbox register, and variable flags. Expandable FIFOs are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFOs have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFOs allow the user to program the level of two additional full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

1K x 16 to 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

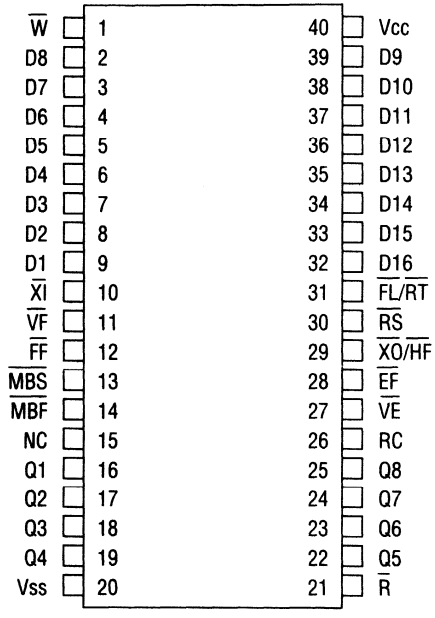
- High speed: 25ns access, 35ns cycle time
- Asynchronous and simultaneous READ and WRITE
- Empty and Full Flags
- Easy expansion capability
- Automatic retransmit
- Transistor loads for maximum data integrity
- One chip interface between a 16 bit bus and an 8 bit bus
- Low power
- Programmable Mailbox register
- Programmable Empty/Full Flags (128 increments)

OPTIONS — MARKING

- Timing
  - 25ns access time — -25
  - 30ns access time — -30
  - 35ns access time — -35
- Packages
  - Plastic DIP — None
  - Ceramic DIP — C

PIN ASSIGNMENT (Top View)

40L DIP



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 6-transistor memory cell with resistive loads. They are fabricated using silicon gate CMOS technology.

There are three major user options that are available separately or in combination: expandable, mailbox register, and variable flags. Expandable FIFOs are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFOs have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFOs allow the user to program the level of two additional full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

2K x 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

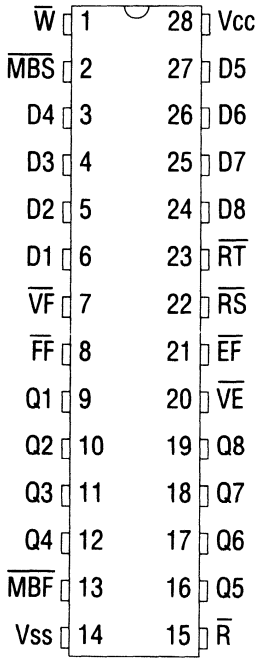
- High speed: 25ns access, 35ns cycle time
- Asynchronous and simultaneous READ and WRITE
- Empty and Full Flags
- Automatic retransmit
- Transistor loads for maximum data integrity
- Low power
- Programmable Mailbox register
- Programmable Empty/Full Flags (128 increments)

OPTIONS

OPTIONS	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

28L DIP



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 6-transistor memory cell with resistive loads. They are fabricated using silicon gate CMOS technology.

There are three major user options that are available separately or in combination: expandable, mailbox register, and variable flags. Expandable FIFOs are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFOs have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFOs allow the user to program the level of two additional full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

2K x 9 FIFO

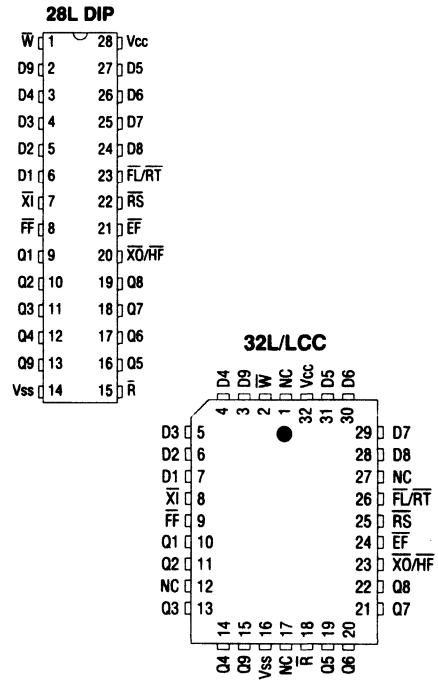
FEATURES

- Very high speed: 25, 30, and 35ns access
- High performance, low power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby); 350mW typ. (act.)
- TTL compatible inputs and outputs
- Asynchronous and simultaneous READ and WRITE
- Empty, Half-Full and Full Flags
- Auto-retransmit capability
- Fully expandable width and depth
- Pin function compatible with higher density 9000 series FIFOs

OPTIONS

	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP (600 mil)	None
Ceramic DIP (600 mil)	C
PLCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

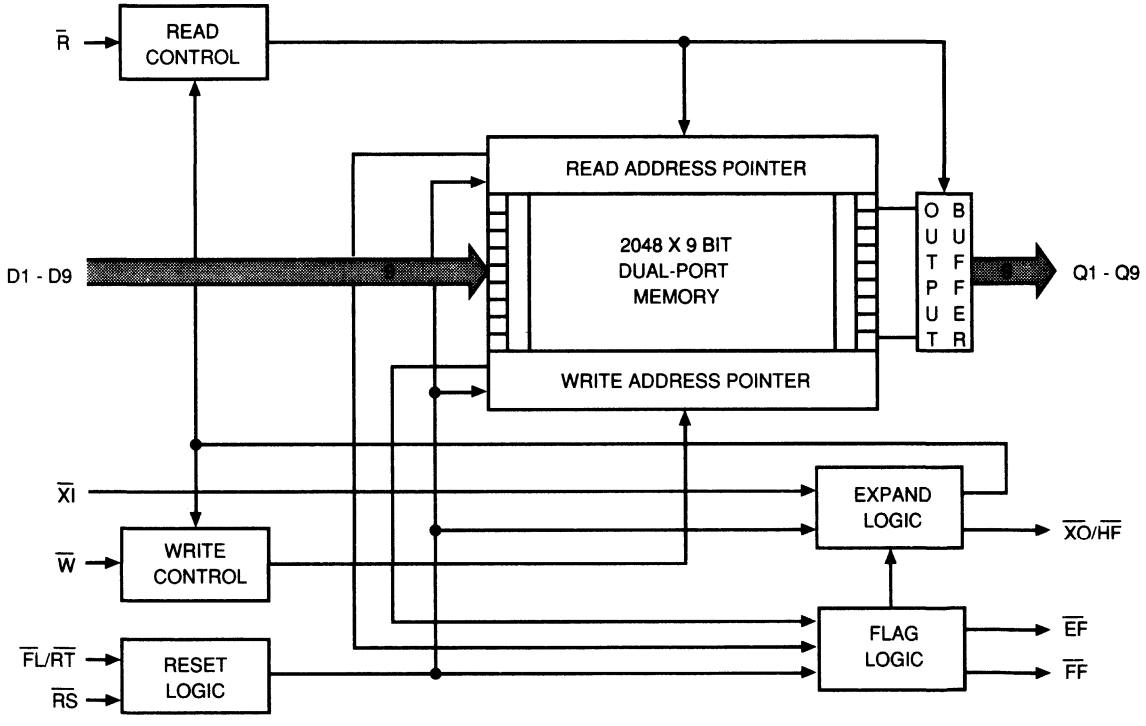


GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port, 6-transistor memory cell with resistive loads.

These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information can be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates. Visibility of the memory volume is given through empty, half-full, and full flags. While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain high impedance. Expansion out, expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the stand alone mode.

The depth of the FIFO can be expanded by cascading multiple devices in the depth expansion mode. Also, the MT52C9020 is speed, function and pin compatible with higher density FIFOs from Micron. This upward compatibility with the 4K x 9 FIFO provides a single chip depth expansion solution.



FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: Taking $\overline{RS}$ LOW will reset the FIFO by initializing the read and write pointers and all flags. After the device is powered up, it must be reset before any writes can take place. Reset also samples $\overline{XI}$ and $\overline{FL/RT}$ to set the depth expansion mode.
2	1	$\overline{W}$	Input	Write Strobe: $\overline{W}$ is taken LOW to write data from the input port (D1 - D9) into the FIFO memory array.
18	15	$\overline{R}$	Input	Read Strobe: $\overline{R}$ is taken LOW to read data from the FIFO memory array to the output port (Q1 - Q9).
8	7	$\overline{XI}$	Input	Expansion In: Sets mode of operation on the L→H transition of $\overline{RS}$; stand alone when LOW; depth expansion when HIGH. When in depth expansion, $\overline{XI}$ will be pulsed LOW once to enable write pointer, then again to enable read pointer.
26	23	$\overline{FL/RT}$	Input	First Load: In depth expansion mode, $\overline{FL}$ will enable the device as the first to be loaded, (enables read and write pointers) when LOW during the L→H transition of $\overline{RS}$. Retransmit: In stand alone mode, $\overline{RT}$ is used to enable the RETRANSMIT cycle. When taken LOW, $\overline{RT}$ resets the read pointer to the first data location and the FIFO is then ready to retransmit data on the following READ operation(s). The flags will be affected according to specific data conditions.
3, 4, 5, 6, 7 28, 29, 30,31	2, 3, 4, 5, 6 24, 25, 26,27	D1 - D9	Input	Data Inputs
24	21	$\overline{EF}$	Output	Empty Flag: Indicates empty FIFO memory when LOW, inhibiting further READ cycles.
9	8	$\overline{FF}$	Output	Full Flag: Indicates full FIFO memory when LOW, inhibiting further WRITE cycles.
23	20	$\overline{XO/HF}$	Output	Expansion Out: During depth expansion, $\overline{XO}$ will pulse LOW on the last physical WRITE and READ operations, disabling writes then reads to the FIFO. Half-full Flag: During stand alone operation $\overline{HF}$ indicates when the (Half-full + 1) memory location is written; will stay LOW until the (Half-full + 1) location is read.
10,11,13,14 15, 19, 20,21,22	9,10,11,12,13 16, 17, 18,19	Q1 - Q9	Output	Data Output: Output or high impedance.
32	28	Vcc	Supply	Power Supply: +5V 10%
16	14	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9020 uses a dual-port SRAM memory cell with separate read and write pointers that results in a flexible length FIFO buffer memory, with independent, asynchronous READ and WRITE capabilities and with no fallthrough or bubblethrough time constraints.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing half-full flags the $\overline{XO}/\overline{HF}$ pin will be shown as $(\overline{XO})/\overline{HF}$.*

RESET

After Vcc is stable, RESET ($\overline{RS}$) must be taken LOW to initialize the read and write pointers and flags. RESET also sets the mode of operation, stand alone or expanded. During the RESET pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the stand alone or depth expansion mode. The stand alone mode is entered when $\overline{XI}$ is LOW during the RESET cycle. When $\overline{XI}$ is HIGH or is connected to $\overline{XO}/(\overline{HF})$ of another FIFO, the depth expansion mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW, while $\overline{FF}$ is HIGH. The WRITE cycle is initiated by the falling edge of $\overline{W}$ and data on the D1-D9 pins is latched on the rising edge. If the location to be written is the last empty location in the FIFO, the $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is LOW, any attempted writes will be inhibited, with no loss of data already stored in the FIFO. When a device is used in the stand alone mode, $(\overline{XO})/\overline{HF}$ is asserted when the half-full-plus-one location (2048/2 + 1) is written. It will stay asserted until the half-full-plus-one location is read or the FIFO is reset. The first write to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the depth expansion mode, the last write to a FIFO will cause $\overline{FF}$ to go LOW and will cause $\overline{XI}$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and data is available ($\overline{EF}$ is HIGH). The data-out (Q1 - Q9) pins will go active (low Z) ^tRLZ after the falling edge of $\overline{R}$ and valid data will appear ^tA after the falling edge of $\overline{R}$. When the last data word is read, $\overline{EF}$ will go LOW after the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (high Z). When the FIFO is being used in the single device mode and the half-full-plus-one location is read, $(\overline{XO})/\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$. When the FIFO is full ($\overline{FF}$ asserted) and a read is initiated, $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the expanded mode, the last read to a FIFO will cause the $\overline{EF}$ to go LOW and will cause $\overline{XI}$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the stand alone mode, the MT52C9020 allows the receiving device to request that data just read from the FIFO to be repeated. When the $(\overline{FL})/\overline{RT}$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may again start reading the data from the beginning of the FIFO ^tRTR after $(\overline{FL})/\overline{RT}$ is taken HIGH. The empty, half-full and full flags will be affected as specified for the data volume.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty points, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a flow-through write. Flow-through writes are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a flow-through read can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. Flow-through reads are initiated from the rising edge of $\overline{W}$ and access time measured from the rising edge of $\overline{EF}$.

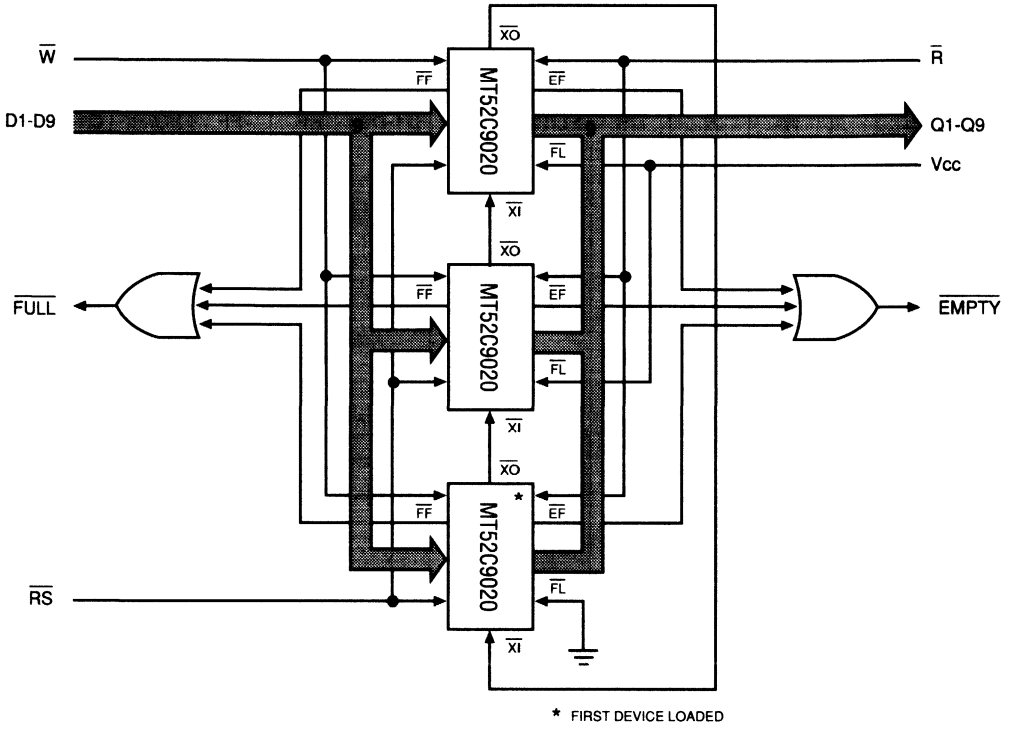


Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the stand alone or groups of expanded depth mode FIFOs. Expanded width operation is acheived by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1), when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9020s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}$/($\overline{HF}$) and $\overline{FL}$/($\overline{RT}$). Figure 1 illustrates a typical three device expansion. The depth expansion mode is entered during a reset cycle, by tying the $\overline{XO}$/($\overline{HF}$) pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}$/($\overline{RT}$) pin grounded. The remaining devices in the chain will have $\overline{FL}$/($\overline{RT}$) tied HIGH. During reset cycle, $\overline{XO}$/($\overline{HF}$) of each device goes HIGH, disabling the read and write pointers of every FIFO, except the first load device. When the last physical location of the first device is written, the $\overline{XO}$/($\overline{HF}$) pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling the first. The writes will continue to go to the second device until it is full. Then it will "pass" the write pointer to the third device. This process continues until all devices are full. When the entire FIFO array is written, the full condition is signaled by ORing all the $\overline{FF}$ pins, further writes are inhibited. On the last physical read of the first device, its $\overline{XO}$/($\overline{HF}$) will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. On the last read, an empty condition is signaled by "ORing" all of the $\overline{EF}$ pins. This inhibits further reads. While in the depth expansion mode, the half-full flag and retransmit functions are not available.

TRUTH TABLE

MODE	INPUTS						OUTPUTS				NOTES
	$\overline{W}$	$\overline{R}$	$\overline{RS}$	$\overline{FL/RT}$	$\overline{XI}$	D1-D9	$\overline{EF}$	$\overline{FF}$	$\overline{XO/HF}$	Q1-Q9	
RESET	H	H	L	X	X	X	L	H	X	X	
WRITE	L	X	H	X	X	Data In	X	H	X	X	1
READ	X	L	H	X	X	X	H	X	X	Data Out	2
EMPTY (LAST READ)	X	H→L	H	X	X	X	H→L	X	X	Data Out	
FULL (LAST WRITE)	H→L	X	H	X	X	Data In	X	H→L	L	X	
HALF-FULL	H→L	X	H	X	X	Data In	X	H	H→L	X	3, 4
RETRANSMIT	H	H	H	L	X	X	H	X	X	X	4

FIFO

NOTES:
1. WRITE operations are independent of READ operations.
2. READ operations are independent of WRITE operations.
3. The half-full location is (2048/2 + 1) or 1025.
4. Functional in stand alone mode only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -0.5V to +7.0V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All inputs	V_{IL}	-0.5	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}$, $\overline{R} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}		100	mA	3
Power Supply Current: Standby	$\overline{W}$, $\overline{R} \ge V_{IH}$, V_{CC} = Max.	I_{SB1}		10	mA	
	$\overline{W}$, $\overline{R} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}		1	mA	
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		8	pF	4
Output Capacitance	V_{CC} = 5V	C_O		8	pF	4

FIFO

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C, Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-25		-30		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access Time	t_A		25		30		35	ns	
READ Cycle Time	t_{RC}	35		40		45		ns	
READ Recovery Time	t_{RR}	10		10		10		ns	
Read Pulse Width	t_{RPW}	25		30		35		ns	
Read LOW to low Z	t_{RLZ}	5		5		5		ns	
Read to HIGH to high Z	t_{RHZ}		18		20		20	ns	
Read HIGH to Data Valid	t_{DV}		18		20		20	ns	
WRITE Cycle Time	t_{WC}	35		40		45		ns	
Write Pulse Width	t_{WPW}	25		30		35		ns	
WRITE Recovery Time	t_{WR}	10		10		10		ns	
Write HIGH to LOW Z	t_{WLZ}	5		5		5		ns	5
Data Set-up Time	t_{DS}	15		18		20		ns	
Data Hold Time	t_{DH}	0		0		0		ns	
RESET Cycle Time	t_{RCS}	35		40		45		ns	
Reset Pulse Width	t_{RSP}	25		30		35		ns	6
RESET Recovery Time	t_{RSR}	10		10		10		ns	
Read HIGH to Reset HIGH	t_{RRS}	25		30		35		ns	
Write HIGH to Reset HIGH	t_{WRS}	25		30		35		ns	
RETRANSMIT Cycle Time	t_{RTC}	35		40		45		ns	
Retransmit Pulse Width	t_{RT}	25		30		35		ns	
RETRANSMIT Recovery Time	t_{RTR}	10		10		12		ns	
Retransmit Set-up Time	t_{RTS}	25		30		35		ns	
Reset to $\overline{EF}$ LOW	t_{EFL}		35		40		45	ns	
Reset to $\overline{FF}$ HIGH	t_{FFH}		35		40		45	ns	
Reset to $\overline{HF}$ HIGH	t_{HFH}		35		40		45	ns	
Read LOW to $\overline{EF}$ LOW	t_{REF}		25		30		35	ns	
Read HIGH to $\overline{FF}$ HIGH	t_{RFF}		25		30		35	ns	
Write LOW to $\overline{FF}$ LOW	t_{WFF}		25		30		35	ns	
Write HIGH to $\overline{EF}$ HIGH	t_{WEF}		25		30		35	ns	
Write LOW to $\overline{HF}$ LOW	t_{WHF}		35		40		45	ns	
Read HIGH to $\overline{HF}$ HIGH	t_{RHF}		35		40		45	ns	
Read Pulse after $\overline{EF}$ HIGH	t_{RPE}	25		30		35		ns	5
Write Pulse Width after $\overline{FF}$ HIGH	t_{WPF}	25		30		35		ns	
Read/Write to $\overline{XO}$ LOW	t_{XOL}		25		30		35	ns	
Read/Write to $\overline{XO}$ HIGH	t_{XOH}		25		30		35	ns	
$\overline{XI}$ Pulse Width	t_{XIP}	25		30		35		ns	
$\overline{XI}$ Set-up Time	t_{XIS}	15		15		15		ns	
$\overline{XI}$ Recovery Time	t_{XIR}	10		10		10		ns	

FIFO

NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through data mode only.
6. Pulse widths less than minimum are not allowed.

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 1

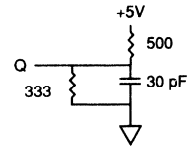
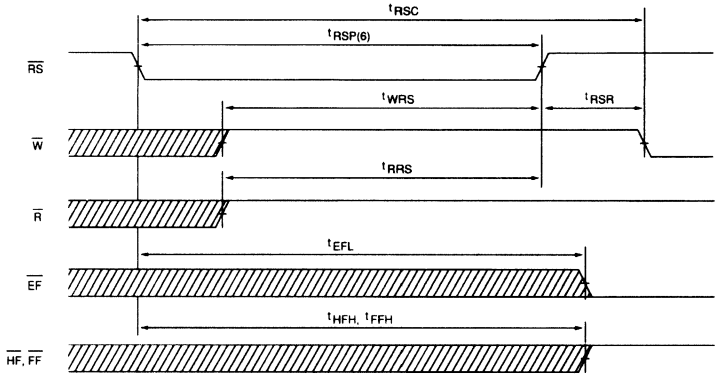
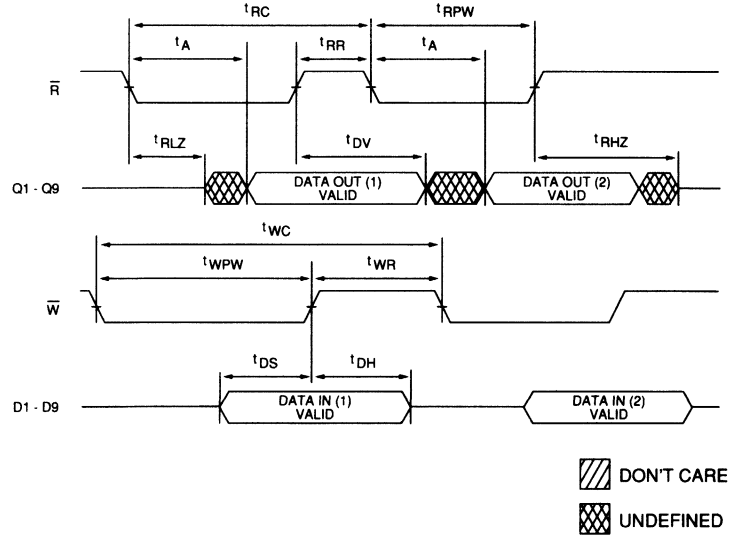


Fig. 1 OUTPUT LOAD EQUIVALENT

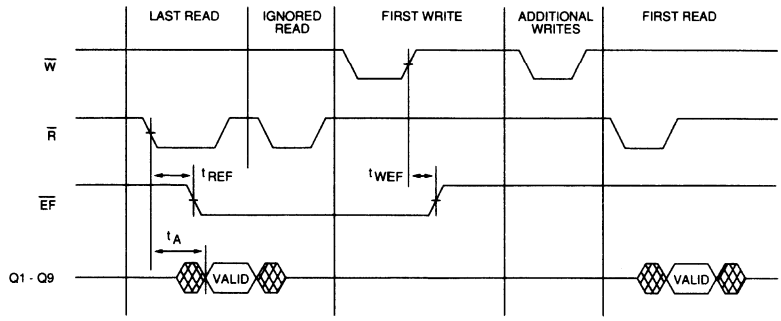
RESET



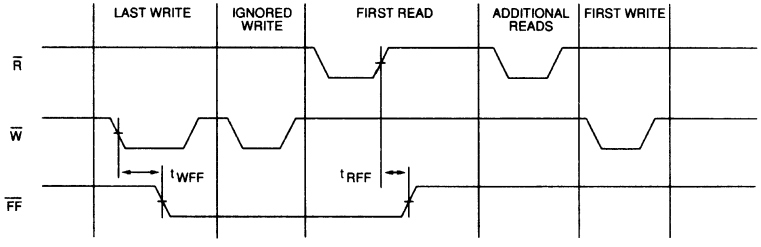
ASYNCHRONOUS READ AND WRITE



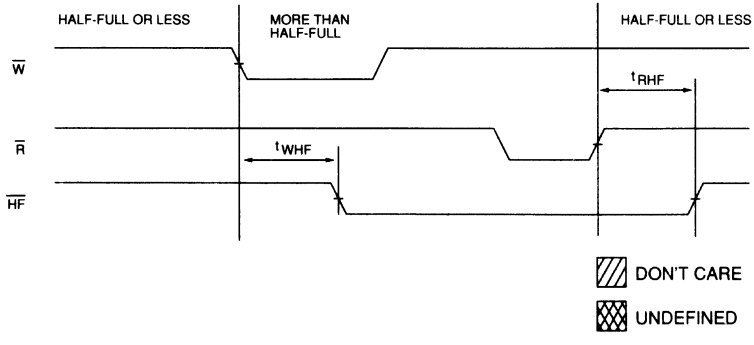
EMPTY FLAG



FULL FLAG

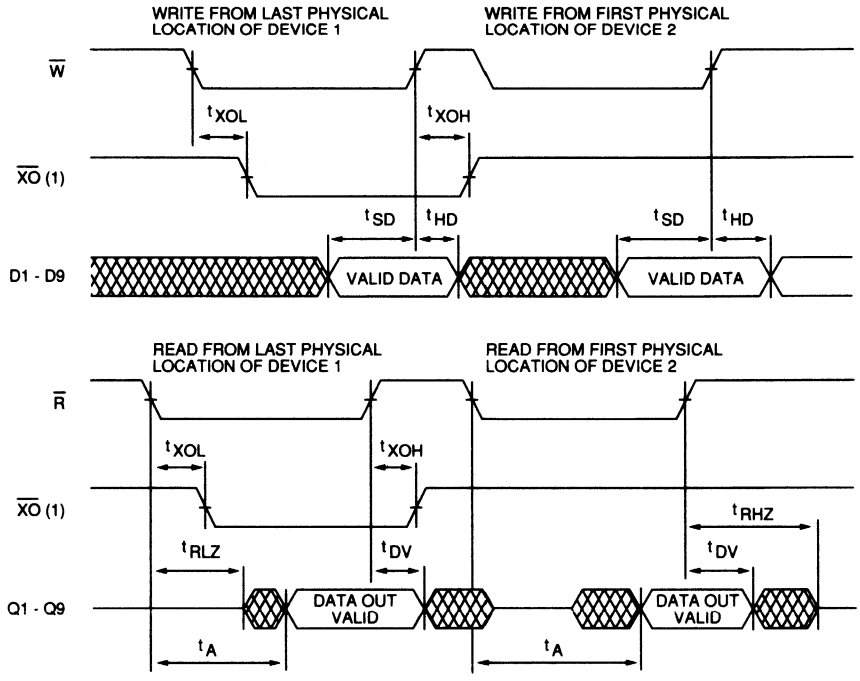


HALF-FULL FLAG



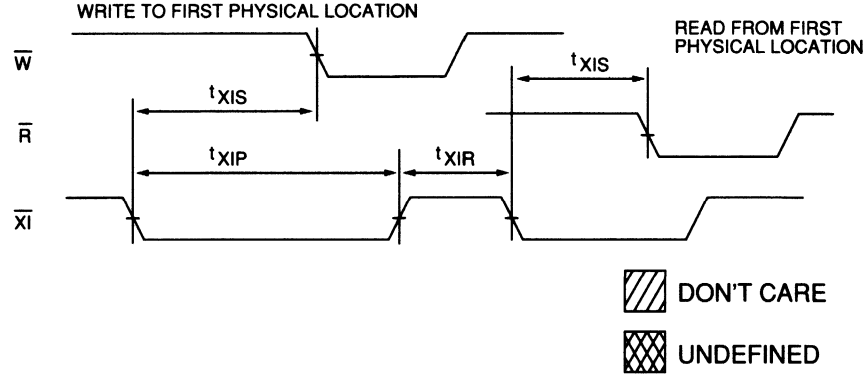
FIFO

EXPANSION MODE ($\overline{XO}$)



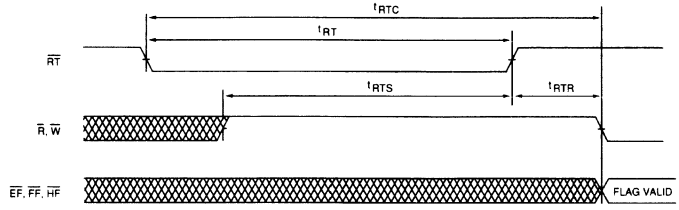
Note 1: $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

EXPANSION MODE ($\overline{XI}$)

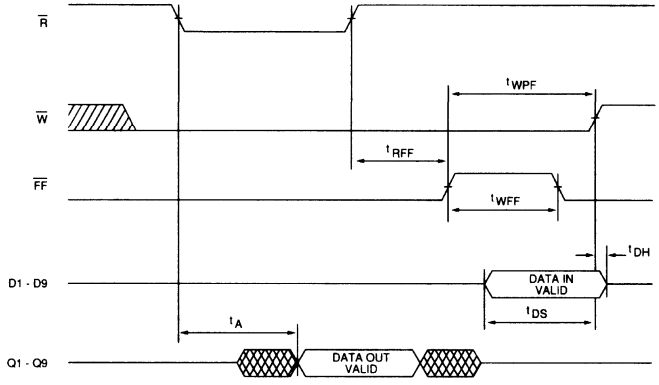


FIFO

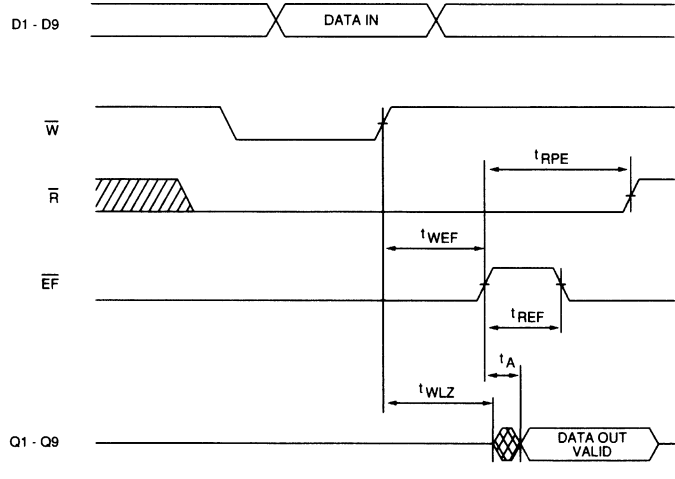
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH



FIFO

FIFO

2K x 9 FIFO

MAILBOX REGISTER

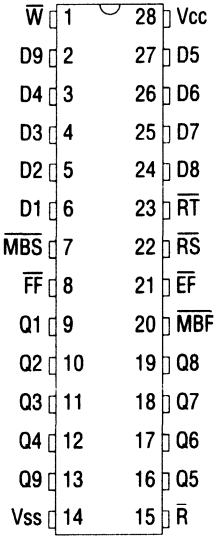
FEATURES

- High speed: 25ns access, 35ns cycle time
- Asynchronous and simultaneous READ and WRITE
- Empty and Full Flags
- Automatic retransmit
- Transistor loads for maximum data integrity
- Low power
- Programmable Mailbox register

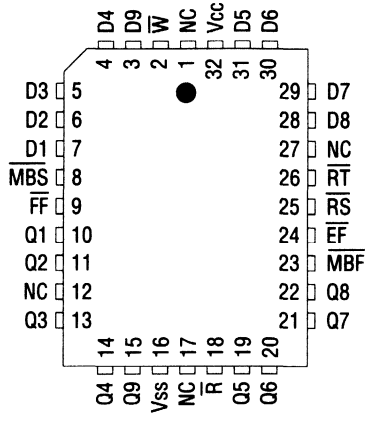
OPTIONS	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C
PLCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 6-transistor memory cell with resistive loads. They are fabricated using silicon gate CMOS technology.

There are three major user options that are available separately or in combination: expandable, mailbox register, and variable flags. Expandable FIFOs are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFOs have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFOs allow the user to program the level of two additional full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

2K x 9 FIFO

VARIABLE FLAGS

FEATURES

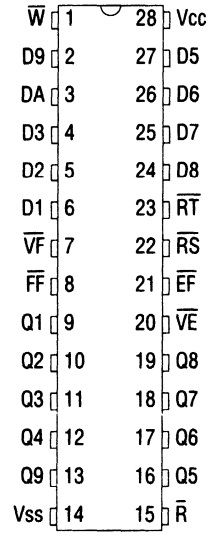
- High speed: 25ns access, 35ns cycle time
- Asynchronous and simultaneous READ and WRITE
- Empty and Full Flags
- Automatic retransmit
- Transistor loads for maximum data integrity
- Low power
- Programmable Empty/Full Flags (128 increments)

OPTIONS

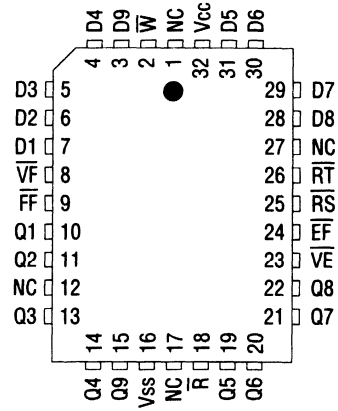
	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic LCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



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All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

2K x 16 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

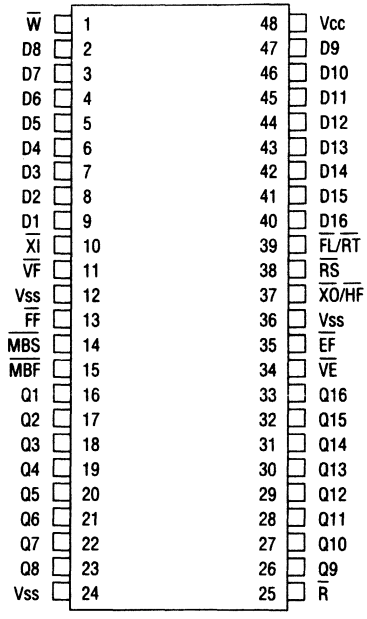
- Very high speed: 25, 30, and 35ns access
- High performance, low power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby); 350mW typ. (act.)
- TTL compatible inputs and outputs
- Asynchronous and simultaneous READ and WRITE
- Empty, Half-Full and Full Flags
- Auto-retransmit capability
- Fully expandable width and depth
- Mailbox Register
- Programmable Full and Empty Flags (128 increments)
- 16 bit data bus reduces chip count

OPTIONS

	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP (600 mil)	None
Ceramic DIP (600 mil)	C
PLCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

48L DIP



FIFO

GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port, 6-transistor memory cell with resistive loads.

These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information can be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates. Visibility of the memory volume is given through empty, variable empty, half-full, variable full, and full flags. While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain high impedance. The variable empty, and full flags are programmed to an offset from empty and full, respectively. A mailbox register and mailbox full flag provide single word transfer around the FIFO memory array. A retransmit pin allows data to be resent on the receiver's request when the FIFO is in the stand alone mode.

The depth of the FIFO can be expanded by cascading multiple devices in the depth expansion mode. Expansion out, expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation.

FIFO

2K x 16/8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

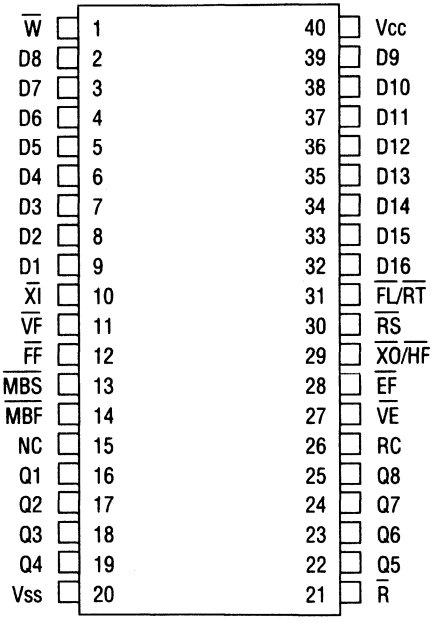
- Very high speed: 25, 30, and 35ns access
- High performance, low power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby), 350mW typ. (act.)
- TTL compatible inputs and outputs
- Asynchronous and simultaneous READ and WRITE
- Empty, Half-Full and Full Flags
- Auto-retransmit capability
- Fully expandable width and depth
- Mailbox Register
- Programmable Full and Empty Flags (128 increments)
- Bus muxing from 16 to 8 bits

OPTIONS

	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP (600 mil)	None
Ceramic DIP (600 mil)	C
PLCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

40L DIP



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port, 6-transistor memory cell with resistive loads.

These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information can be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates. Visibility of the memory volume is given through empty, variable empty, half-full, variable full, and full flags. While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain high impedance. The variable empty, and full flags are programmed to an offset from empty and full, respectively. A mailbox register and mailbox full flag provide single word transfer around the FIFO memory array. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the stand alone mode.

The depth of the FIFO can be expanded by cascading multiple devices in the depth expansion mode. Expansion out, expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation.

FIFO

4K x 8 FIFO

VARIABLE FLAGS/MAILBOX REGISTER

FEATURES

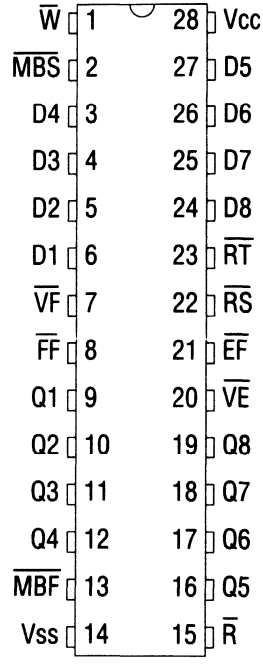
- High speed: 25ns access, 35ns cycle time
- Asynchronous and simultaneous READ and WRITE
- Empty and Full Flags
- Automatic retransmit
- Transistor loads for maximum data integrity
- Low power
- Programmable Mailbox register
- Programmable Empty/Full Flags (128 increments)

OPTIONS

OPTIONS	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C

PIN ASSIGNMENT (Top View)

28L DIP



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 6-transistor memory cell with resistive loads. They are fabricated using silicon gate CMOS technology.

There are three major user options that are available separately or in combination: expandable, mailbox register, and variable flags. Expandable FIFOs are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFOs have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFOs allow the user to program the level of two additional full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO 4K x 9 FIFO

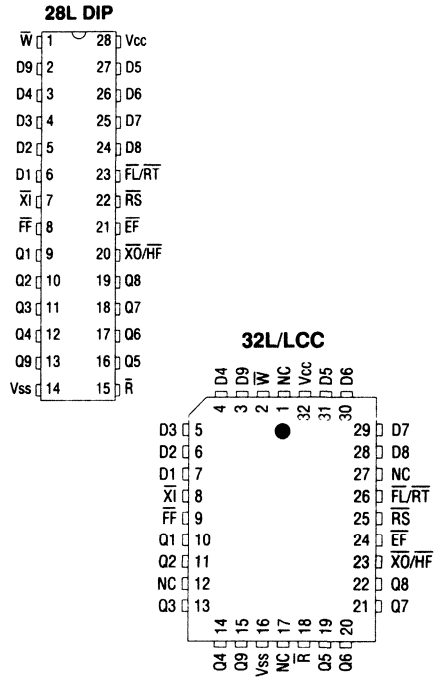
FEATURES

- Very high speed: 25, 30, and 35ns access
- High performance, low power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby); 350mW typ. (act.)
- TTL compatible inputs and outputs
- Asynchronous and simultaneous READ and WRITE
- Empty, Half-Full and Full Flags
- Auto-retransmit capability
- Fully expandable width and depth

OPTIONS MARKING

• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP (600 mil)	None
Ceramic DIP (600 mil)	C
PLCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

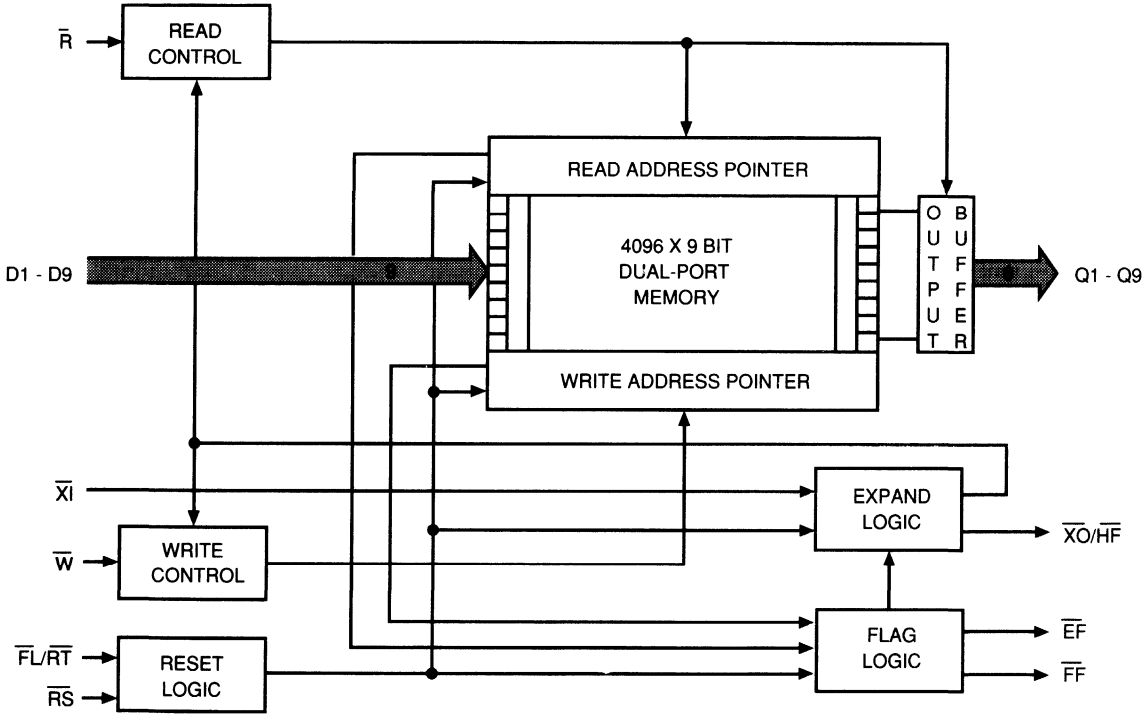


GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port, 6-transistor memory cell with resistive loads.

These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information can be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates. Visibility of the memory volume is given through empty, half-full, and full flags. While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain high impedance. Expansion out, expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the stand alone mode.

The depth of the FIFO can be expanded by cascading multiple devices in the depth expansion mode.



FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: Taking $\overline{RS}$ LOW will reset the FIFO by initializing the read and write pointers and all flags. After the device is powered up, it must be reset before any writes can take place. Reset also samples $\overline{XI}$ and $\overline{FL/RT}$ to set the depth expansion mode.
2	1	$\overline{W}$	Input	Write Strobe: $\overline{W}$ is taken LOW to write data from the input port (D1 - D9) into the FIFO memory array.
18	15	$\overline{R}$	Input	Read Strobe: $\overline{R}$ is taken LOW to read data from the FIFO memory array to the output port (Q1 - Q9).
8	7	$\overline{XI}$	Input	Expansion In: Sets mode of operation on the L→H transition of $\overline{RS}$; stand alone when LOW; depth expansion when HIGH. When in depth expansion, $\overline{XI}$ will be pulsed LOW once to enable write pointer, then again to enable read pointer.
26	23	$\overline{FL/RT}$	Input	First Load: In depth expansion mode, $\overline{FL}$ will enable the device as the first to be loaded, (enables read and write pointers) when LOW during the L→H transition of $\overline{RS}$. Retransmit: In stand alone mode, $\overline{RT}$ is used to enable the RETRANSMIT cycle. When taken LOW, $\overline{RT}$ resets the read pointer to the first data location and the FIFO is then ready to retransmit data on the following READ operation(s). The flags will be affected according to specific data conditions.
3, 4, 5, 6, 7 28, 29, 30,31	2, 3, 4, 5, 6 24, 25, 26,27	D1 - D9	Input	Data Inputs
24	21	$\overline{EF}$	Output	Empty Flag: Indicates empty FIFO memory when LOW, inhibiting further READ cycles.
9	8	$\overline{FF}$	Output	Full Flag: Indicates full FIFO memory when LOW, inhibiting further WRITE cycles.
23	20	$\overline{XO/HF}$	Output	Expansion Out: During depth expansion, $\overline{XO}$ will pulse LOW on the last physical WRITE and READ operations, disabling writes then reads to the FIFO. Half-full Flag: During stand alone operation $\overline{HF}$ indicates when the (Half-full + 1) memory location is written; will stay LOW until the (Half-full + 1) location is read.
10,11,13,14 15, 19, 20,21,22	9,10,11,12,13 16, 17, 18,19	Q1 - Q9	Output	Data Output: Output or high impedance.
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9040 uses a dual-port SRAM memory cell with separate read and write pointers that results in a flexible length FIFO buffer memory, with independent, asynchronous READ and WRITE capabilities and with no fallthrough or bubblethrough time constraints.

Note: *For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing half-full flags the $\overline{XO}/\overline{HF}$ pin will be shown as $(\overline{XO})/\overline{HF}$.*

RESET

After Vcc is stable, RESET ($\overline{RS}$) must be taken LOW to initialize the read and write pointers and flags. RESET also sets the mode of operation, stand alone or expanded. During the RESET pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the stand alone or depth expansion mode. The stand alone mode is entered when $\overline{XI}$ is LOW during the RESET cycle. When $\overline{XI}$ is HIGH or is connected to $\overline{XO}/(\overline{HF})$ of another FIFO, the depth expansion mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW, while $\overline{FF}$ is HIGH. The WRITE cycle is initiated by the falling edge of $\overline{W}$ and data on the D1-D9 pins is latched on the rising edge. If the location to be written is the last empty location in the FIFO, the $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is LOW, any attempted writes will be inhibited, with no loss of data already stored in the FIFO. When a device is used in the stand alone mode, $(\overline{XO})/\overline{HF}$ is asserted when the half-full-plus-one location (4096/2 + 1) is written. It will stay asserted until the half-full-plus-one location is read or the FIFO is reset. The first write to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the depth expansion mode, the last write to a FIFO will cause $\overline{FF}$ to go LOW and will cause $\overline{XI}$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and data is available ($\overline{EF}$ is HIGH). The data-out (Q1 - Q9) pins will go active (low Z) ^{t}RLZ after the falling edge of $\overline{R}$ and valid data will appear ^{t}A after the falling edge of $\overline{R}$. When the last data word is read, $\overline{EF}$ will go LOW after the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (high Z). When the FIFO is being used in the single device mode and the half-full-plus-one location is read, $(\overline{XO})/\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$. When the FIFO is full ($\overline{FF}$ asserted) and a read is initiated, $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the expanded mode, the last read to a FIFO will cause the $\overline{EF}$ to go LOW and will cause $\overline{XI}$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the stand alone mode, the MT52C9040 allows the receiving device to request that data just read from the FIFO to be repeated. When the $(\overline{FL})/\overline{RT}$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may again start reading the data from the beginning of the FIFO ^{t}RTR after $(\overline{FL})/\overline{RT}$ is taken HIGH. The empty, half-full and full flags will be affected as specified for the data volume.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty points, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a flow-through write. Flow-through writes are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a flow-through read can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. Flow-through reads are initiated from the rising edge of $\overline{W}$ and access time measured from the rising edge of $\overline{EF}$.

FIFO

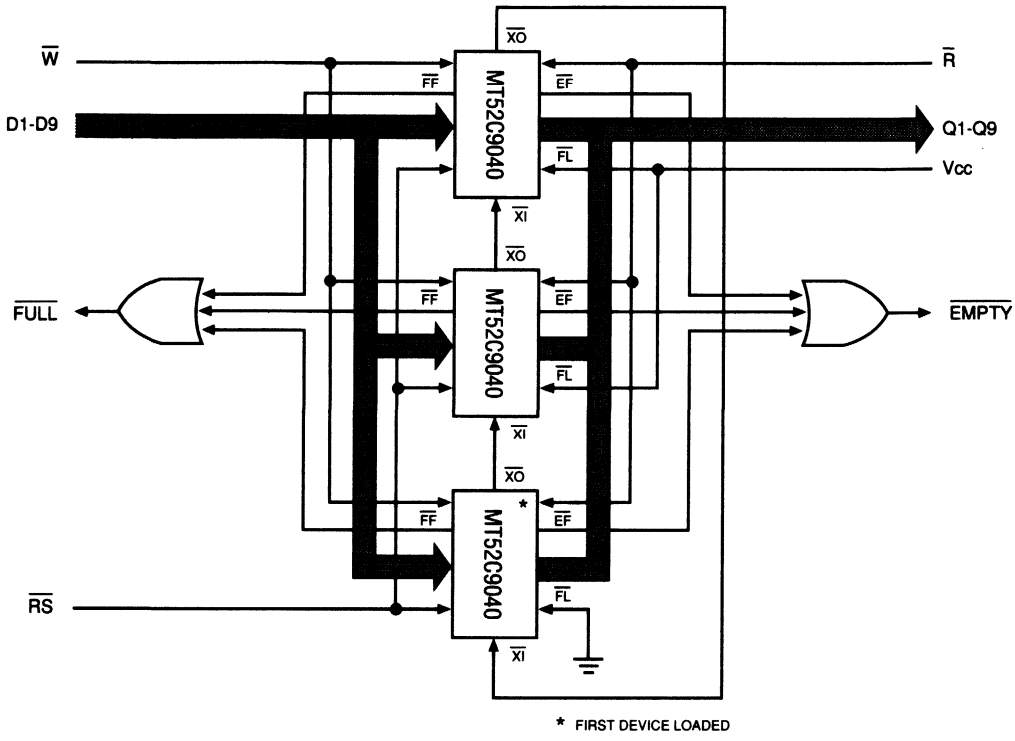


Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the stand alone or groups of expanded depth mode FIFOs. Expanded width operation is acheived by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1), when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9040s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}/(\overline{HF})$ and $\overline{FL}/(\overline{RT})$. Figure 1 illustrates a typical three device expansion. The depth expansion mode is entered during a RESET cycle, by tying the $\overline{XO}/(\overline{HF})$ pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}/(\overline{RT})$ pin grounded. The remaining devices in the chain will have $\overline{FL}/(\overline{RT})$ tied HIGH. During RESET cycle, $\overline{XO}/(\overline{HF})$ of each device goes HIGH, disabling the read and write pointers of every FIFO, except the first load device. When the last physical location of the first device is written, the $\overline{XO}/(\overline{HF})$ pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling the first. The writes will continue to go to the second device until it is full. Then it will "pass" the write pointer to the third device. This process continues until all devices are full. When the entire FIFO array is written, the full condition is signaled by ORing all the $\overline{FF}$ pins, further writes are inhibited. On the last physical read of the first device, its $\overline{XO}/(\overline{HF})$ will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. On the last read, an empty condition is signaled by "ORing" all of the $\overline{EF}$ pins. This inhibits further reads. While in the depth expansion mode, the half-full flag and retransmit functions are not available.

FIFO

TRUTH TABLE

MODE	INPUTS						OUTPUTS				NOTES
	$\overline{W}$	$\overline{R}$	$\overline{RS}$	FL/$\overline{RT}$	$\overline{XI}$	D1-D9	$\overline{EF}$	$\overline{FF}$	$\overline{XO}$/$\overline{HF}$	Q1-Q9	
RESET	H	H	L	X	X	X	L	H	X	X	
WRITE	L	X	H	X	X	Data In	X	H	X	X	1
READ	X	L	H	X	X	X	H	X	X	Data Out	2
EMPTY (LAST READ)	X	H→L	H	X	X	X	H→L	X	X	Data Out	
FULL (LAST WRITE)	H→L	X	H	X	X	Data In	X	H→L	L	X	
HALF-FULL	H→L	X	H	X	X	Data In	X	H	H→L	X	3, 4
RETRANSMIT	H	H	H	L	X	X	H	X	X	X	4

FIFO

NOTES:

1. WRITE operations are independent of READ operations.
2. READ operations are independent of WRITE operations.
3. The half-full location is (4096/2 + 1) or 2049.
4. Functional in stand alone mode only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -0.5V to +7.0V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All inputs	V_{IL}	-0.5	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}$, $\overline{R} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}		100	mA	3
Power Supply Current: Standby	$\overline{W}$, $\overline{R} \ge V_{IH}$, V_{CC} = Max.	I_{SB1}		10	mA	
	$\overline{W}$, $\overline{R} \ge V_{CC}$ - 0.2, V_{CC} = Max. $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}		1	mA	
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I		8	pF	4
Output Capacitance	V_{CC} = 5V	C_O		8	pF	4

FIFO

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C, Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-25		-30		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access Time	t_A		25		30		35	ns	
READ Cycle Time	t_{RC}	35		40		45		ns	
READ Recovery Time	t_{RR}	10		10		10		ns	
Read Pulse Width	t_{RPW}	25		30		35		ns	
Read LOW to low Z	t_{RLZ}	5		5		5		ns	
Read to HIGH to high Z	t_{RHZ}		18		20		20	ns	
Read HIGH to Data Valid	t_{DV}		18		20		20	ns	
WRITE Cycle Time	t_{WC}	35		40		45		ns	
Write Pulse Width	t_{WPW}	25		30		35		ns	
WRITE Recovery Time	t_{WR}	10		10		10		ns	
Write HIGH to LOW Z	t_{WLZ}	5		5		5		ns	5
Data Set-up Time	t_{DS}	15		18		20		ns	
Data Hold Time	t_{DH}	0		0		0		ns	
RESET Cycle Time	t_{RCS}	35		40		45		ns	
Reset Pulse Width	t_{RSP}	25		30		35		ns	6
RESET Recovery Time	t_{RSR}	10		10		10		ns	
Read HIGH to Reset HIGH	t_{RRS}	25		30		35		ns	
Write HIGH to Reset HIGH	t_{WRS}	25		30		35		ns	
RETRANSMIT Cycle Time	t_{RTC}	35		40		45		ns	
Retransmit Pulse Width	t_{RT}	25		30		35		ns	
RETRANSMIT Recovery Time	t_{RTR}	10		10		12		ns	
Retransmit Set-up Time	t_{RTS}	25		30		35		ns	
Reset to $\overline{EF}$ LOW	t_{EFL}		35		40		45	ns	
Reset to $\overline{FF}$ HIGH	t_{FFH}		35		40		45	ns	
Reset to $\overline{HF}$ HIGH	t_{HFH}		35		40		45	ns	
Read LOW to $\overline{EF}$ LOW	t_{REF}		25		30		35	ns	
Read HIGH to $\overline{FF}$ HIGH	t_{RFF}		25		30		35	ns	
Write LOW to $\overline{FF}$ LOW	t_{WFF}		25		30		35	ns	
Write HIGH to $\overline{EF}$ HIGH	t_{WEF}		25		30		35	ns	
Write LOW to $\overline{HF}$ LOW	t_{WHF}		35		40		45	ns	
Read HIGH to $\overline{HF}$ HIGH	t_{RHF}		35		40		45	ns	
Read Pulse after $\overline{EF}$ HIGH	t_{RPE}	25		30		35		ns	5
Write Pulse Width after $\overline{FF}$ HIGH	t_{WPF}	25		30		35		ns	
Read/Write to $\overline{XO}$ LOW	t_{XOL}		25		30		35	ns	
Read/Write to $\overline{XO}$ HIGH	t_{XOH}		25		30		35	ns	
$\overline{XI}$ Pulse Width	t_{XIP}	25		30		35		ns	
$\overline{XI}$ Set-up Time	t_{XIS}	15		15		15		ns	
$\overline{XI}$ Recovery Time	t_{XIR}	10		10		10		ns	

FIFO

NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through data mode only.
6. Pulse widths less than minimum are not allowed.

AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 1

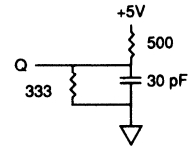
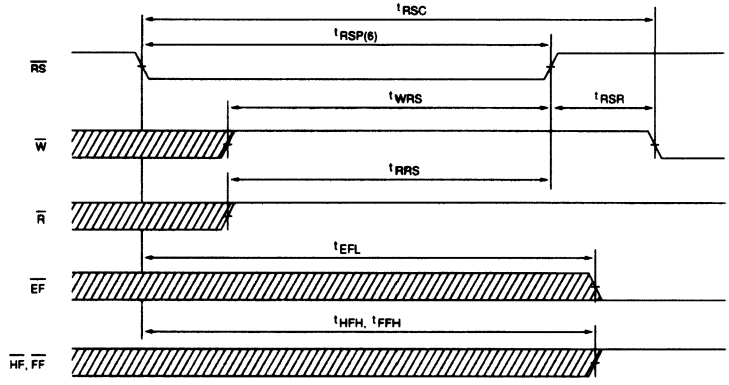
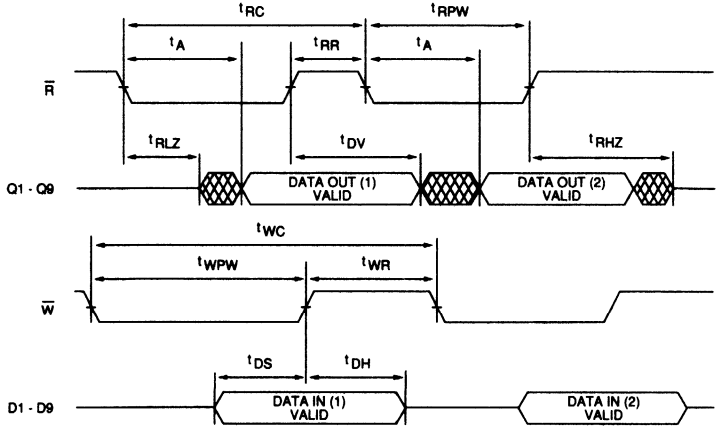


Fig. 1 OUTPUT LOAD EQUIVALENT

RESET



ASYNCHRONOUS READ AND WRITE

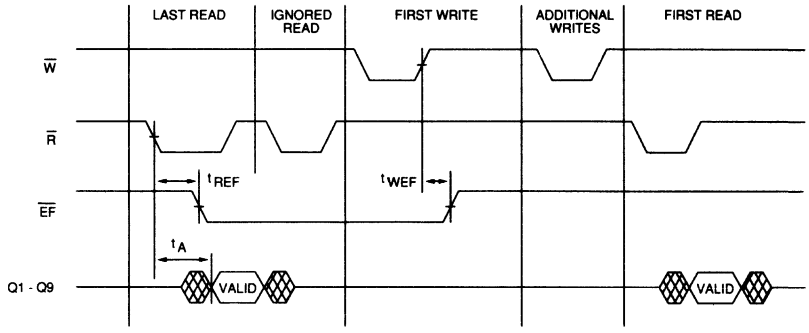


DON'T CARE

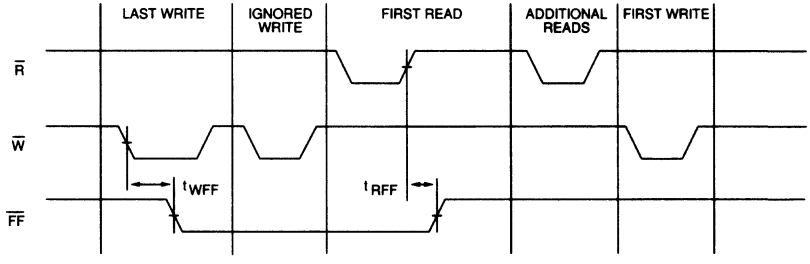
UNDEFINED

FIFO

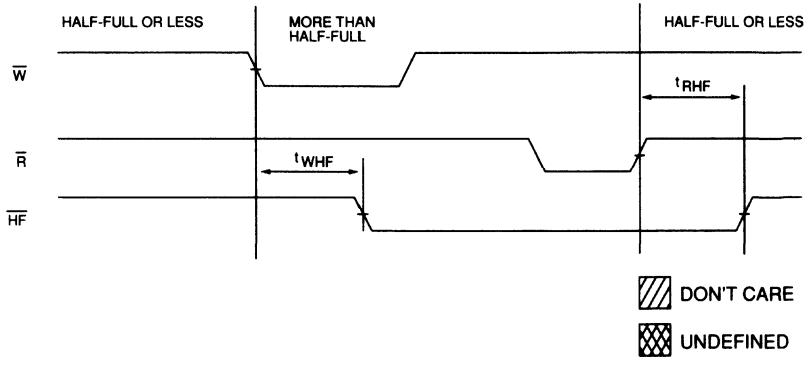
EMPTY FLAG



FULL FLAG

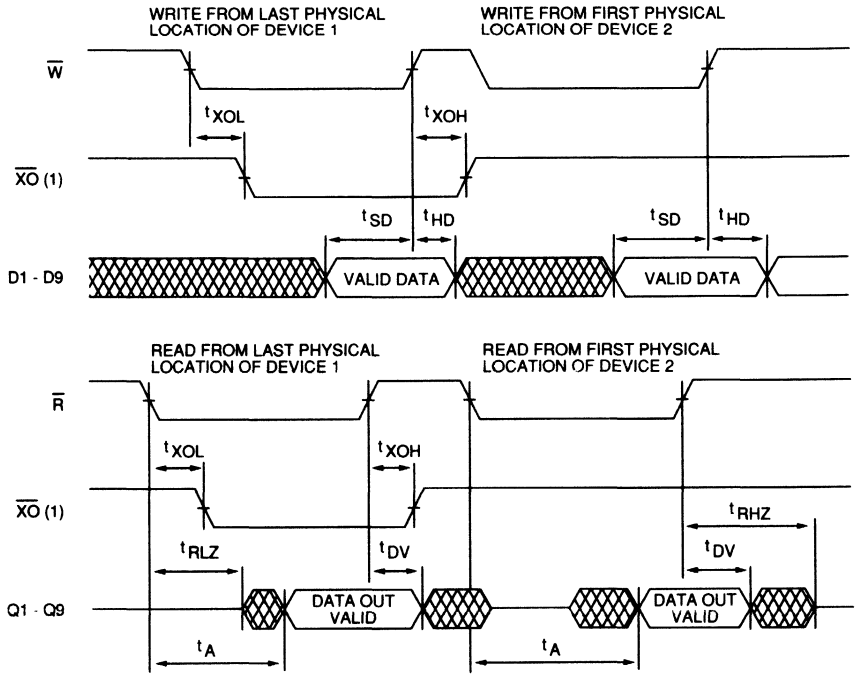


HALF-FULL FLAG



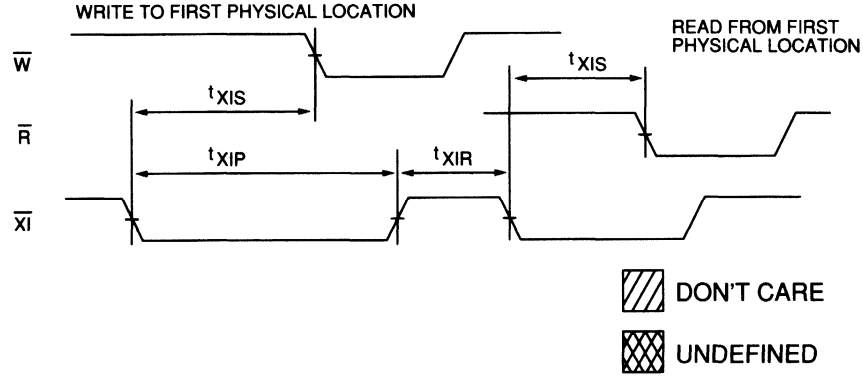
FIFO

EXPANSION MODE ($\overline{XO}$)



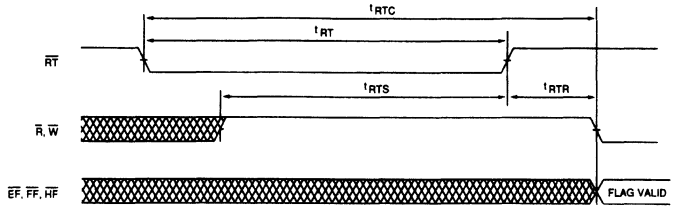
Note 1: $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

EXPANSION MODE ($\overline{XI}$)

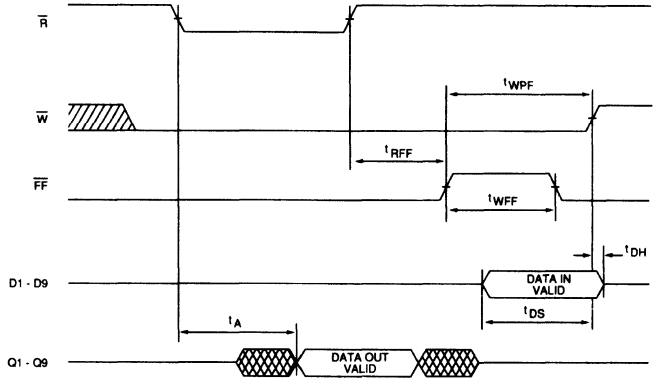


FIFO

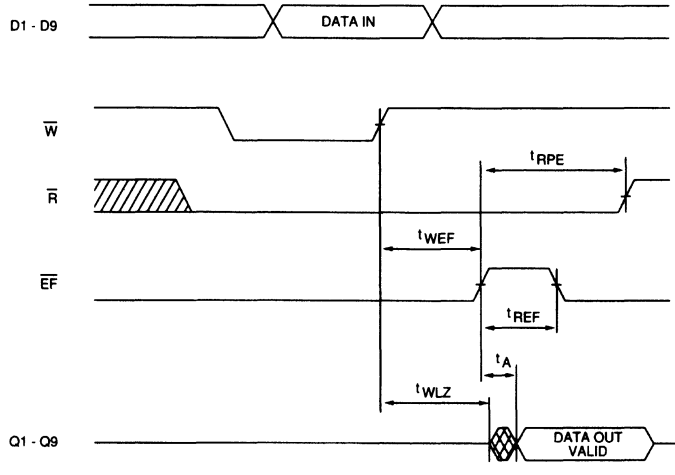
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH



DON'T CARE

UNDEFINED

FIFO

FIFO

4K x 9 FIFO

MAILBOX REGISTER

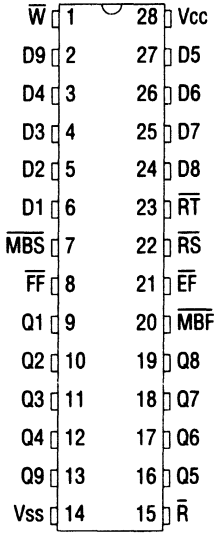
FEATURES

- High speed: 25ns access, 35ns cycle time
- Asynchronous and simultaneous READ and WRITE
- Empty and Full Flags
- Automatic retransmit
- Transistor loads for maximum data integrity
- Low power
- Programmable Mailbox register

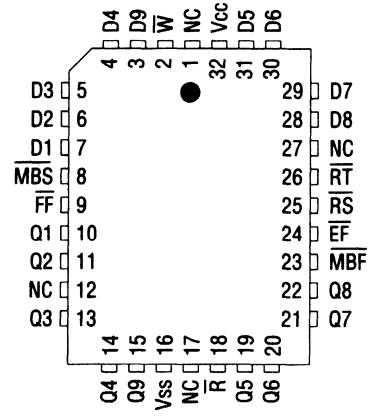
OPTIONS	MARKING
• Timing	
25ns access time	-25
30ns access time	-30
35ns access time	-35
• Packages	
Plastic DIP	None
Ceramic DIP	C
PLCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



GENERAL DESCRIPTION

The Micron FIFO family employs high speed, low power CMOS designs using a true dual-port 6-transistor memory cell with resistive loads. They are fabricated using silicon gate CMOS technology.

There are three major user options that are available separately or in combination: expandable, mailbox register, and variable flags. Expandable FIFOs are designed to be compatible with industry standard devices and have fixed full and empty flags. Mailbox FIFOs have an on-chip programmable register that is used to bypass specific words around the FIFO. Variable flag FIFOs allow the user to program the level of two additional full and empty flags.

All devices operate from a single +5V power supply and all inputs and outputs are TTL compatible.

FIFO

4K x 9 FIFO

VARIABLE FLAGS

FEATURES

- High speed: 25ns access, 35ns cycle time
- Asynchronousand simultaneous READ and WRITE
- Empty and Full Flags
- Automatic retransmit
- Transistor loads for maximum data integrity
- Low power
- Programmable Empty/Full Flags (128 increments)

OPTIONS — MARKING

- Timing

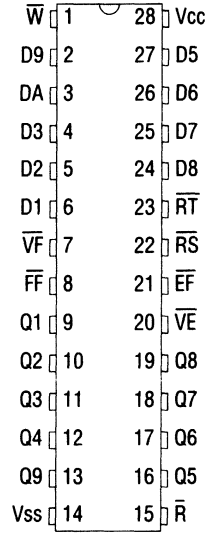
25ns access time	-25
30ns access time	-30
35ns access time	-35

- Packages

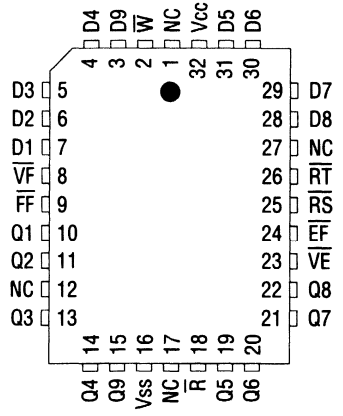
Plastic DIP	None
Ceramic DIP	C
PLCC	EJ
Ceramic LCC	EC

PIN ASSIGNMENT (Top View)

28L DIP



32L/LCC



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Technical Note

Introduction to Mailbox and Variable Flag FIFOs

INTRODUCTION

Micron has introduced two new features to offer the system designer a FIFO solution that will give the highest system performance. Variable flags and mailbox registers will be incorporated on a variety of Micron FIFOs both separately and together, with expandability. An on-chip mailbox register will facilitate high speed, single word data exchange between devices buffered by the FIFO. The variable flag option provides programmable variable empty and full flags. The variable flag option provides improved monitoring of the FIFO capacity to enhance the elasticity of the FIFO buffer. These functions will increase system efficiency through improved data management.

MAILBOX REGISTER

The mailbox register function provides a data path from input to output of the FIFO that is completely separate from the dual-port memory array. It allows one data word to be written "around" the FIFO memory array to a dedicated register that can be selected for output at any time. The mailbox register allows data to bypass the FIFO memory and is available to the receiving device without resetting the FIFO. Information (i.e. bus control handshaking) can be sent asynchronously and independent of the data loaded into the FIFO memory buffer.

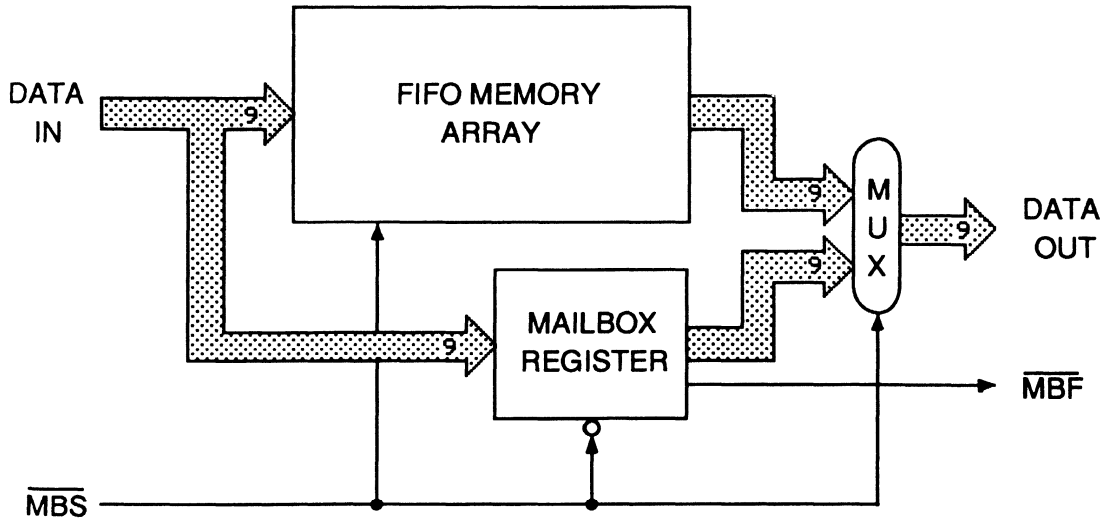


Figure 1. Mailbox FIFO Functional Block Diagram

APPLICATION INFORMATION

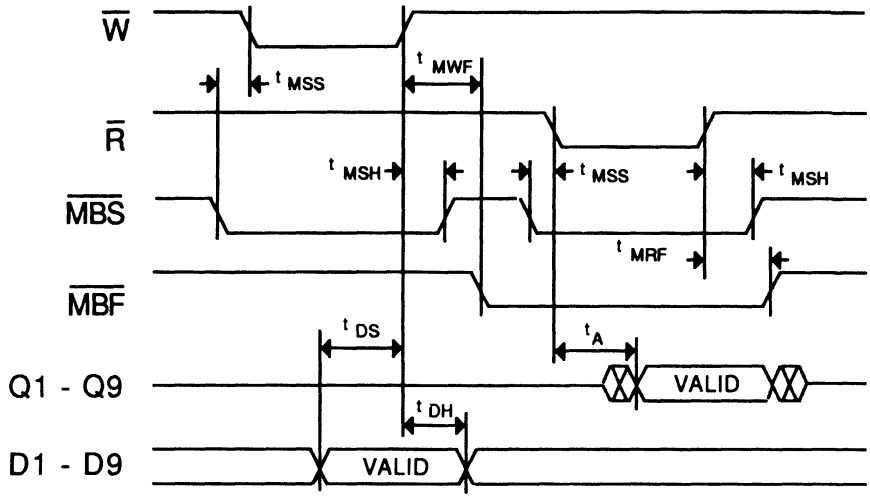


Figure 2. Mailbox Register Timing

Figure 1 illustrates the basic data path in and out of the mailbox equipped FIFO. Detail of the general control lines ($\overline{W}$, $\overline{R}$, etc.) is deleted for simplicity. The mailbox register is loaded via the same D1-D9 input pins as the FIFO memory array and controlled by the same $\overline{R}$ and $\overline{W}$ pins. The WRITE cycle timing is the same as that of a write to the FIFO memory with the addition of the mailbox select ($\overline{MBS}$) pin.

Figure 2 illustrates the write and read timing for the mailbox register. The read timing is the same. The select pin is taken LOW ^{t}MSS before the falling edge of the write strobe ($\overline{W}$) to initiate a MAILBOX WRITE cycle. The combination of a LOW $\overline{MBS}$ pin and an active $\overline{WR}$ or $\overline{RD}$ pin will inhibit a WRITE or READ to the FIFO memory array during a mailbox write or read, respectively.

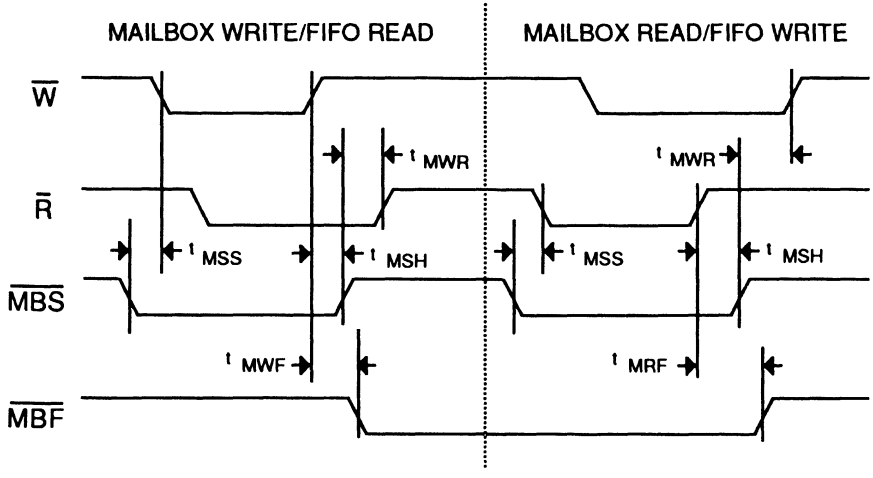


Figure 3. Overlapped Mailbox/FIFO Timing

Data is latched into the mailbox register on the rising edge of $\overline{W}$ and the $\overline{MBS}$ pin is held LOW for ^{t}MSS*. Dedicated control logic for the mailbox register is selected by the $\overline{MBS}$ control signal. This logic plus the standard read and write signals control mailbox READS and WRITES.

To inform the receiving device of valid mailbox data, a mailbox full ($\overline{MBF}$) flag is provided. The $\overline{MBF}$ pin will be asserted (LOW) ^{t}MWF after the rising edge of $\overline{W}$ and will stay LOW until the mailbox register is read. By asserting $\overline{MBF}$ on the rising edge of $\overline{W}$, overlapping of WRITE and READ cycles to the mailbox is automatically inhibited. Further WRITES to the mailbox are inhibited when the mailbox is full.

To initiate a READ cycle, the $\overline{MBS}$ must again be taken LOW ^{t}MSS before a read strobe ($\overline{R}$) falling edge. When $\overline{MBS}$ is LOW during a READ cycle, the mailbox data will be valid at the output pins (Q1-Q9) ^{t}A after the falling edge of $\overline{R}$. The $\overline{MBF}$ signal will go invalid (HIGH) ^{t}MRF after the rising edge of $\overline{R}$. As with writes, this will prohibit overlapping of READS and WRITES since WRITES are inhibited while $\overline{MBF}$ is LOW. A mailbox access can occur coincident with a FIFO access. If the FIFO access is initiated first, no special timing considerations apply. However, if the mailbox access is initiated first, the $\overline{MBS}$ pin must be invalid ^{t}MWR before the rising edge of the FIFO access control signal ($\overline{R}$ or $\overline{W}$), see Figure 3.

VARIABLE FLAGS

The second of the new options provides, in addition to industry standard empty and full flags, two "variable" empty and full flags. The variable flags provide another level of data monitoring capability in addition to the standard full, half-full and empty flags. Their programmability allows the system designer to tailor full and empty conditions to the system performance requirements. This will result in a data rate buffer optimized to the system design. These flags are programmed with an offset from empty and full.

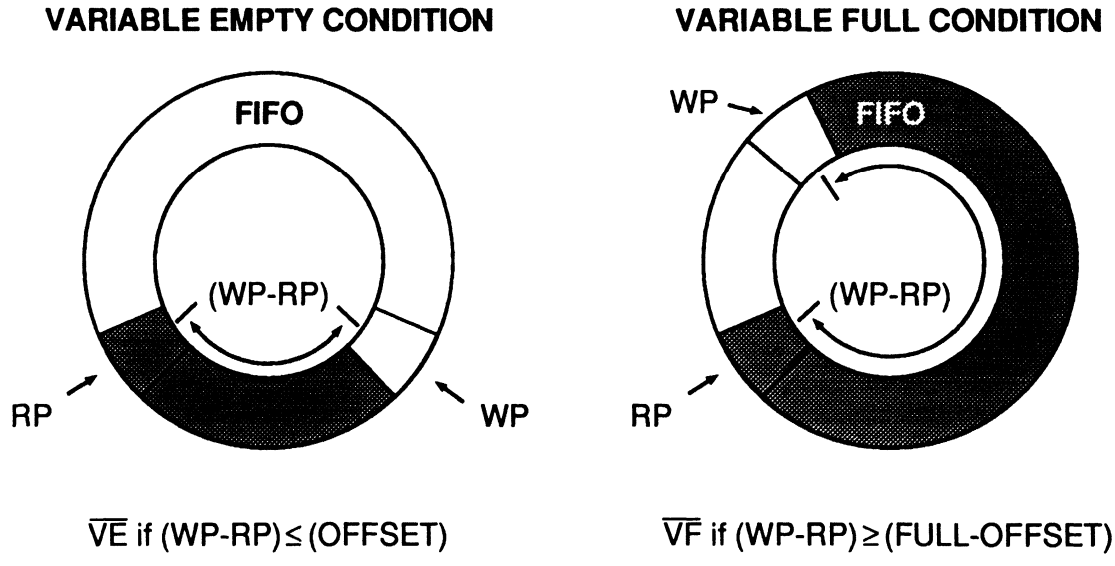


Figure 4. Variable Flag Regions

APPLICATION INFORMATION

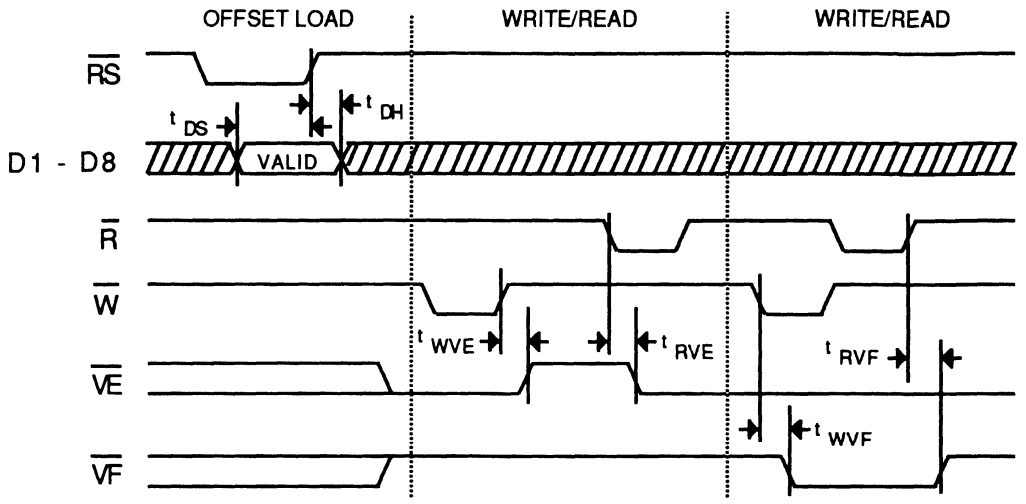


Figure 5. Variable Flag Timing

The offset is programmed into the FIFO via the D1-D8 pins during a RESET cycle. On the rising edge of $\overline{RS}$, the levels of the D1-D8 pins are latched into the offset register, see Figure 4. The D1-D7 pins define the offset value (0-127) and the D8 pin selects the programming mode. The mode pin (D8) will select the default offset value of 4 when LOW or the binary offset value of D1-D7 when HIGH. The mode pin allows the offset to be set by one data pin if the variable offset is not needed. Because one data byte is loaded on the L→H transition of $\overline{RS}$, the variable empty ($\overline{VE}$) and variable full ($\overline{VF}$) flags are set to the same offset. Figure 5 illustrates the programmable conditons for the flags.

Valid data is indicated by the (▒) shaded area. Both flags are simultaneously set to trigger anywhere in a region 127 or less locations from empty for the $\overline{VE}$ flag and 127 or less locations from full for the $\overline{VF}$ flag. This region is determined by the relative difference between the write pointer (WP) and the read pointer (RP). The $\overline{VE}$ flag is asserted LOW when the relative address difference of the WP and RP is equal or less than the programmed offset value. Likewise, the $\overline{VF}$ flag is asserted (LOW) when the relative difference of the WP and RP is equal or greater than the full condition less the offset.

SUMMARY

As system speeds continue to increase, the role of the hardware FIFO buffer is likely to increase. The mailbox register and variable flag options will provide more flexibility through better data management and an increase in overall system speeds. The Micron FIFO family includes these functions as well as the industry standard options on a variety of device types and densities.

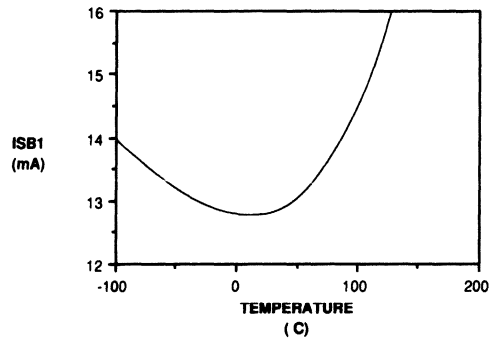
Technical Note

256K FAST SRAM Typical Operating Curves

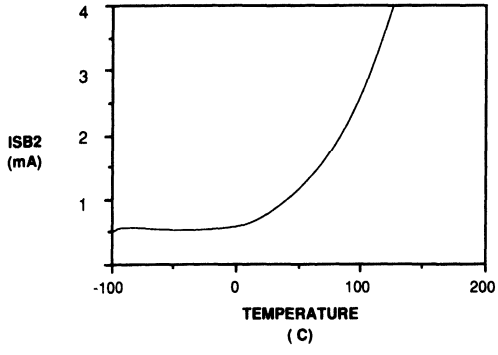
INTRODUCTION

These curves represent the typical operating characteristics of a 25ns SRAM. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets in the SRAM section of this data book.

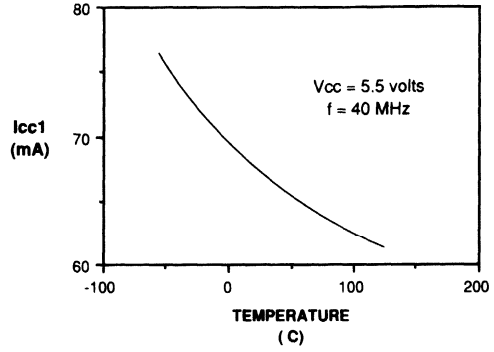
ISB1 vs. TEMPERATURE



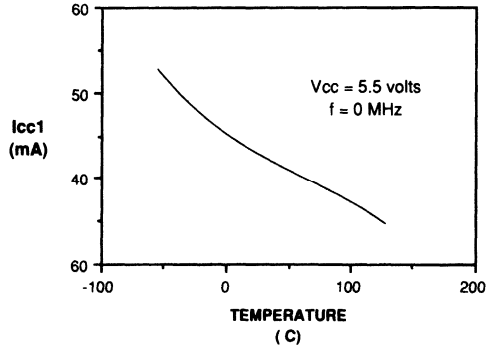
ISB2 vs. TEMPERATURE



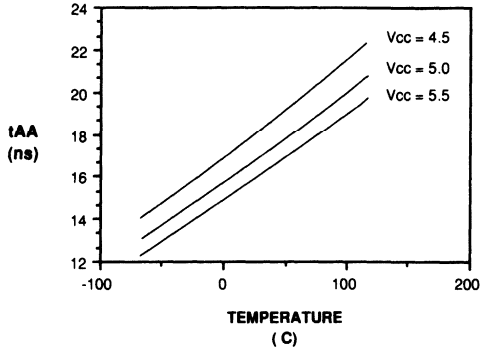
Icc1 vs. TEMPERATURE



Icc1 vs. TEMPERATURE



tAA vs. TEMPERATURE



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MICRON

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MICRON TECHNOLOGY, DEFENSE ELECTRONICS DIVISION

Micron Technology, Inc. is a Pacific Northwest company with manufacturing facilities located in Boise, Idaho, U.S.A. We are now the only U.S.-based memory manufacturer of Fast static RAMs and dynamic RAMs maintaining both the CMOS and NMOS Joint Army Navy (JAN) certification. Micron has maintained the Mil-Std-38510 certification status on our NMOS product line since 1986. We achieved CMOS JAN certification in March of 1989 becoming the only supplier of military SRAMs, video RAMs and DRAMs as an on-shore JAN-certified facility.

Current assembly package capabilities include ceramic DIP, LCC and flat pack. One hundred percent of our military assembly is performed in Boise, Idaho. Military products are tested on MegaTest Q2/52 and Teradyne J937 test stations as well as in intelligent burn-in ovens which were designed and manufactured by Micron exclusively for memory burn-in — model name AMBYX ™.

As a supplier to the defense electronics industry, Micron offers a broad line of military memory products including: 256K SRAMs in 32Kx8, 64Kx4 and 256Kx1 configurations compatible with military industry standard pin-outs and offered in 25 nanoseconds (ns) through 45ns access speeds; 64K SRAMs in 8Kx8, 16Kx4 and 64Kx1 configurations compatible with military standard pin-outs with speeds available in 20ns through 35ns; and 16K SRAMs available in 2Kx8 offered in 20ns through 35ns access speeds. All SRAMs are processed as CMOS products and are packaged in 300 mil dual-in-line packages (DIP) and leadless chip carriers (LCC). Micron's line of DRAMs, SRAMs and VRAMs are available meeting Defense Electronic Supply Center (DESC) Standard Military Drawings and Mil-Std-883 Class B Rev. C. We also have next generation devices under development including the 4-Meg DRAM, 1-Meg VRAM and 1-Meg SRAM.

MILITARY PRODUCTS - FUTURE REQUIREMENTS

In the area of radiation tolerance, Micron believes most contracts will require a defined level of radiation immunity. In response, we are currently characterizing SRAM and DRAM CMOS products through total dose, dose rate, single event upset and latch up.

We believe the defense industry is heading toward higher-density memory, faster speeds and more sophisticated "memory solutions." This may include more system functionality on chip or non- standard packaging concepts specially designed for cooling or higher density than currently available from individual components.

Micron further believes that the defense memory industry will move towards tighter processing geometries, new package concepts and more advanced hardware development through an interface of the component designer and the systems design engineer. Our processes, technology and marketing resources are poised to support such requirements.

MICRON MIL-STD 883C COMPLIANT PRODUCT ASSURANCE FLOW

Description of Requirements and Screens	Methods and Test Conditions	Comment
General MIL-M-38510		
1. MIL-STD 883, Class B, Rev. C	Establish and implement a product assurance program plan	
2. Certification	Manufacturer's QA survey	Self audit
3. Traceability	Traceable to wafer production lot	Computer lot history records
4. Country of Origin (Not required for 883C)	N/A	Devices manufactured, assembled and tested in Boise, Idaho USA
MIL-STD 883 Fabrication		
5. Incoming Materials	Receiving inspection. Vendor Audits	
6. Wafer Fabrication	Method 2018, SEM Monitors	Sample
7. Assembly	Process Monitors	Sample
	Statistical Process Controls	Sample
MIL-STD 883, Class B, Rev. C, Method 5004 Screening		
8. Internal Visual	Method 2010, cond. B	100%
9. Temperature Cycle	Method 1010, cond. C	100%
10. Constant Acceleration	Method 2001, cond. E	100%
11. Hermeticity		
A. Fine Leak	Method 1014, cond. A	100%
B. Gross Leak	Method 1014, cond. C	100%
12. Initial Electricals	Manufacturer's documented data sheet	100%
13. Burn-in	Method 1015	100%
14. Final Electrical Post Burn-in Test	Method 5004, Class B, paragraph 3.1.15, 5% PDA	100%
15. Marking	Method 2015	100%
16. External Visual	Method 2009	100%
17. Quality Conformance Inspection	Method 5005 in-line Class B	Groups A, B, C, D
18. Pack/Ship	Includes C of C, with QCI data (attributes only)	100%
Quality Conformance Inspection per Method 5005 (attributes data only)		
19. Group A	Manufacturer's documented data sheet	Each inspection lot/sublot
20. Group B	Package functional and construction tests	Each inspection lot/sublot
21. Group C	Die related	Each microcircuit group, every 52 weeks
22. Group D	Package related test	Each package type, every 52 weeks

DRAMs

Description	Speed	Micron Part Number	SMD Part Number	JAN Part Number
64K X 1 CDIP	120ns	MT4264C-12 883C		
	150ns	MT4264C-15 883C	8201004EC	
			8201006EC	
	200ns	MT4264C-20 883C	8201005EC	
			8201007EC	
64K X 1 CLCC	120ns	MT4264EC-12 883C		
	150ns	MT4264EC-15 883C	8201004-06ZA	
	200ns	MT4264EC-20 883C	8201006-07ZA	
64K X 1 Flat Pack	120ns	MT4264F-12 883C		
	150ns	MT4264F-15 883C		
	200ns	MT4264F-20 883C		
256K X 1 CDIP	120ns	MT1259C-12 883C	8515203EC	M38510/24601-03BEC
	150ns	MT1259C-15 883C	8515201EC	M38510/24602-04BEC
	200ns	MT1259C-20 883C	8515202EC	
256K X 1 CLCC	120ns	MT1259EC-12 883C	8515203XA	M38510/24601-03BX
	150ns	MT1259EC-15 883C	8515201XA	M38510/24602-04BX
	200ns	MT1259EC-20 883C	8515202XA	
64K X 4 CDIP	100ns	MT4067C-10 883C	8767604VC	
	120ns	MT4067C-12 883C	8767601VC	
	150ns	MT4067C-15 883C	8767602VC	
	200ns	MT4067C-20 883C	8767603VC	
64K X 4 CLCC	100ns	MT4067EC-10 883C	8767604XA	
	120ns	MT4067EC-12 883C	8767601XA	
	150ns	MT4067EC-15 883C	8767602XA	
	200ns	MT4067EC-20 883C	8767603XA	
1MB X 1 CDIP	100ns	MT4C1024C-10 883C	AVAILABLE FY'89	AVAILABLE FY'89
	120ns	MT4C1024C-12 883C		
	150ns	MT4C1024C-15 883C		
1MB X 1 CLCC	100ns	MT4C1024EC-10 883C	AVAILABLE FY'89	AVAILABLE FY'89
	120ns	MT4C1024EC-12 883C		
	150ns	MT4C1024EC-15 883C		
1MB X 1 Flat Pack	100ns	MT4C1024F-10 883C	AVAILABLE FY'89	AVAILABLE FY'89
	120ns	MT4C1024F-12 883C		
	150ns	MT4C1024F-15 883C		

SRAMs

Description	Speed	Micron Part Number	SMD Part Number	JAN Part Number
256K X 1 CDIP	25ns	MT5C2561C-25(L) 883C	8872505LC	M38510/293
	35ns	MT5C2561C-30(L) 883C	8872501LC	Call Factory
	45ns	MT5C2561C-45 883C	8872502LC	AVAILABLE FY'89
256K X 1 CLCC	25ns	MT5C2561EC-25(L) 883C	8872505XA	
	35ns	MT5C2561EC-30(L) 883C	8872501XA	
	45ns	MT5C2561EC-45 883C	8872502XA	
256K X 1 Flat Pack	25ns	MT5C2561F-25(L) 883C	TBD	M38510/293
	35ns	MT5C2561F-30(L) 883C		
	45ns	MT5C2561F-45(L) 883C	AVAILABLE FY'89,	call factory
64K X 4 CDIP	25ns	MT5C2564C-25(L) 883C		
	35ns	MT5C2564C-30(L) 883C	8868101LC	
	45ns	MT5C2564C-45 883C	8868101LC	
64K X 4 CLCC	25ns	MT5C2564EC-25(L) 883C		
	35ns	MT5C2564EC-30(L) 883C	8868101XA	
	45ns	MT5C2564EC-45 883C	8868101XA	
64K X 4 Flat Pack	25ns	MT5C2564F-25(L) 883C	TBD	
	35ns	MT5C2564F-30(L) 883C		
	45ns	MT5C2564F-45(L) 883C	AVAILABLE FY'89	
32K X 8 CDIP	25ns	MT5C2568C-25(L) 883C		
300 MIL	35ns	MT5C2568C-30(L) 883C		
	45ns	MT5C2568C-45 883C	8866204XC	
32K X 8 CDIP	25ns	MT5C2568CW-25(L) 883C		
600 MIL	35ns	MT5C2568CW-30(L) 883C		
	45ns	MT5C2568CW-45(L) 883C	8866204XC	
32K X 8 CLCC	25ns	MT5C2568EC-25(L) 883C		
28 PIN	35ns	MT5C2568EC-30(L) 883C		
	45ns	MT5C2568EC-45(L) 883C		
32K X 8 CLCC	25ns	MT5C2568ECW-25(L) 883C		
32 PIN	35ns	MT5C2568ECW-30(L) 883C		
	45ns	MT5C2568ECW-45(L) 883C	8866204YA	
32K X 8 Flat Pack	25ns	MT5C2568F-25(L) 883C	TBD	
	35ns	MT5C2568F-30(L) 883C		
	45ns	MT5C2568F-45(L) 883C		
64K X 1 CDIP	20ns	MT5C6401C-20(L) 883C	Note 1	
	25ns	MT5C6401C-25(L) 883C		
	30ns	MT5C6401C-30(L) 883C		
	35ns	MT5C6401C-35(L) 883C		

(L): Optional low volt data retention available on all parts with (L) indentifier.

Note 1: The current SMD are written for the slower grade devices, Micron has submitted new drawings to DESC for faster devices.

SRAMs cont.

Description	Speed	Micron Part Number	SMD Part Number	JAN Part Number
64K X 1 CLCC	20ns	MT5C6401EC-20(L) 883C	Note 1	
	25ns	MT5C6401EC-25(L) 883C		
	30ns	MT5C6401EC-30(L) 883C		
	35ns	MT5C6401EC-35(L) 883C		
16K X 4 CDIP	20ns	MT5C6404C-20(L) 883C	Note 1	
	25ns	MT5C6404C-25(L) 883C		
	30ns	MT5C6404C-30(L) 883C		
	35ns	MT5C6404C-35(L) 883C		
16K X 4 CLCC	20ns	MT5C6404EC-20(L) 883C	Note 1	
	25ns	MT5C6404EC-25(L) 883C		
	30ns	MT5C6404EC-30(L) 883C		
	35ns	MT5C6404EC-35(L) 883C		
8K X 8 CDIP 300 MIL	20ns	MT5C6408C-20(L) 883C	Note 1	
	25ns	MT5C6408C-25(L) 883C		
	30ns	MT5C6408C-30(L) 883C		
	35ns	MT5C6408C-35(L) 883C		
8K X 8 CDIP 600 MIL	20ns	MT5C6408CW-20(L) 883C	Note 1	
	25ns	MT5C6408CW-25(L) 883C		
	30ns	MT5C6408CW-30(L) 883C		
	35ns	MT5C6408CW-35(L) 883C		
8K X 8 CLCC 28 PIN	20ns	MT5C6408EC-20(L) 883C	Note 1	
	25ns	MT5C6408EC-25(L) 883C		
	30ns	MT5C6408EC-30(L) 883C		
	35ns	MT5C6408EC-35(L) 883C		
8K X 8 CLCC 32 PIN	25ns	MT5C6408EC-25(L) 883C		
	35ns	MT5C6408EC-35(L) 883C		
2K X 8 CDIP	20ns	MT5C1608C-20(L) 883C	Note 1	
	25ns	MT5C1608C-25(L) 883C		
	30ns	MT5C1608C-30(L) 883C		
	35ns	MT5C1608C-35(L) 883C		
2K X 8 CLCC	20ns	MT5C1608EC-20(L) 883C	Note 1	
	25ns	MT5C1608EC-25(L) 883C		
	30ns	MT5C1608EC-30(L) 883C		
	35ns	MT5C1608EC-35(L) 883C		

(L): Optional low volt data retention available on all parts with (L) indentifier

Note 1: The current SMD are written for the slower grade devices, Micron has submitted new drawings to DESC for faster devices.

VRAMs

Description	Speed	Micron Part Number	SMD Part Number	JAN Part Number
64K X 4 CDIP	100ns	MT42C4064C-10 883C	TBD	
	120ns	MT42C4064C-12 883C		
	150ns	MT42C4064C-15 883C		
64K X 4 CDIP	120ns	MT42C4064EC-10 883C	TBD	
	150ns	MT42C4064EC-12 883C		
	200ns	MT42C4064EC-15 883C		

DYNAMIC RAMs 1

DYNAMIC RAM MODULES 2

MULTIPORT DYNAMIC RAMs 3

STATIC RAMs 4

STATIC RAM MODULES 5

CACHE DATA RAMs 6

FIFO MEMORIES 7

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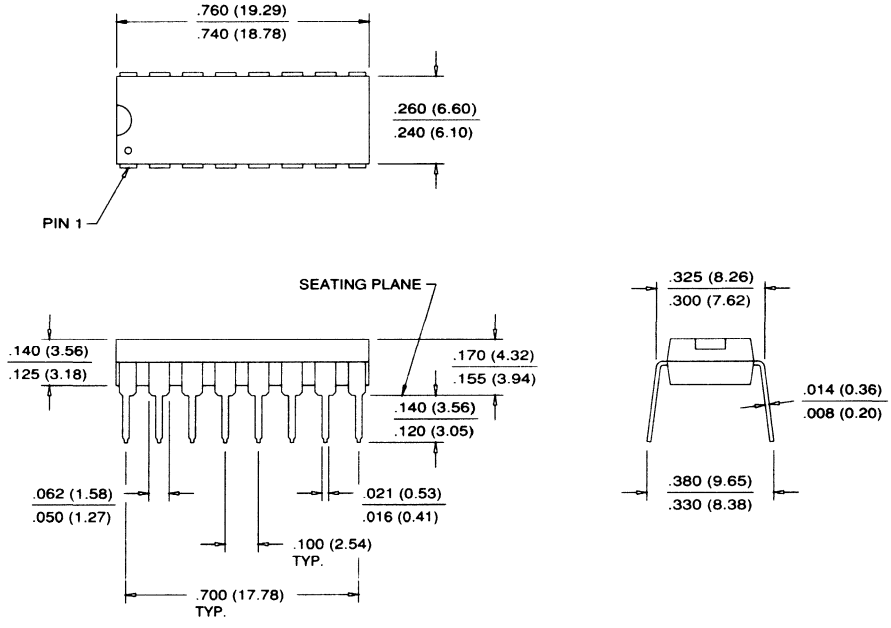
PACKAGE INFORMATION 10

SALES INFORMATION 11

PACKAGE TYPE	PIN COUNT	PAGE
PLASTIC DIP	16	10-3
	18	10-4
	20	10-5
	22	10-6
	24	10-7
	28	10-8
CERAMIC DIP	16	10-9
	18	10-10
	20	10-11
	22	10-12
	24	10-13
	28	10-14
PLASTIC ZIP	16	10-16
	20	10-16
	24	10-17
	28	10-17
PLCC	18	10-18
	52	10-18
PLASTIC SOJ	20	10-19
	24	10-19
	28	10-20
CERAMIC LCC	18	10-21
	20	10-22
	22	10-23
	28	10-24
	32	10-25
FLAT PACK	16	10-26
	20	10-26
	28	10-27
MODULE SIP	22	10-28
	24	10-28
	30	10-29
MODULE SIMM	30	10-30
	72	10-34
MODULE DIP	32	10-36
	40	10-36

16-PIN PLASTIC DIP

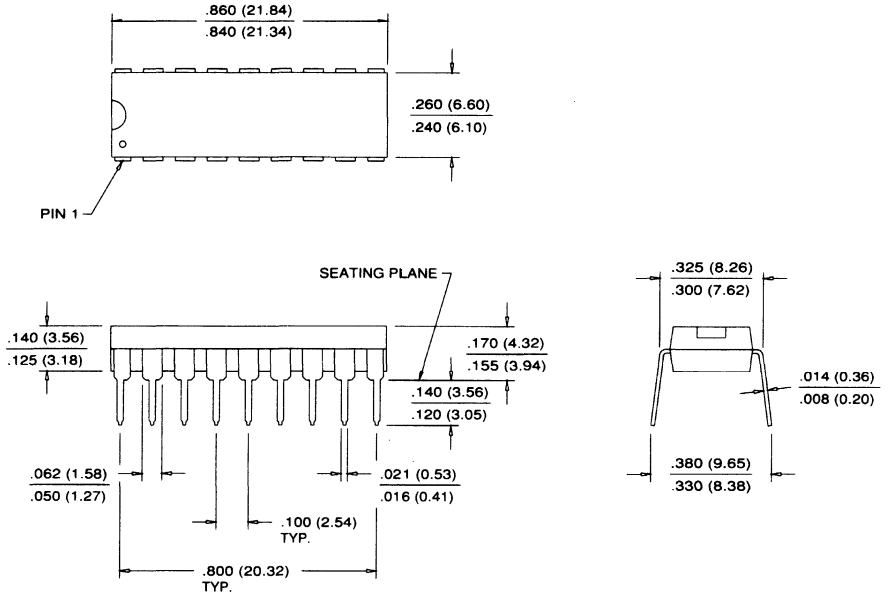
PA



All dimensions in inches (millimeters) $\frac{\text{Max}}{\text{Min}}$ or typical where noted.

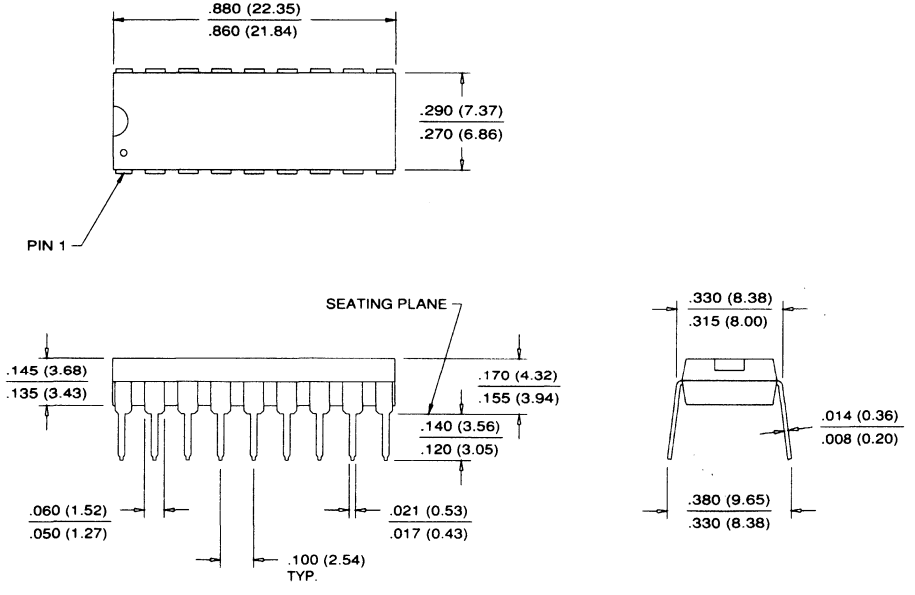
18-PIN PLASTIC DIP

PB



18-PIN PLASTIC DIP

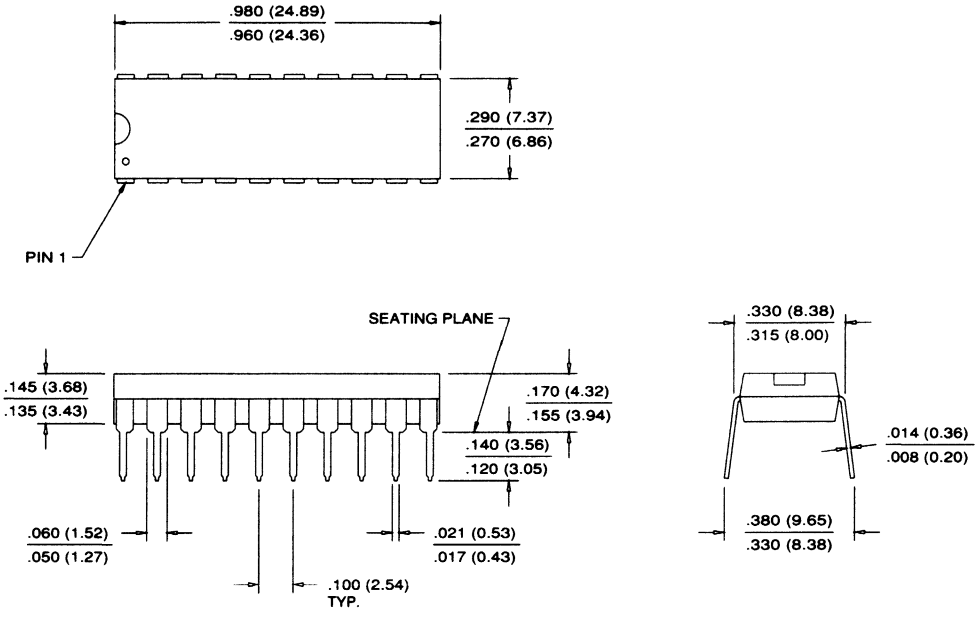
PC



PACKAGE INFORMATION

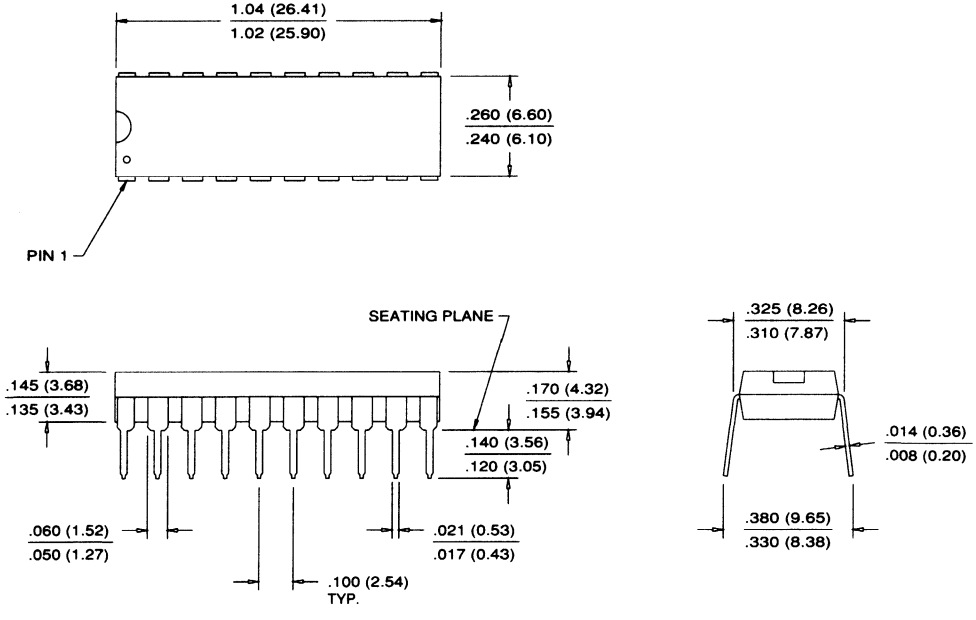
20-PIN PLASTIC DIP

PD



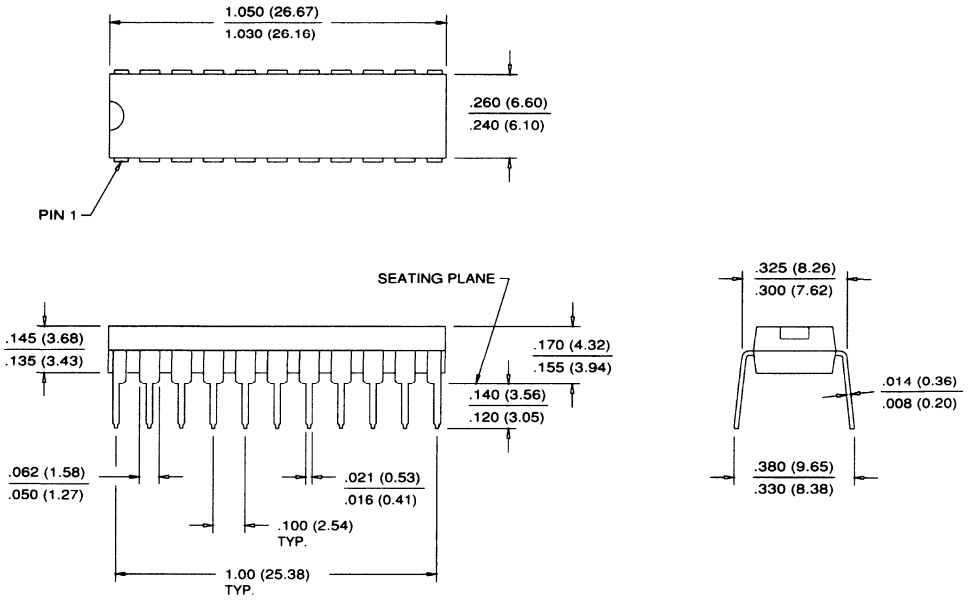
20-PIN PLASTIC DIP

PE



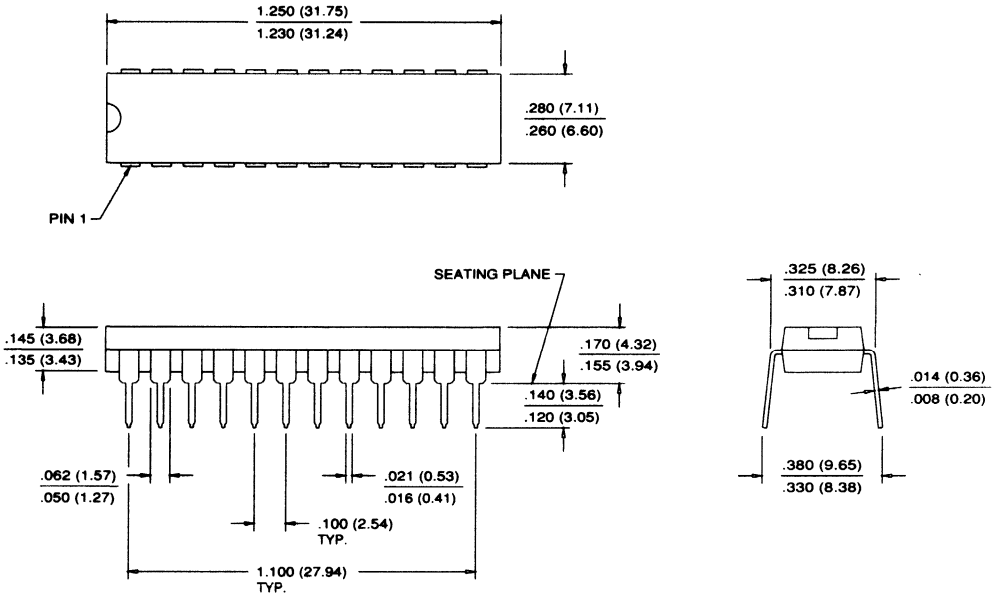
22-PIN PLASTIC DIP

PF



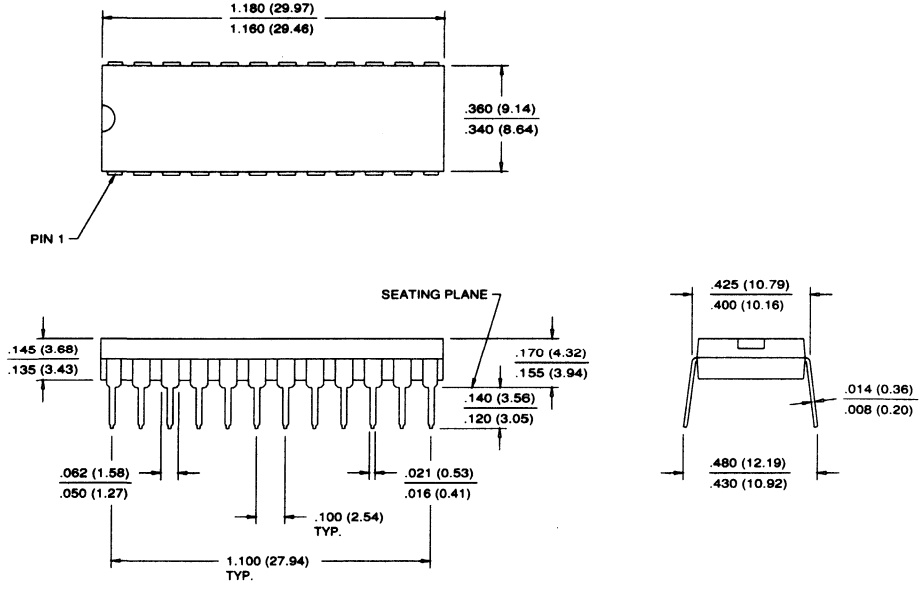
24-PIN PLASTIC DIP

PG



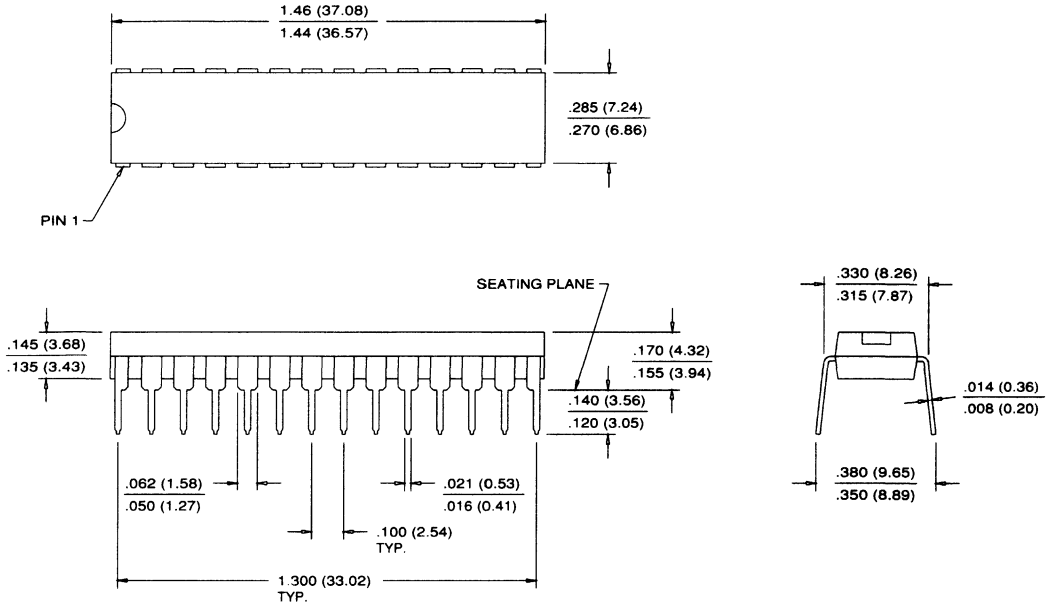
24-PIN PLASTIC DIP

PH



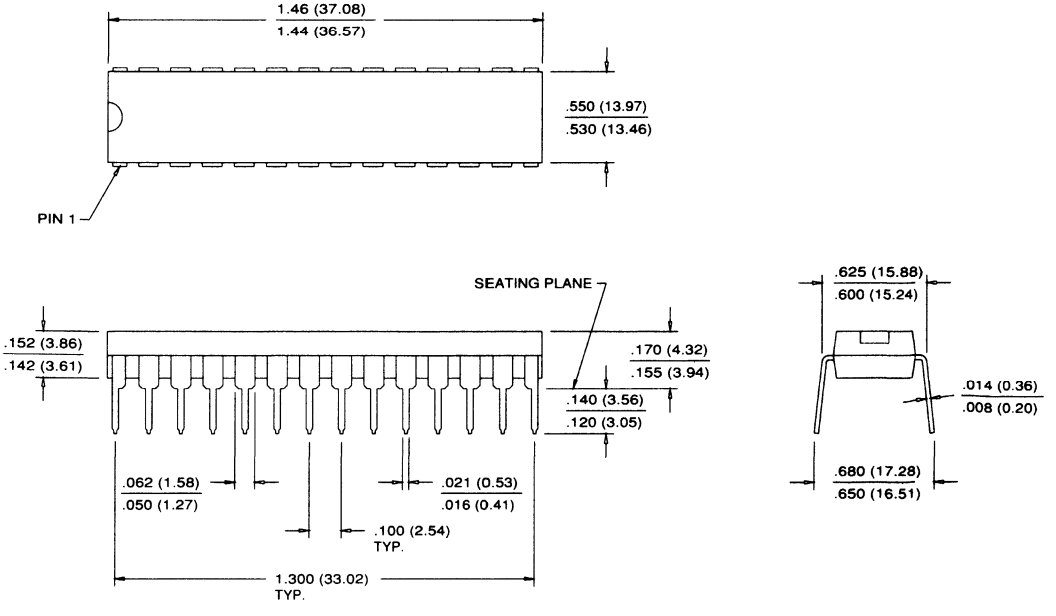
28-PIN PLASTIC DIP

PJ



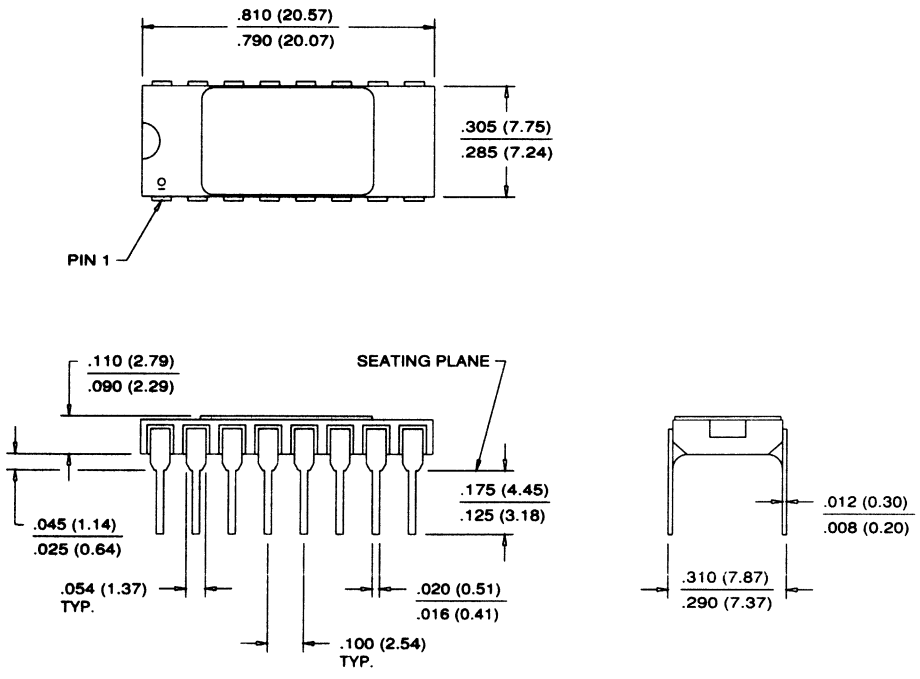
28-PIN PLASTIC DIP

PK



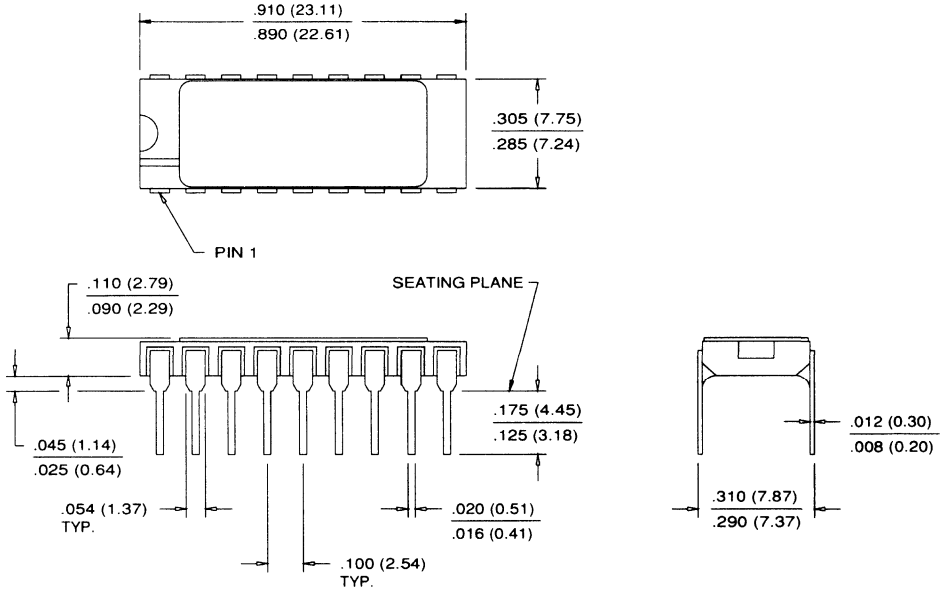
16-PIN CERAMIC DIP

CA



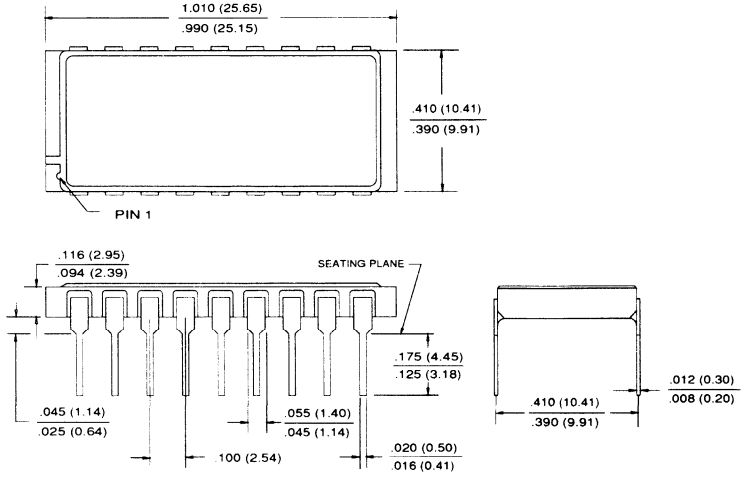
18-PIN CERAMIC DIP

CB



18-PIN CERAMIC DIP

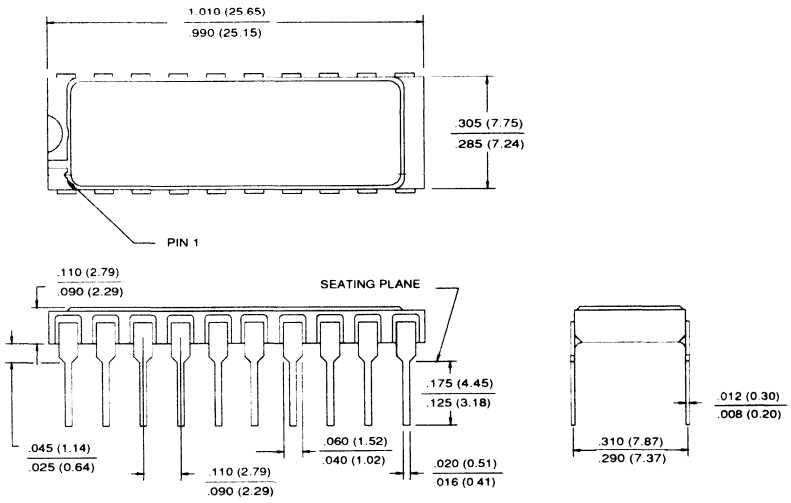
CC



PACKAGE INFORMATION

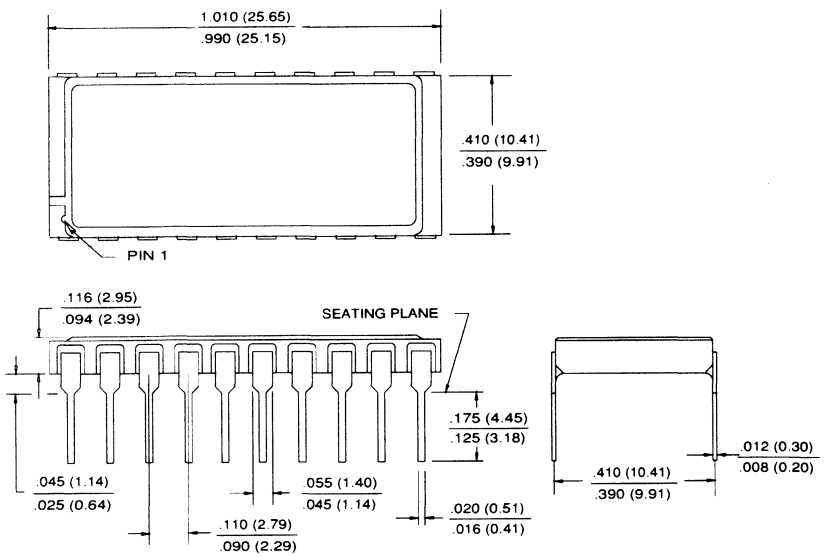
20-PIN CERAMIC DIP

CD



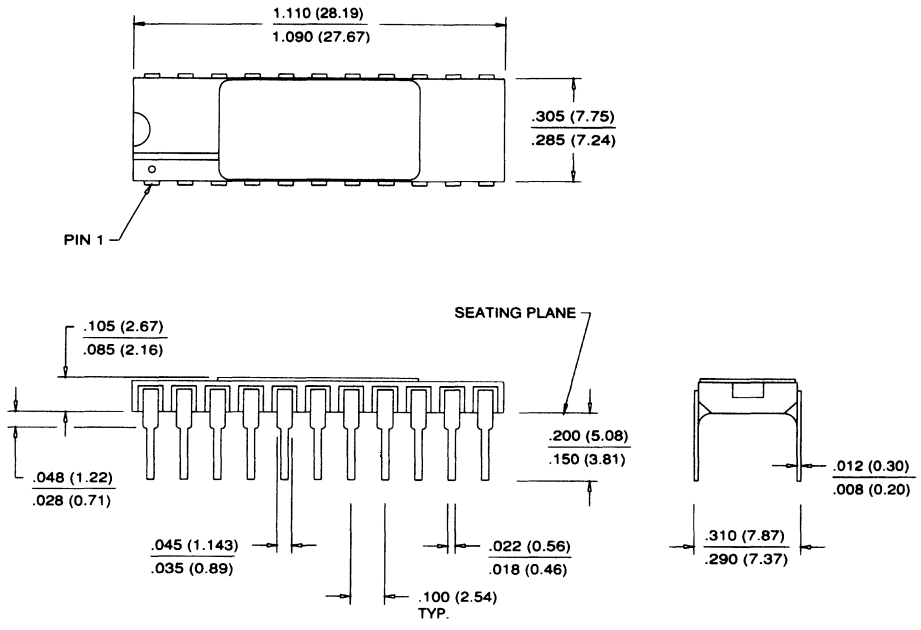
20-PIN CERAMIC DIP

CE



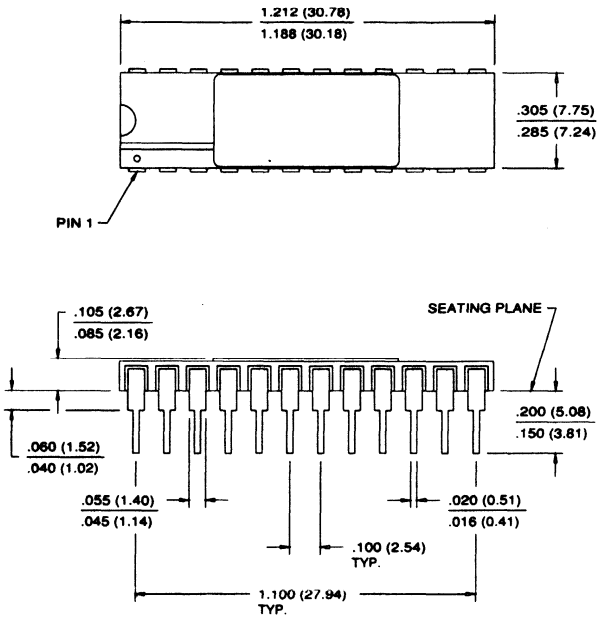
22-PIN CERAMIC DIP

CF



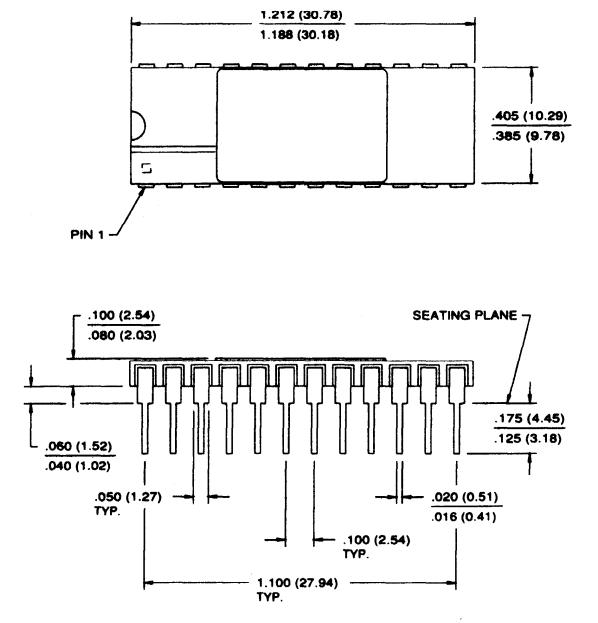
24-PIN CERAMIC DIP

CG



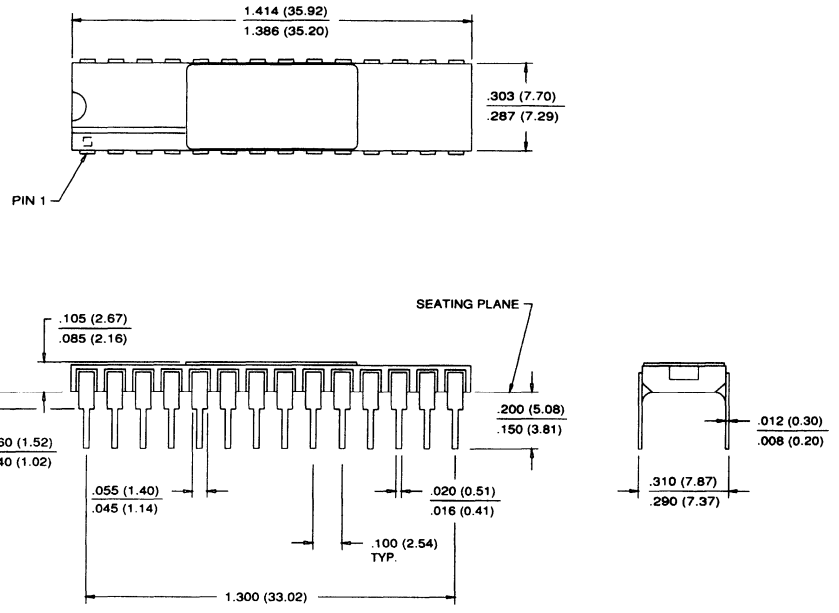
24-PIN CERAMIC DIP

CH



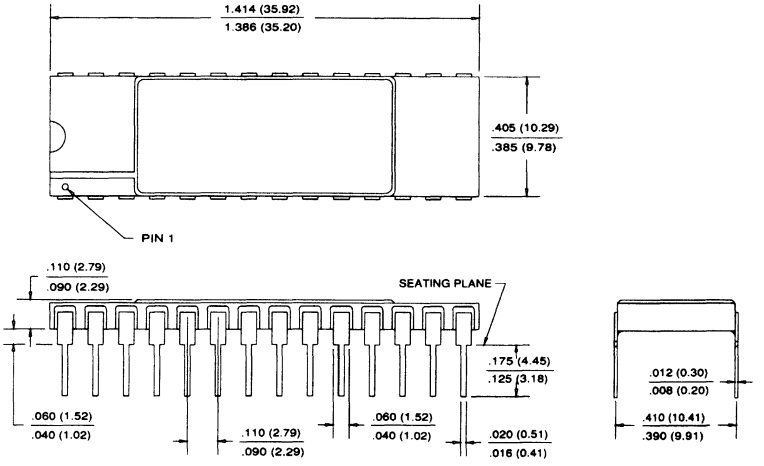
28-PIN CERAMIC DIP

CI



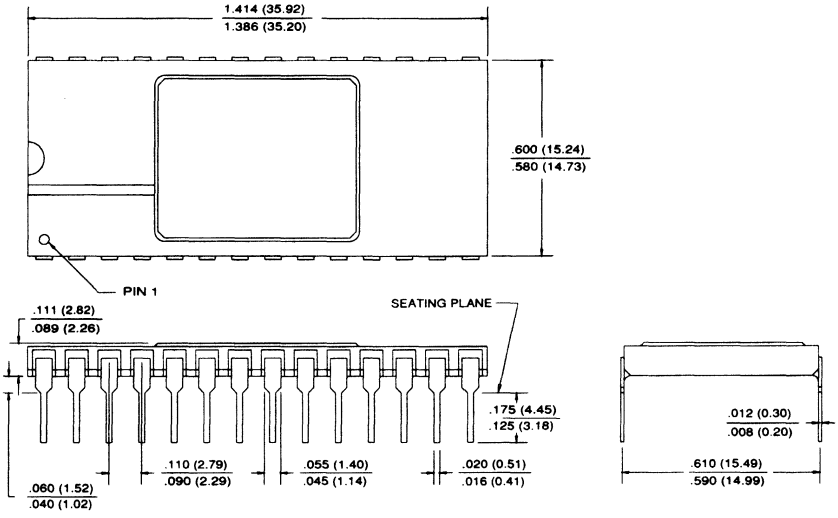
28-PIN CERAMIC DIP

CJ



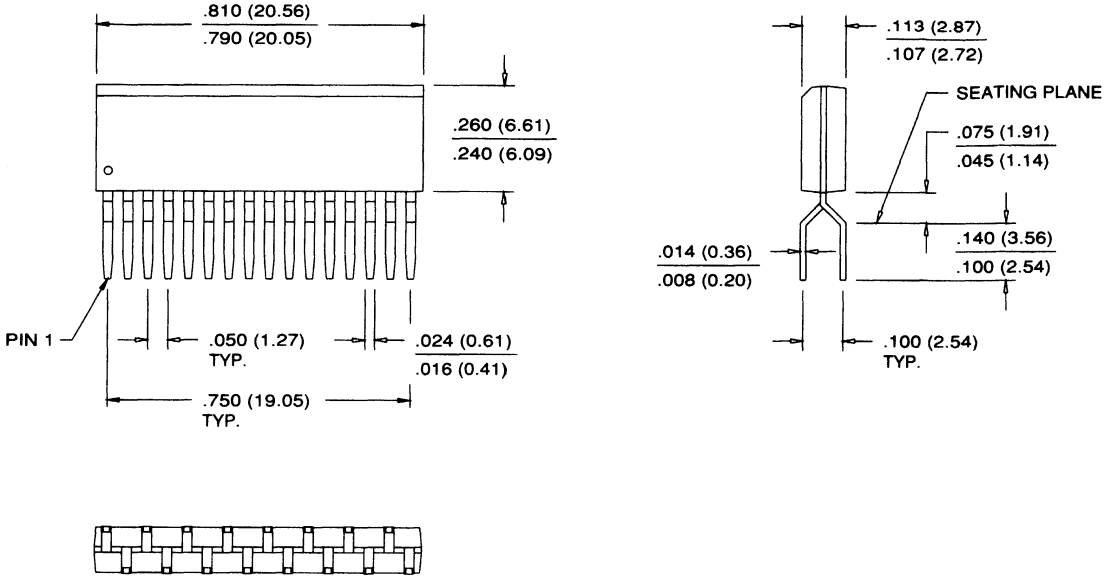
28-PIN CERAMIC DIP

CK



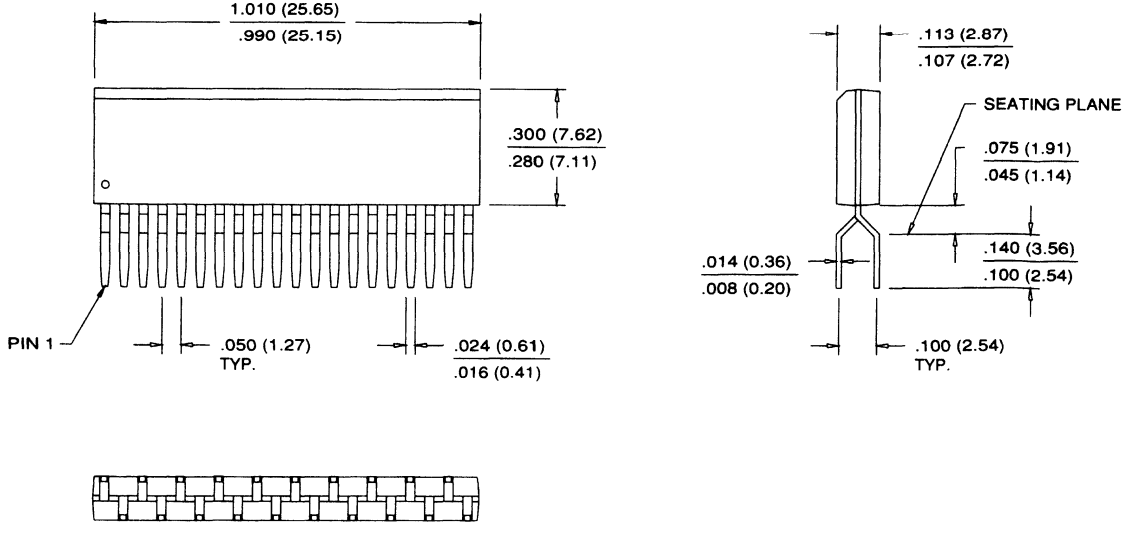
16-PIN PLASTIC ZIP

ZA



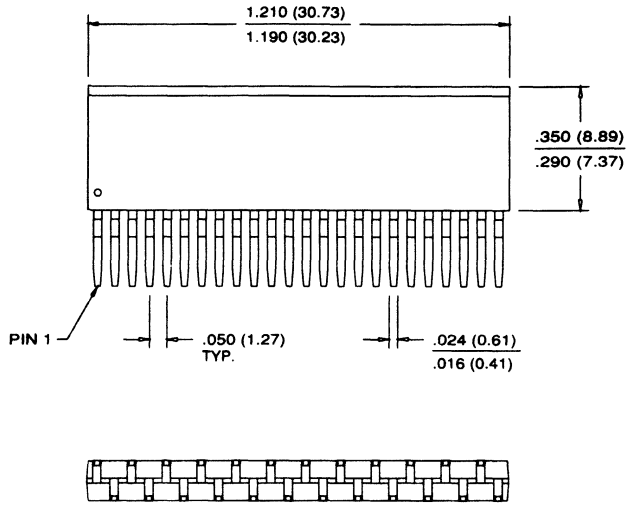
20-PIN PLASTIC ZIP

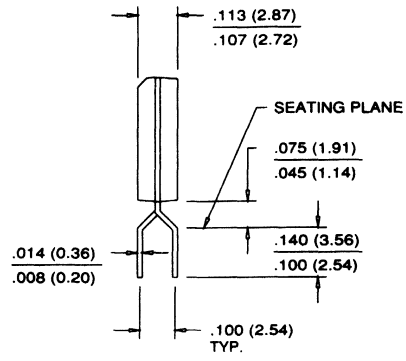
ZB



24-PIN PLASTIC ZIP

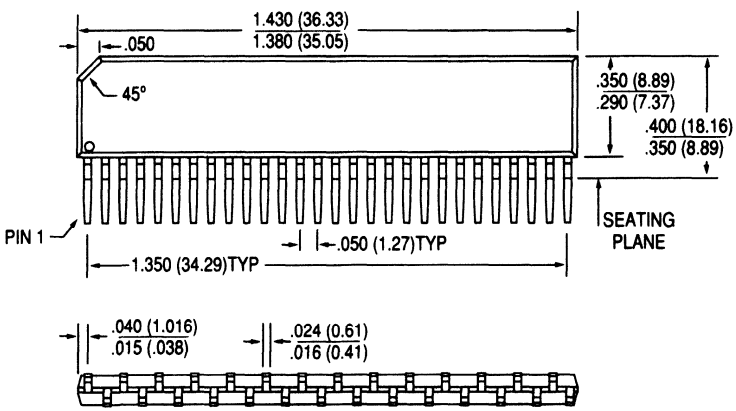
ZC

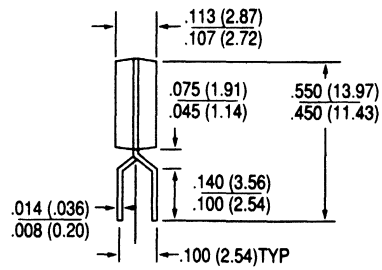




28-PIN PLASTIC ZIP

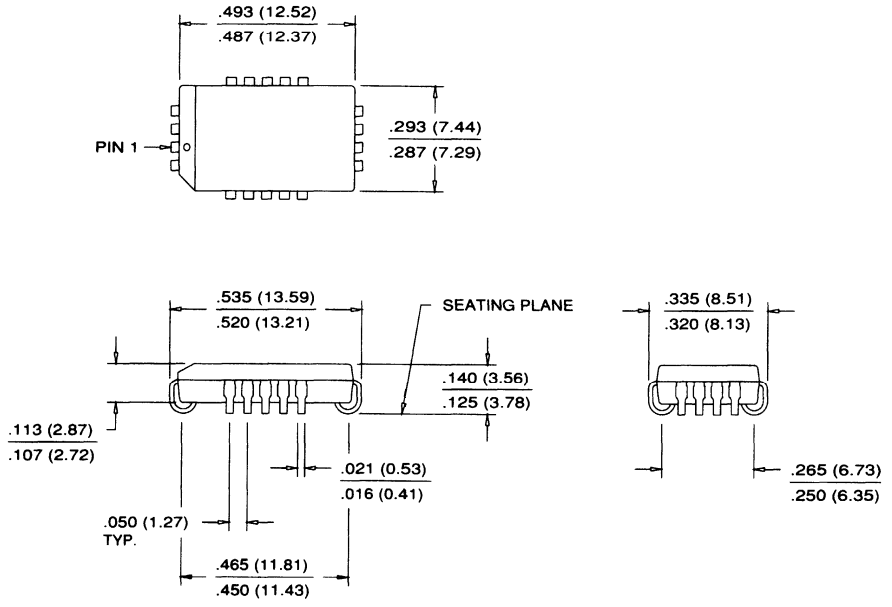
ZD





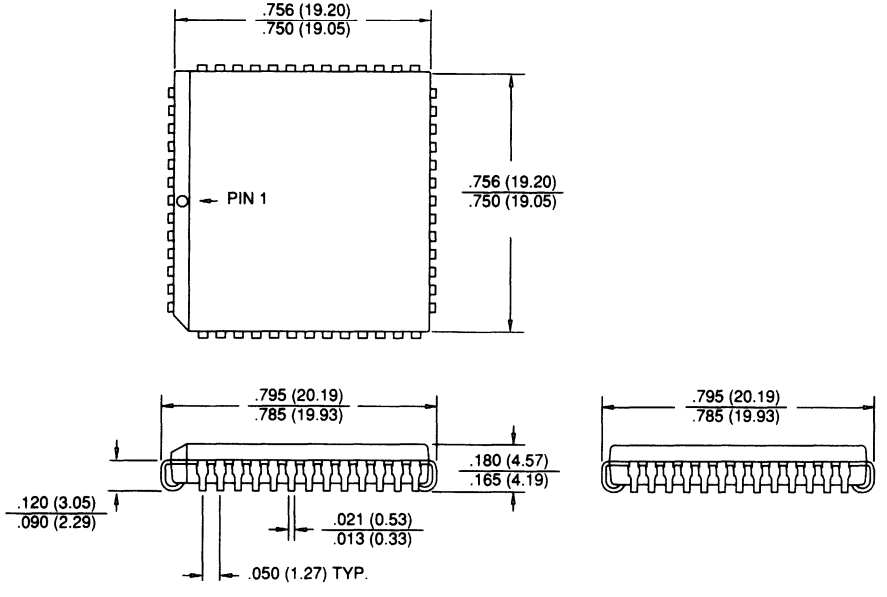
18-PIN PLCC

EJA



52-PIN PLCC

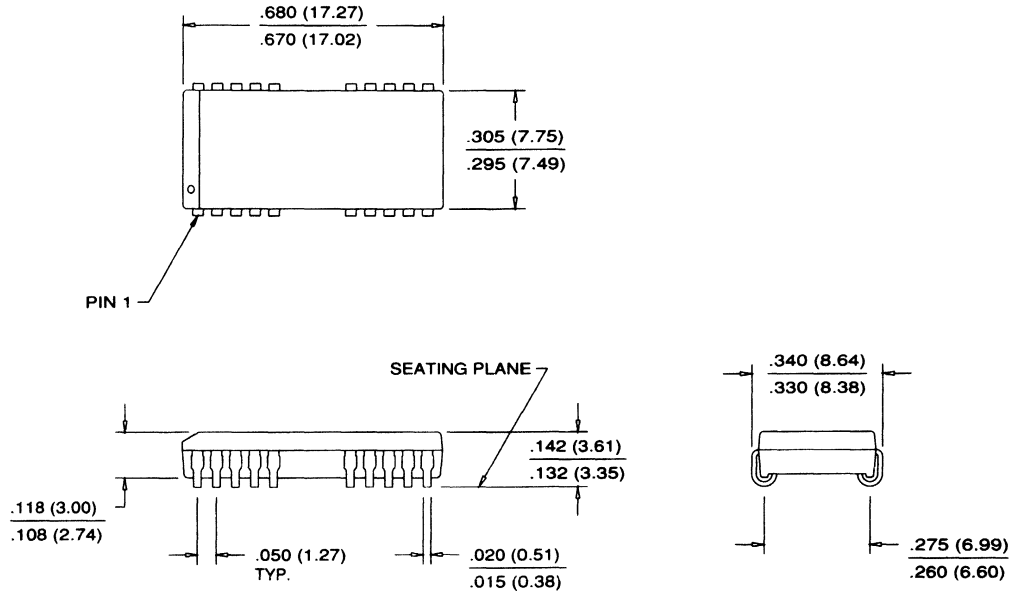
EJB



PACKAGE INFORMATION

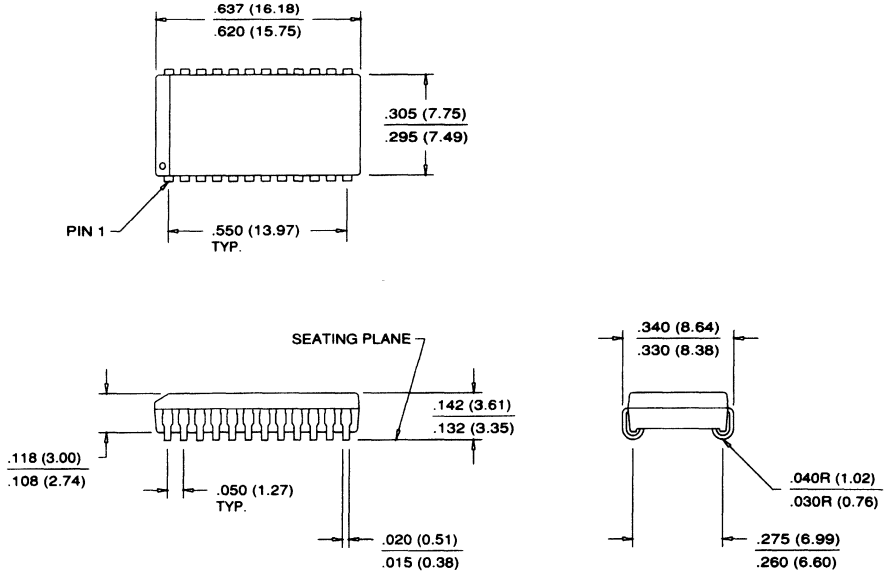
20-PIN PLASTIC SOJ

DJA



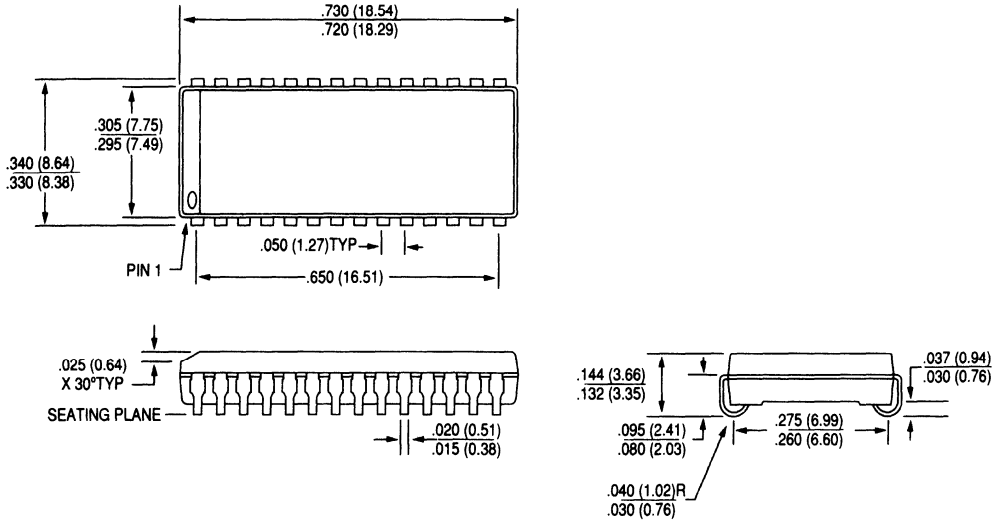
24-PIN PLASTIC SOJ

DJB



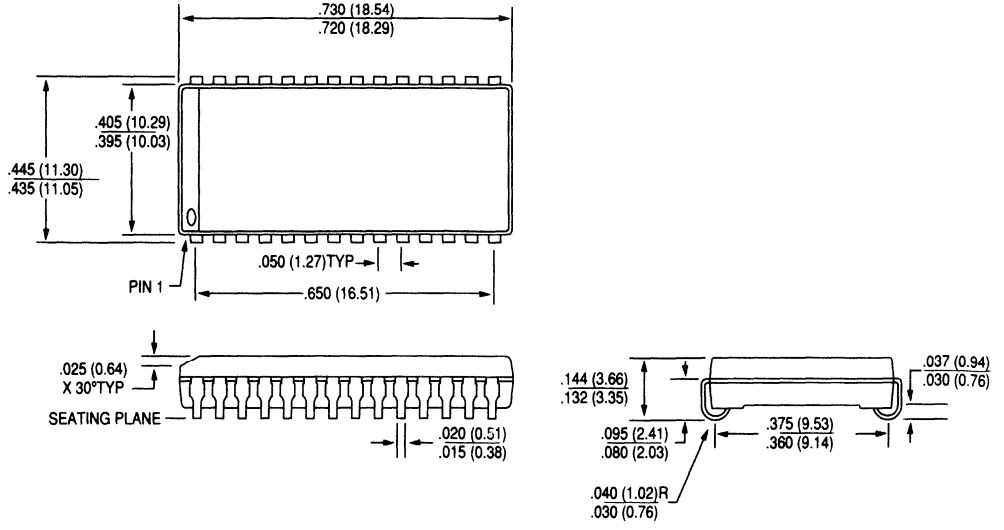
28-PIN PLASTIC SOJ

DJC



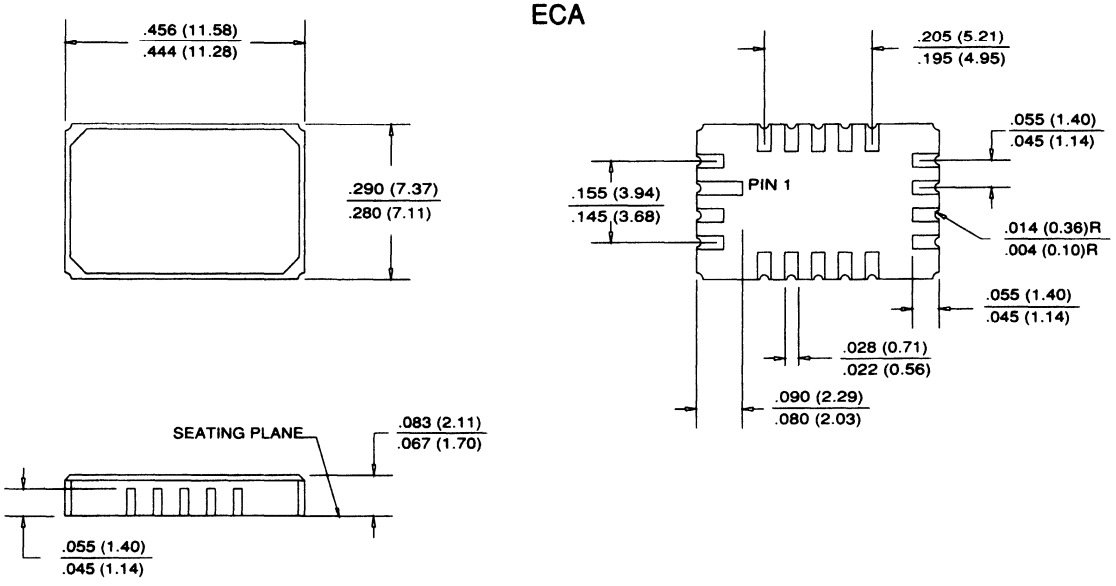
28-PIN PLASTIC SOJ

DJD



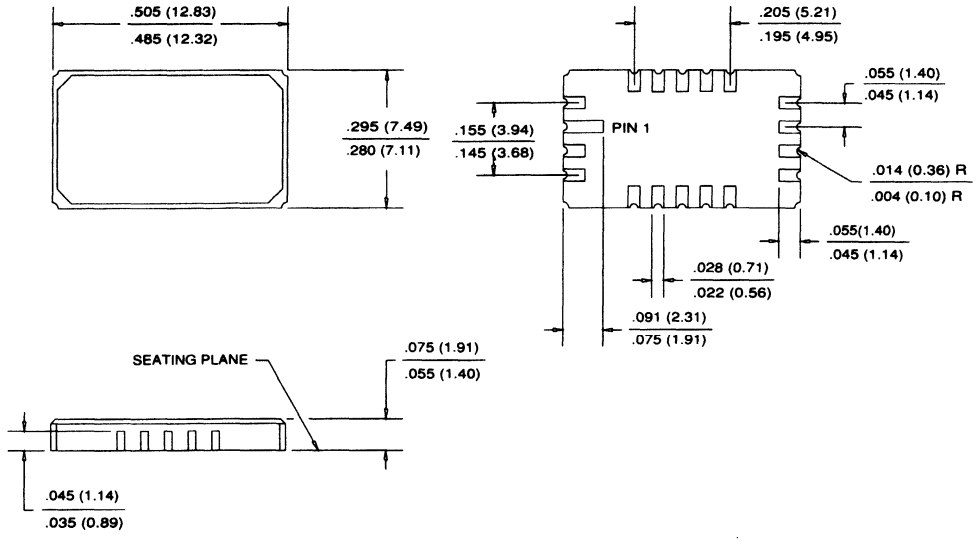
18-PIN CERAMIC LCC

ECA



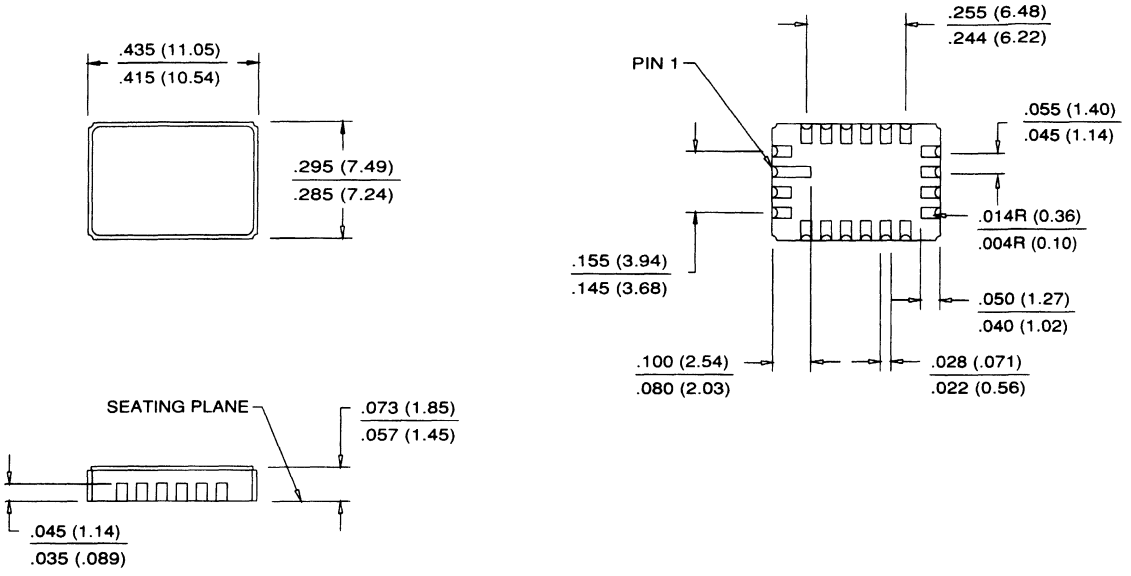
18-PIN CERAMIC LCC

ECB



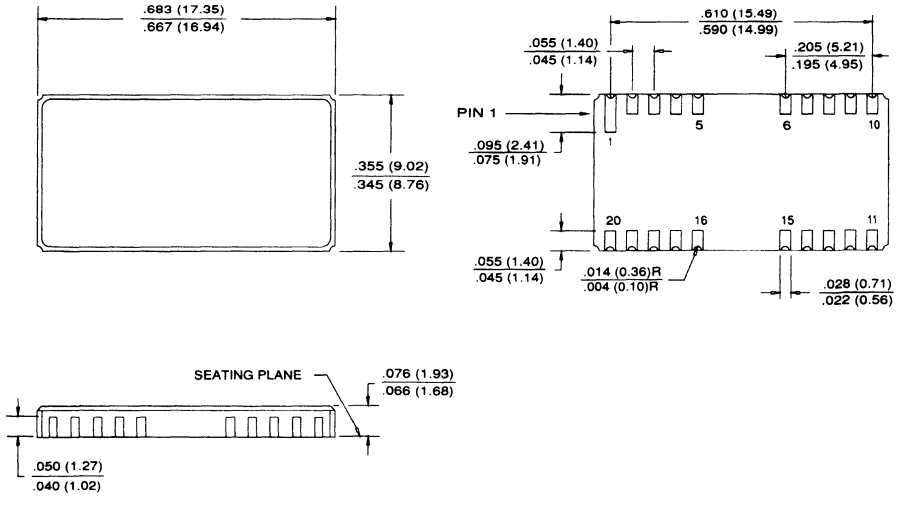
20-PIN CERAMIC LCC

ECC



20-PIN CERAMIC LCC

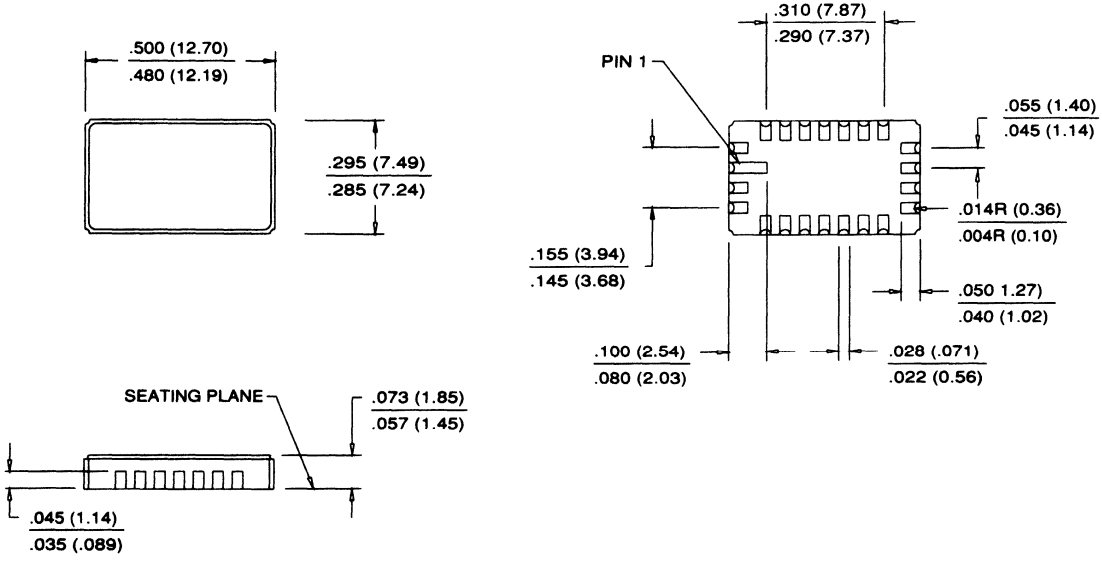
ECD



PACKAGE INFORMATION

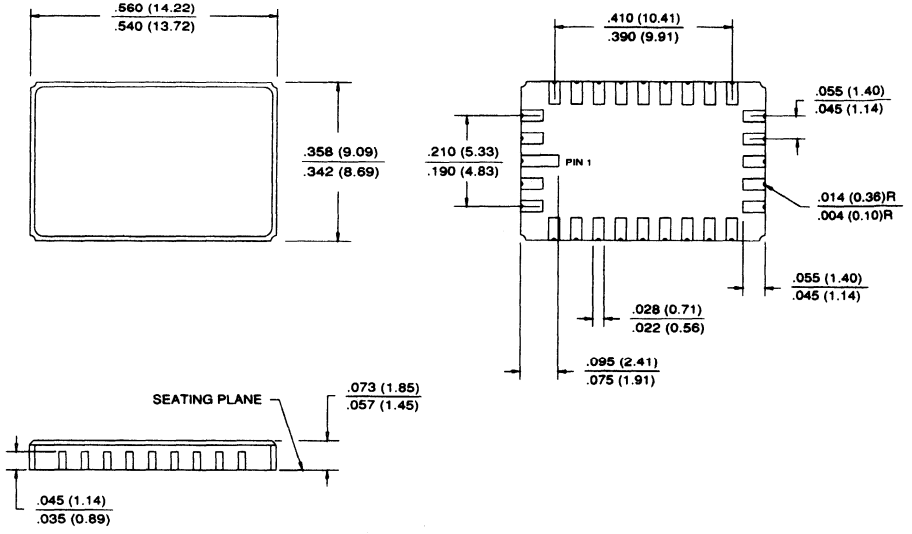
22-PIN CERAMIC LCC

ECE



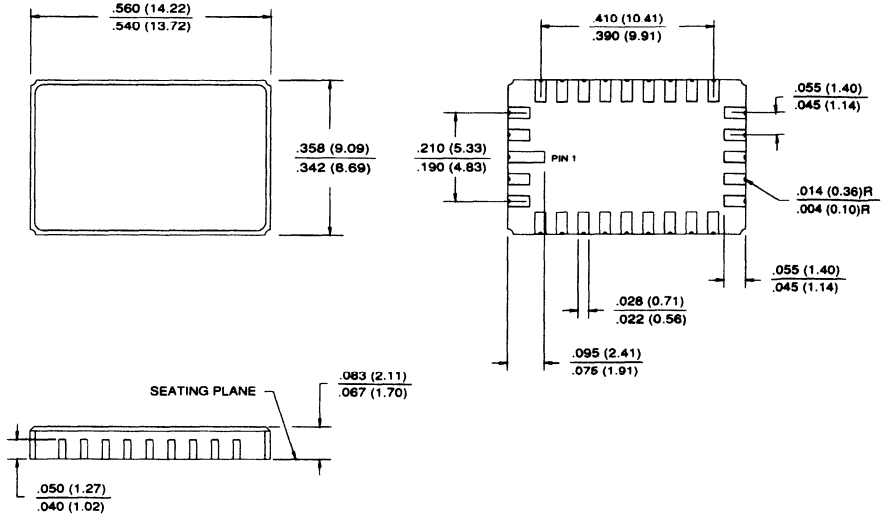
28-PIN CERAMIC LCC

ECF



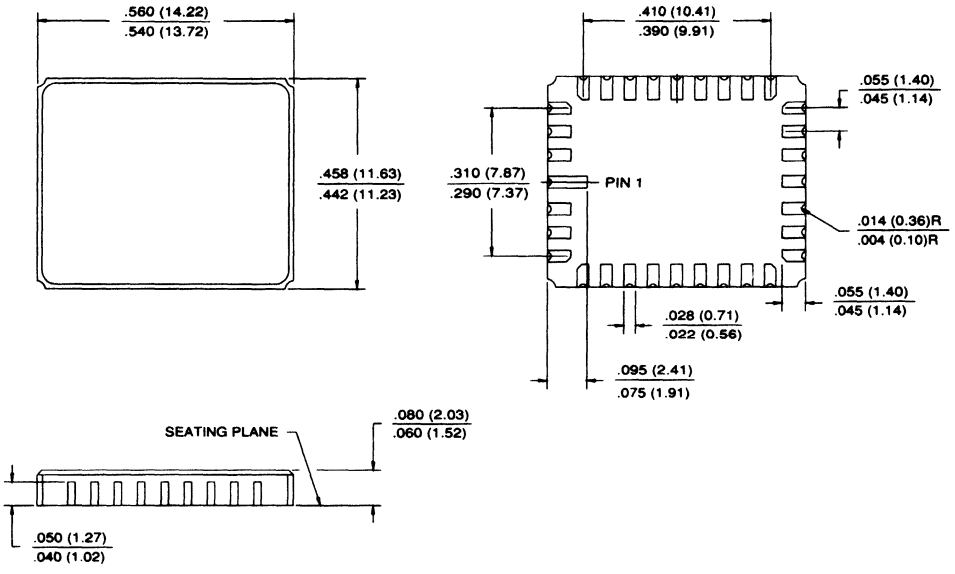
28-PIN CERAMIC LCC

ECG



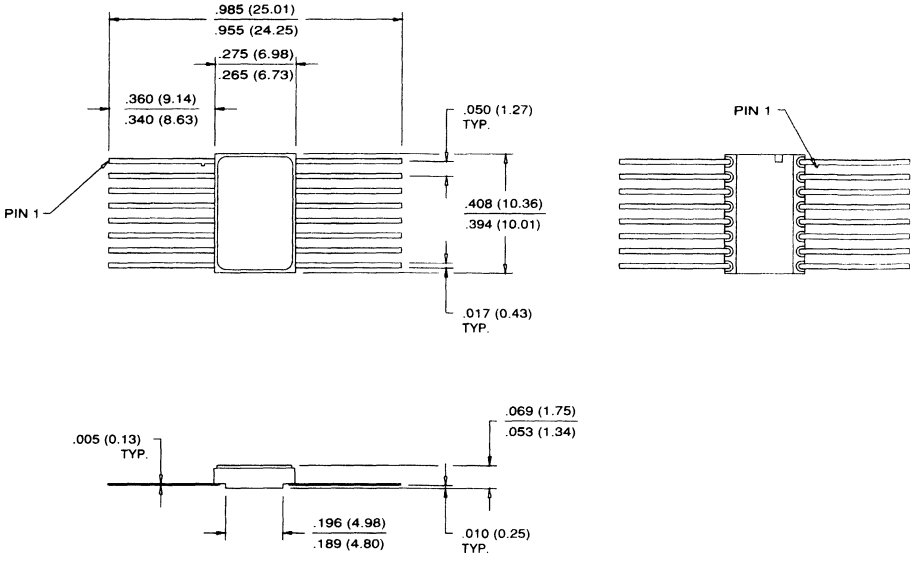
32-PIN CERAMIC LCC

ECH



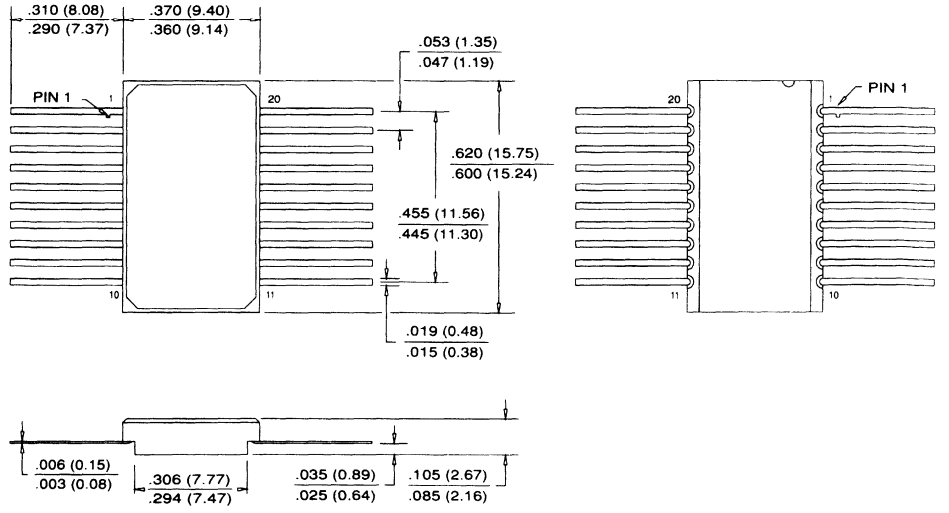
16-PIN FLAT PACK

FA

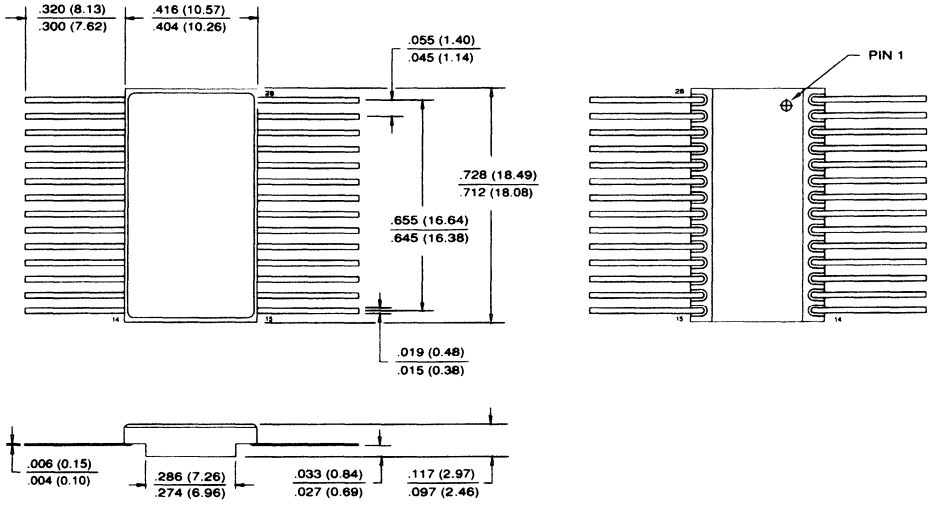


20-PIN FLAT PACK

FB

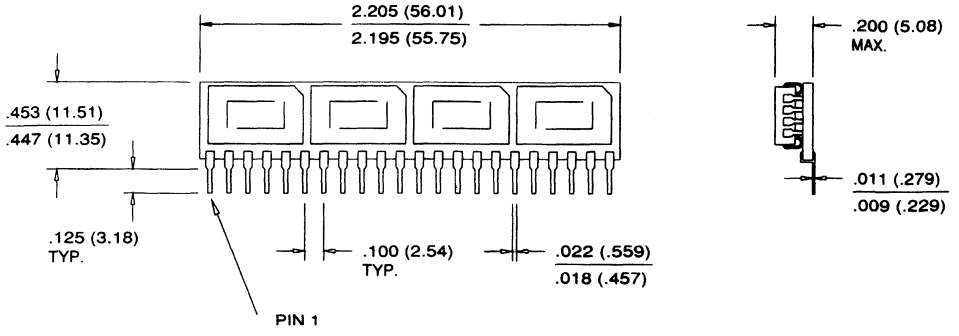


28-PIN FLAT PACK
FC



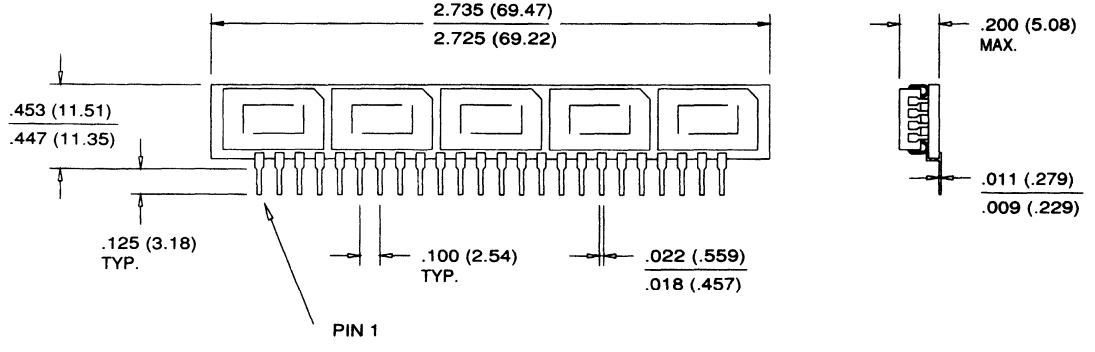
22-PIN MODULE SIP (LOW PROFILE)

MA

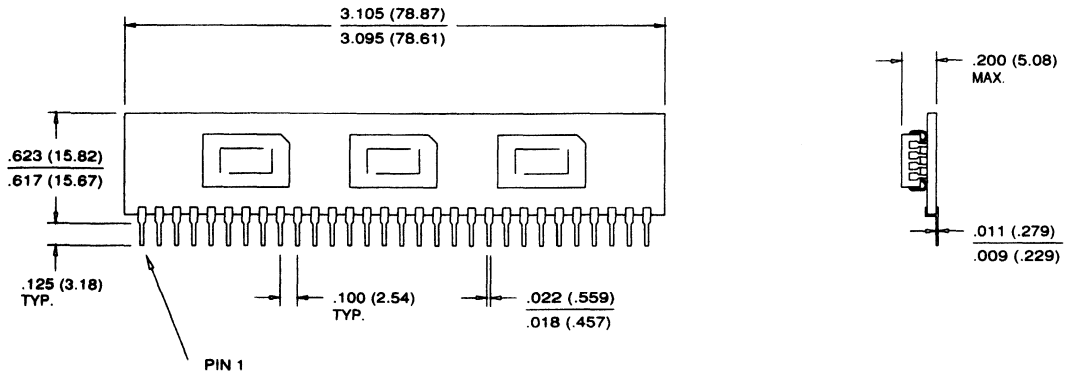


24-PIN MODULE SIP (LOW PROFILE)

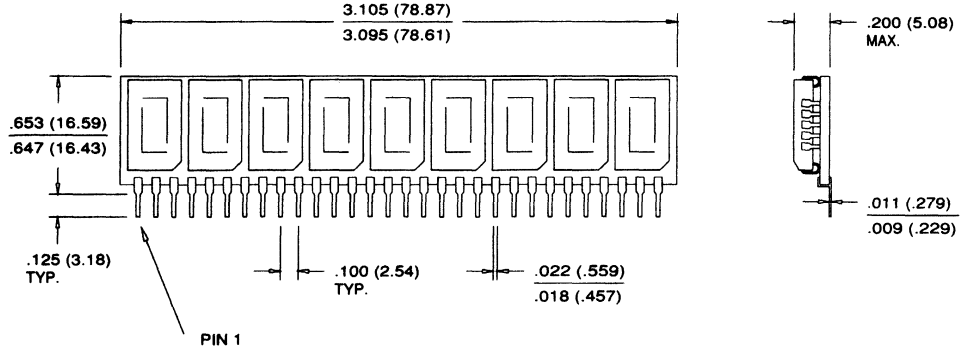
MB



30-PIN MODULE SIP
MC

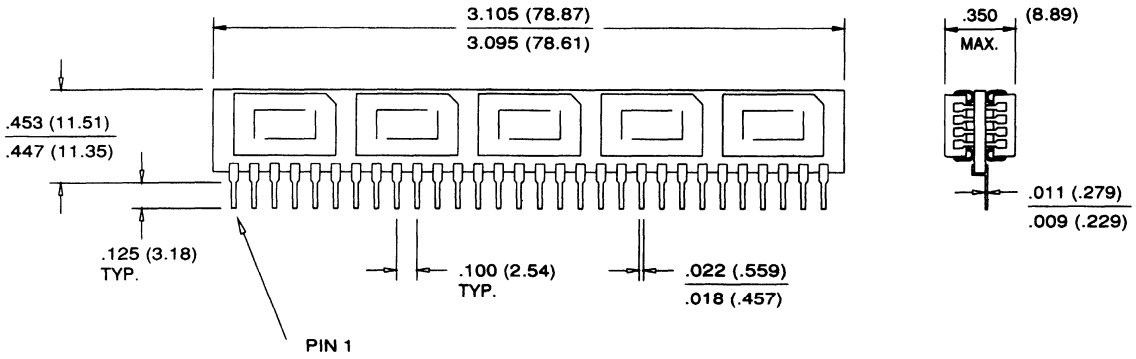


30-PIN MODULE SIP
MD



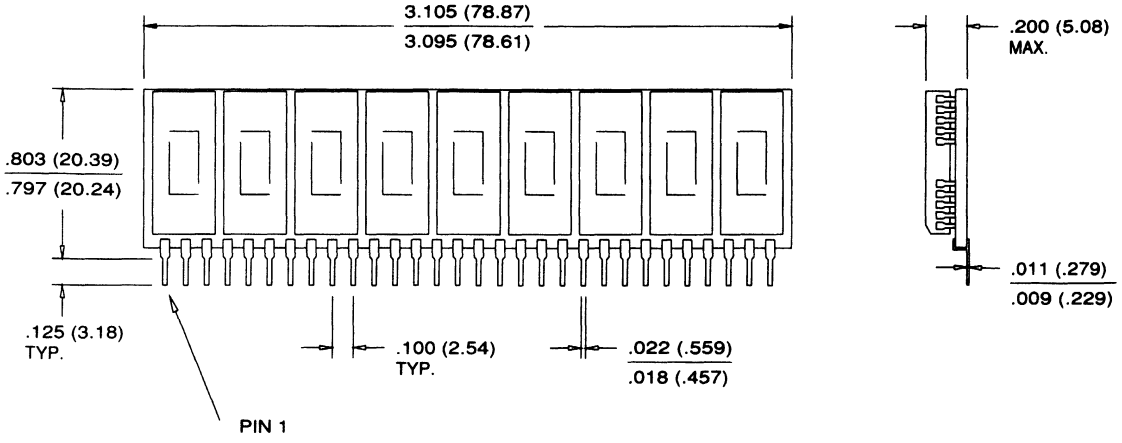
30-PIN MODULE SIP (LOW PROFILE)

ME

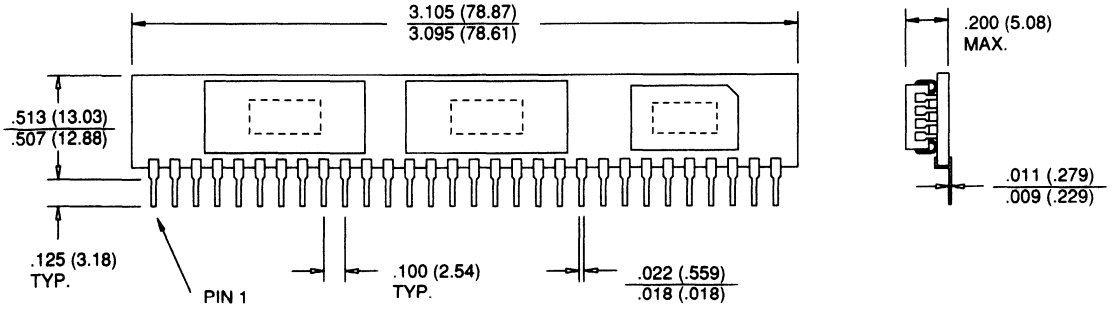


30-PIN MODULE SIP

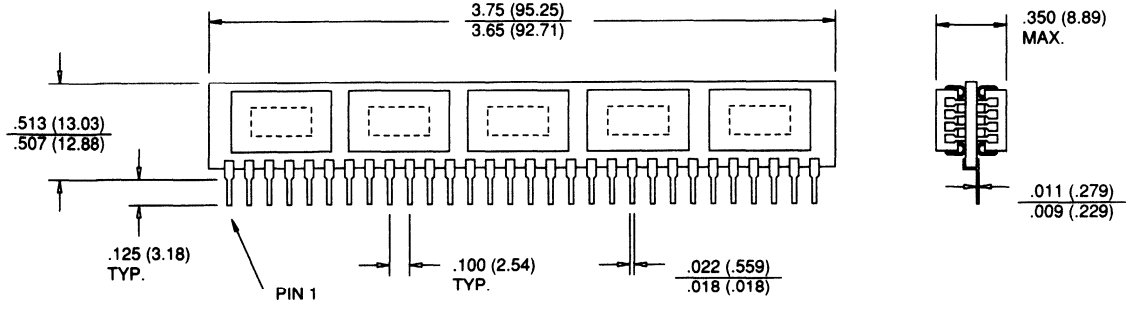
MG



30-PIN MODULE SIP (LOW PROFILE)
MH

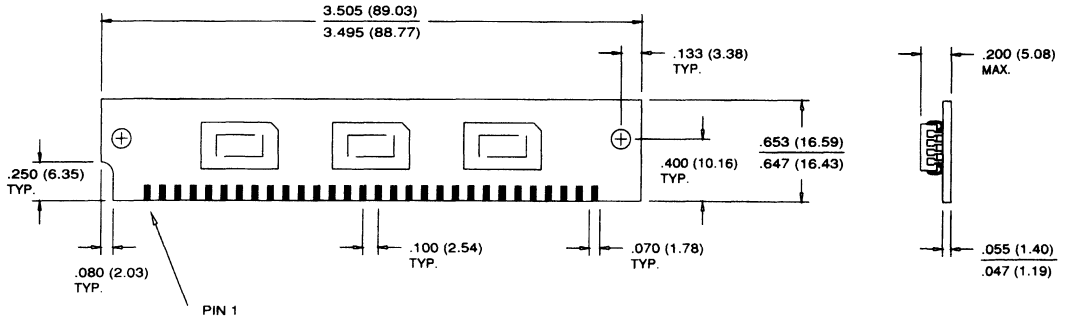


30-PIN MODULE SIP (LOW PROFILE)
MI



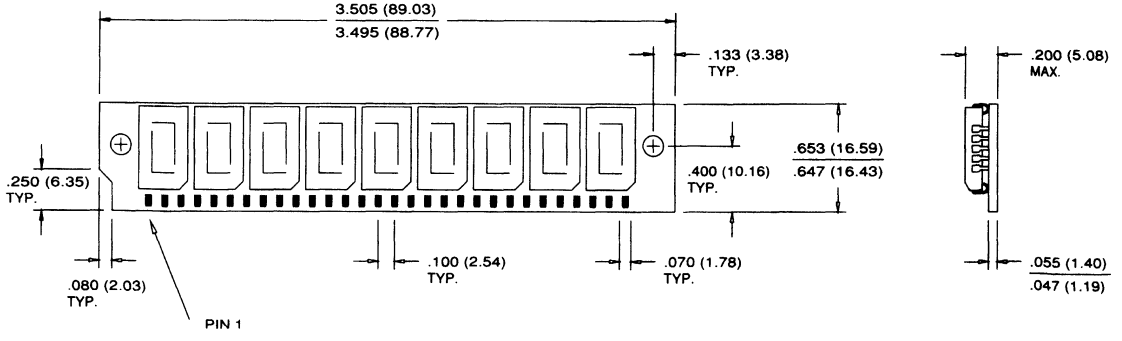
30-PIN MODULE SIMM

MJ

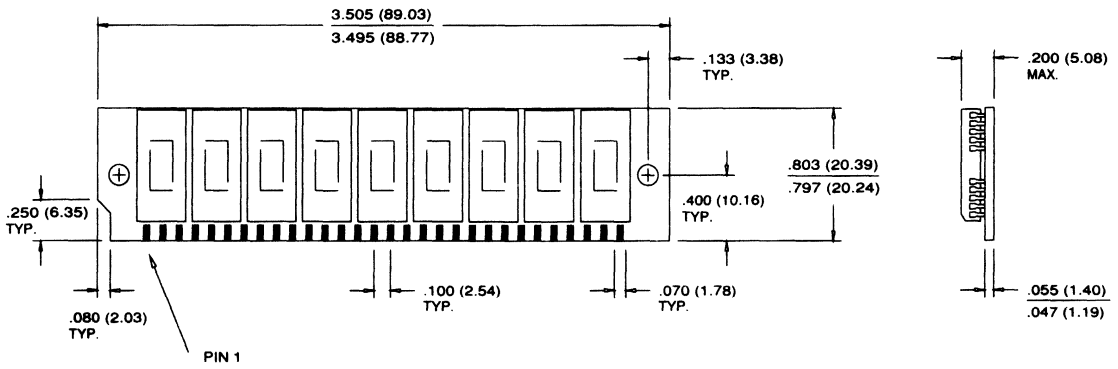


30-PIN MODULE SIMM

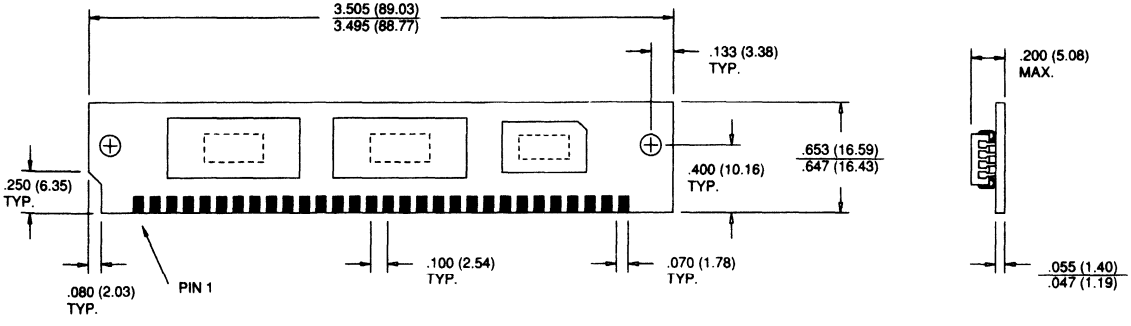
MK



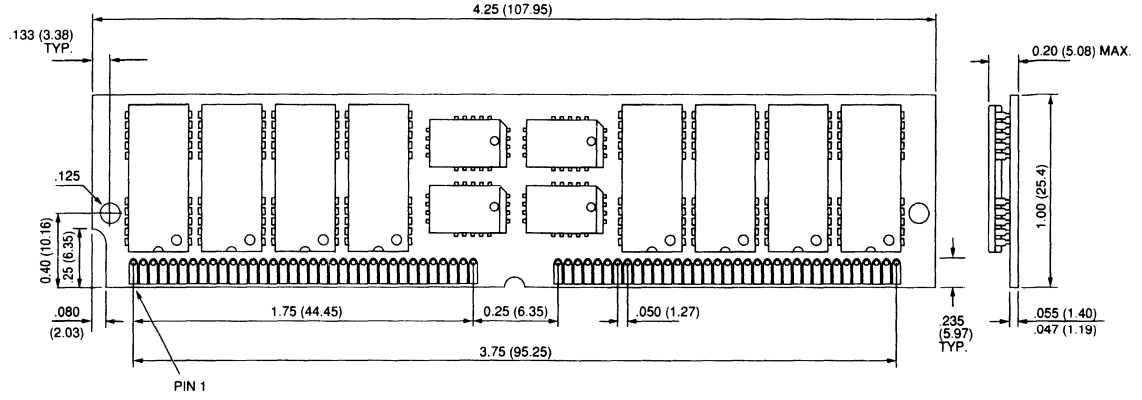
30-PIN MODULE SIMM
ML



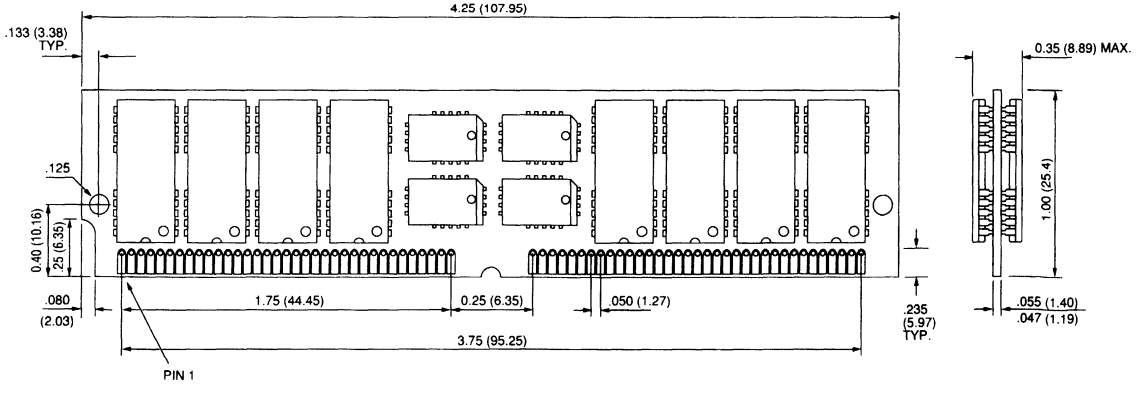
30-PIN MODULE SIMM
MM



72-PIN MODULE SIMM
MN

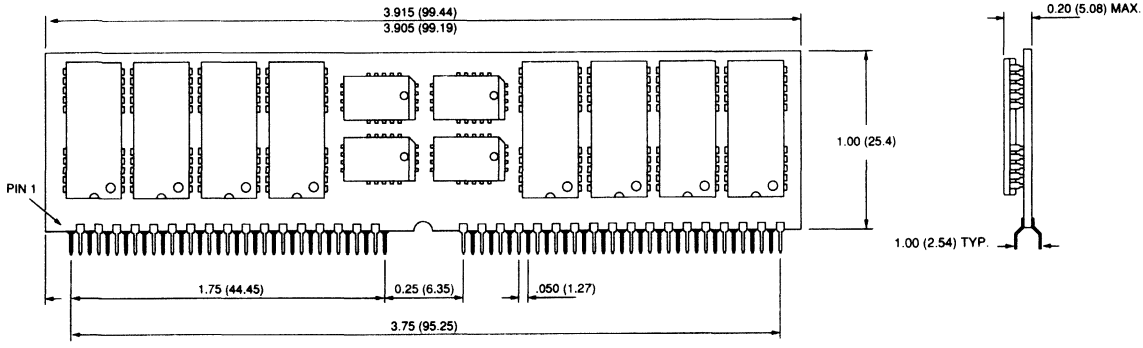


72-PIN MODULE SIMM
MO

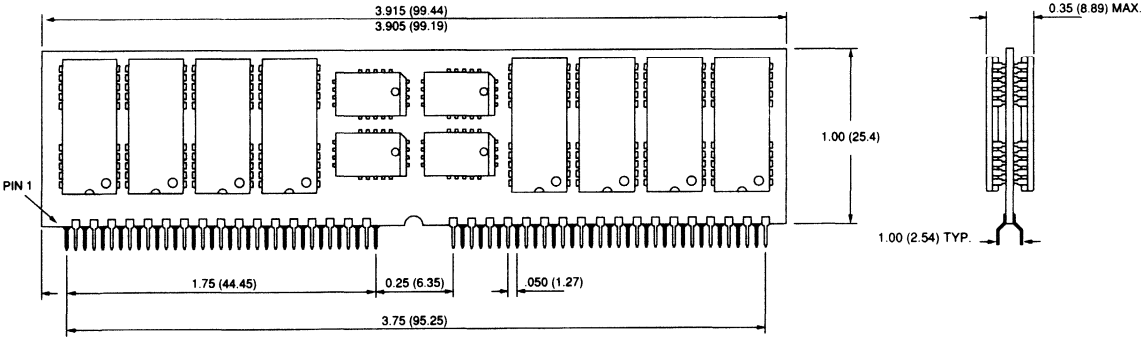


Note: All dimensions listed as typical.

72-PIN MODULE ZIP
MP



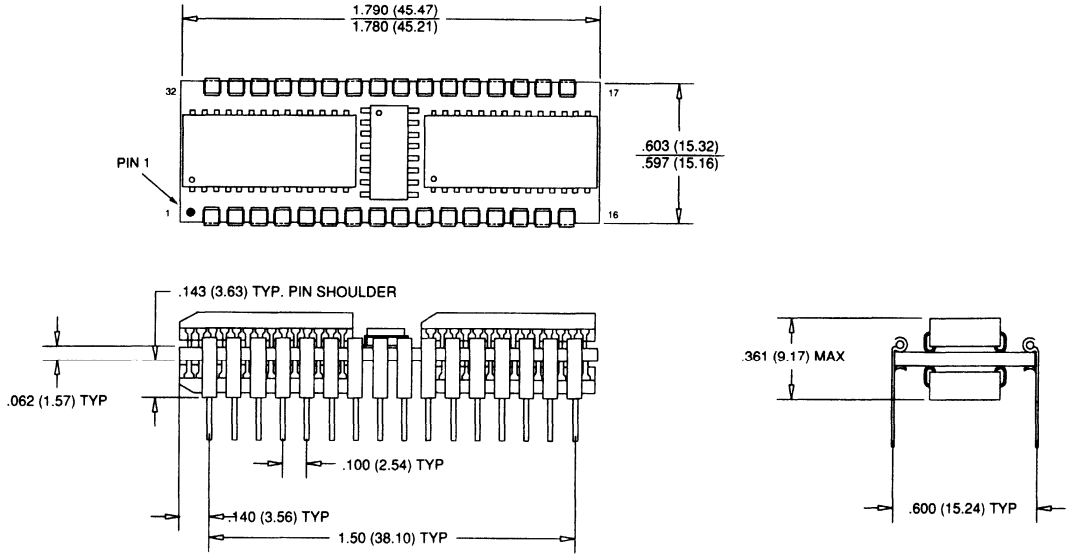
72-PIN MODULE ZIP
MQ



Note: All dimensions listed as typical.

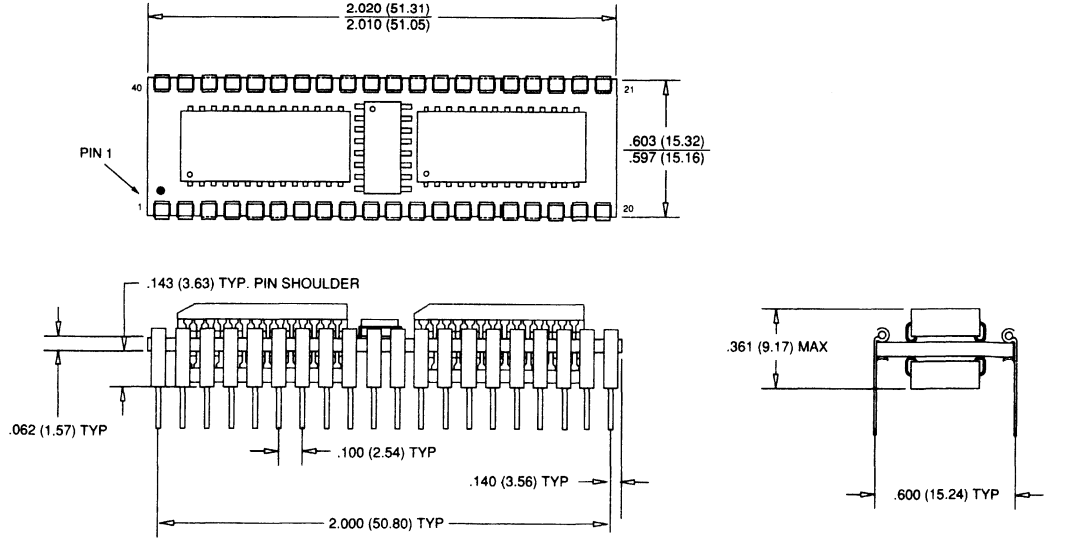
32-PIN MODULE DIP

MR



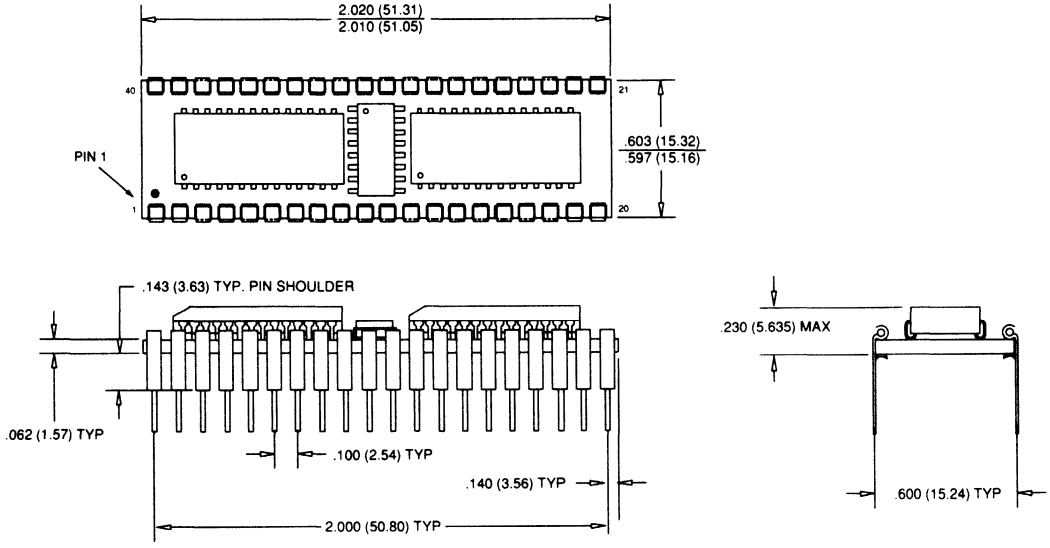
40-PIN MODULE DIP

MS



40-PIN MODULE DIP

MT



MICRON

DYNAMIC RAMs 1

DYNAMIC RAM MODULES 2

MULTIPORT DYNAMIC RAMs 3

STATIC RAMs 4

STATIC RAM MODULES 5

CACHE DATA RAMs 6

FIFO MEMORIES 7

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PACKAGE INFORMATION 10

SALES INFORMATION 11

Micron Component Group Product Numbering System

Format = AA BB CC DDDD EEE-FF GG GG*

PRODUCT FAMILY

DRAM (< 1MEG)	= BLANK
DRAM (≥1MEG)	= 4
DPDRAM	= 42
SRAM	= 5
FIFO	=52
CACHE SRAM	=56
MODULE	
DRAM	=8
SRAM	=85

DEVICE NUMBER
(NUMBER CAN BE MODIFIED TO INDICATE VARIATIONS)

DRAM	= BITS, WORDS
DPDRAM	= BITS, WORDS
TPDRAM	= BITS, WORDS
SRAM	= DENSITY, BITS
FIFO	= BITS, WORDS

ACCESS TIME

-10 = 10ns or 100ns
-12 = 12ns or 120ns
-15 = 15ns or 150ns
-20 = 20ns or 200ns
-25 = 25ns or 250ns
-35 = 35ns or 350ns
-45 = 45ns
-55 = 55ns
-60 = 60ns
-70 = 70ns
-80 = 80ns
-85 = 85ns

AA	BB	CC	DDDD	EEE	FF	GG GG*

PRODUCT LINE IDENTIFIER

MT = Micron Technology Component Product

PROCESS TECHNOLOGY

NMOS	= BLANK
CMOS	= C

PACKAGE CODE

PLASTIC	
DIP	= BLANK
DIP (Wide Body)	= W
ZIP	= Z
LCC	= EJ
SOJ	= DJ
SOIC	= G
CERAMIC	
DIP	= C
DIP (Wide Body)	= CW
LCC	= EC
LCC (Wide Body)	= ECW
SOIC	= CG
PGA	= CA
FLAT PACK	= F
MODULE	
PC BOARD DIP	= BLANK
CERAMIC DIP	= C
SIMM	= M
SIMM (Gold plated)	= GM
SIP	= MN,N
SIP (Double Sided)	= DMN,DN
SIP, ZIG-ZAG	= ZN

PROCESSING* LEVEL/TEMP/SPECIAL

Commercial Process	
0 C TO +70 C	= BLANK
-55 C TO +125 C	= XT
-40 C TO +125 C	= AT
-40 C TO +85 C	= IT
MIL STD 883C	
-55 C to +125 C or +110 C (DRAMs)	= 883C
0 C TO +70 C	= M070
2V Data Retention	= L
Tape and Reel	= TR
Bar Code	= BC

* Multiple processing codes are separated by a space.

ORDER INFORMATION

Micron products are manufactured and quality controlled in our state-of-the-art Boise, Idaho USA facility. All products are functionally equivalent to other manufacturers' products meeting industry standards.

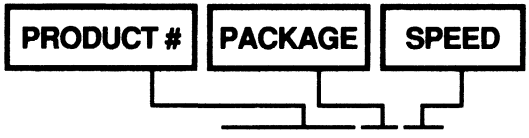
Device functionality is consistently assured over a wider power supply, temperature range and operational range than specified. Each unit receives accelerated burn-in and several hours of system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Our QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability.

ORDER EXAMPLES:

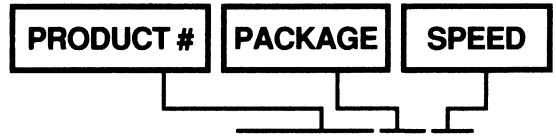
DRAM

1MEG X 1, 100ns in Plastic SOJ



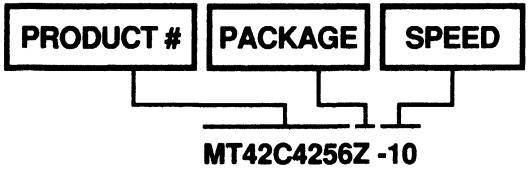
DRAM MODULE

1 MEG X 8, 120ns Fast Page Mode Access, Leaded SIP



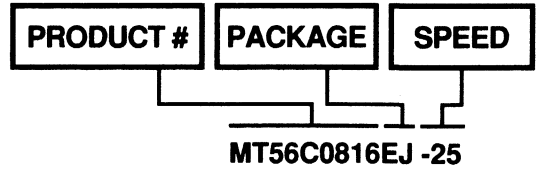
MULTIPORT DRAM (VRAM)

256K X 4, 100ns in ZIP



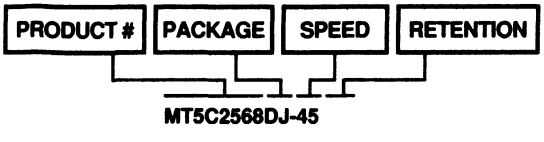
CACHE DATA SRAM

Dual 4K X 16, Single 8K X 16, 25ns in Plastic LCC



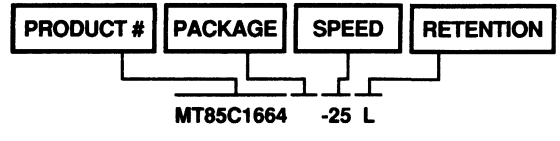
SRAM

32K X 8, 45ns in Plastic SOJ



SRAM MODULE

64K X 16, 25ns in DIP Module with 2 volt data retention



ALABAMA

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Fax - 205-534-2384

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Phone - 205-837-8700
TWX - 810-726-2187

Pioneer Technology
4825 University Square
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Phone - 205-837-9300
TWX - 810-726-2197
FAX - 205-837-9358

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4645 South Lakeshore Drive
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Tempe, AZ 85282
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FAX 602-820-7054

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1727 East Weber Drive
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